

M56620AP

Bi-CMOS 8-BIT PARALLEL-INPUT LATCHED DRIVER

DESCRIPTION

The M56620AP is a semiconductor integrated circuit fabricated using Bi-CMOS technology. It contains bipolar 8 output drivers of CMOS latch.

FEATURES

- Enable input for output control
- Low supply current $I_{CC} \leq 10\mu A$ at standby
- Input level is compatible with standard CMOS
- Driver: Withstand voltage $BV_{CEO} \geq 50V$
Large drive current ($I_{O(max)} = 500mA$)
- Wide operating temperature range $T_a = -20 - +75^\circ C$

APPLICATION

Thermal printer head dot driver, Relay driver, Solenoid driver

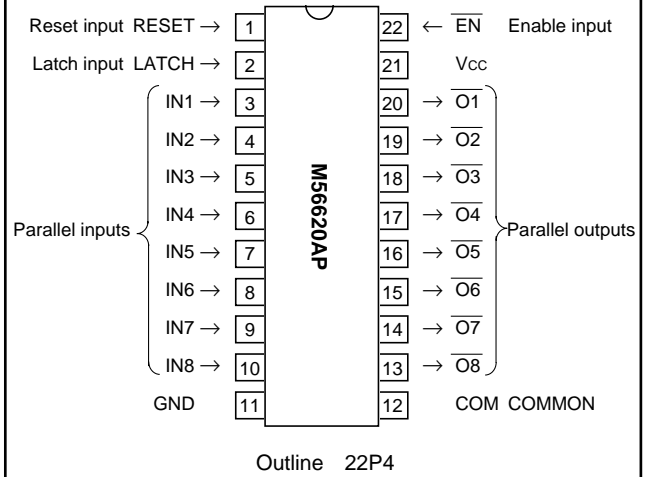
FUNCTION

When data is applied to inputs IN1 – IN8 and LATCH input is set to “H”, the data will be latched with the truth table. Note that when an “H” signal is applied to the RESET input, the latch will maintain the reset state.

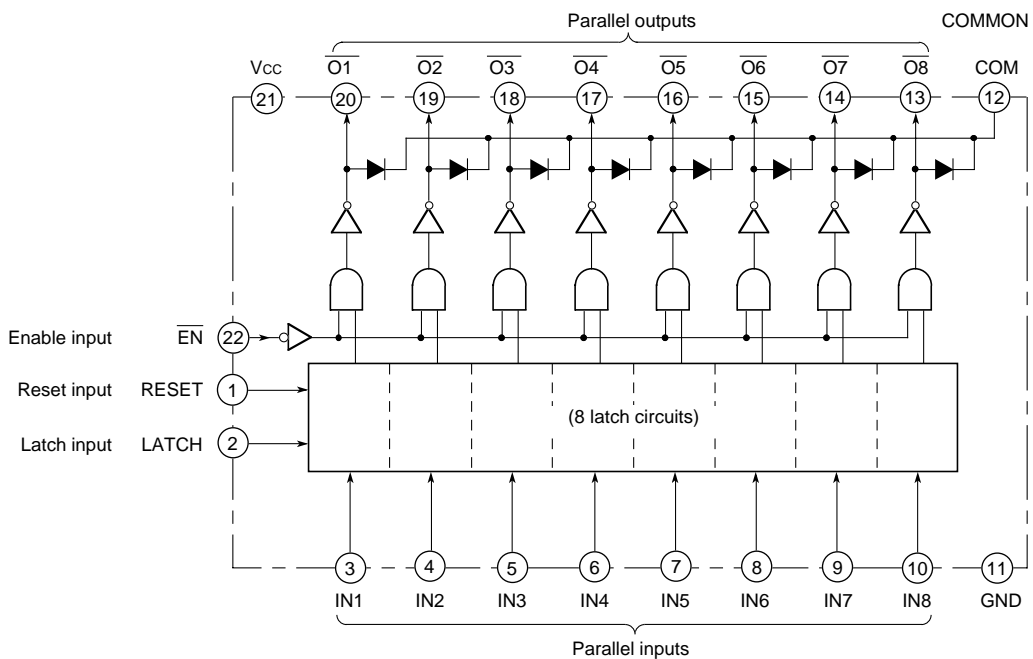
When the \overline{EN} input is set to “L” and the data maintained in the latch are “H”, the corresponding output will be ON and become “L”.

When both the LATCH and RESET inputs are “L”, the latch will maintain the prior state irrespective of input signals IN1 – IN8.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



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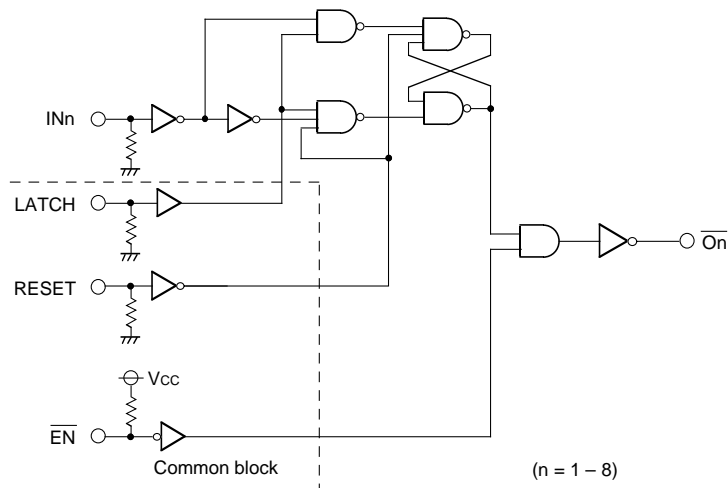
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TRUTH TABLE

IN _n	Input			Output $\overline{\text{On}}$	
	LATCH	RESET	$\overline{\text{EN}}$	t-1	t
L	H	L	L	x	H
H	H	L	L	x	L
x	x	H	x	x	H
x	x	x	H	x	H
x	L	L	L	L	L
x	L	L	L	H	H

L: low level
 H: high level
 x: low level or high level
 t-1: previous state
 t: current state
 H output: OFF state
 L output: ON state

LOGIC DIAGRAM (One circuit)

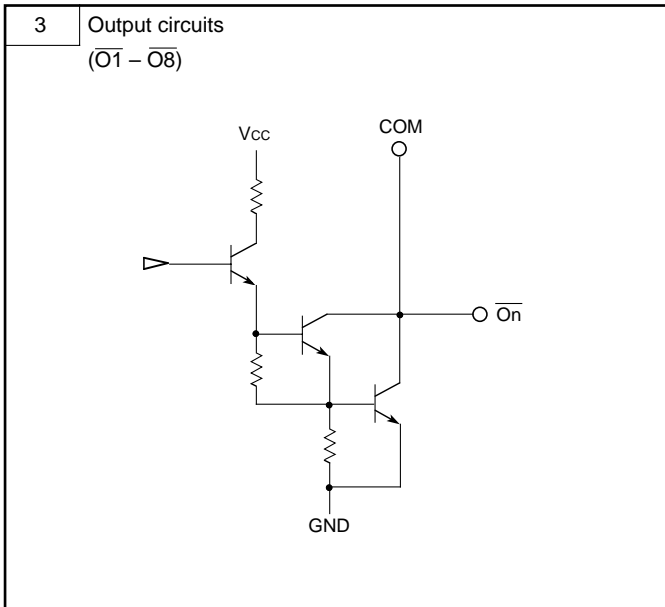


INPUT/OUTPUT EQUIVALENT CIRCUITS

<p>1 Input circuits (IN_n, LATCH, RESET)</p> <p style="text-align: center;">(n = 1 - 8)</p>	<p>2 Input circuit ($\overline{\text{EN}}$)</p>
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ABSOLUTE MAXIMUM RATINGS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.3 – +8	V
Vi	Input voltage		-0.3 – Vcc+0.3	V
Vo	Output voltage	Output: OFF	0 – +50	V
Io	Output current	Output: ON	500	mA
Pd	Power dissipation	Ta=25°C	1.25	W
Topr	Operating temperature		-20 – 75	°C
Tstg	Storage temperature		-55 – 125	°C

RECOMMENDED OPERATING CONDITION (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage		4	5	6	V
Vo	Output apply voltage	Output: OFF			50	V
Io	Output current (per circuit)	All outputs go in ON state simultaneously. Duty cycle < 15%			350	mA

ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VIH	High-level input voltage	Ta=-20 – 75°C	0.7Vcc		Vcc	V
VIL	Low-level input voltage		0		0.3Vcc	V
RIN	Input resistance	VIN=1.5 – 3.5V	50		2000	kΩ
VOL1	Low-level output voltage	IoL=100mA			1.1	V
VOL2		IoL=200mA			1.3	V
VOL3		IoL=350mA			1.6	V
IoLK	Output leak current	Vo=50V			50	μA
VF	Clamping diode forward voltage	IF=350V			2	V
IR	Clamping diode reverse current	VR=50V			50	μA
ICC1	Supply current	EN=5V, All other inputs = 0V			10	μA
ICC2		EN=0V, One output is ON.		1.0	1.5	mA

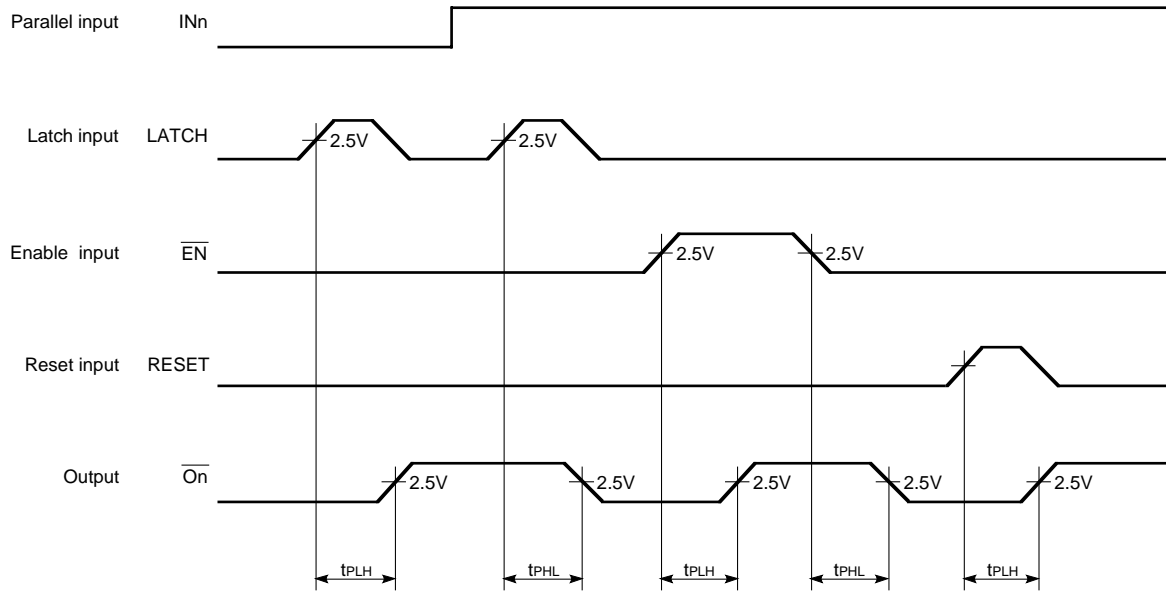
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SWITCHING CHARACTERISTICS (Ta=25°C, Vcc=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tPLH	Low-to-high-level output propagation time From input LATCH to output $\overline{O_n}$	$V_{IH}=5V$ $V_{IL}=0V$ $R_L=100\Omega$ $C_L=15pF$			5	μs
tPHL	High-to-low-level output propagation time From input LATCH to output $\overline{O_n}$				0.5	μs
tPLH	Low-to-high-level output propagation time From input \overline{EN} to output $\overline{O_n}$				5	μs
tPHL	High-to-low-level output propagation time From input \overline{EN} to output $\overline{O_n}$				0.5	μs
tPLH	Low-to-high-level output propagation time From input RESET to output $\overline{O_n}$				5	μs

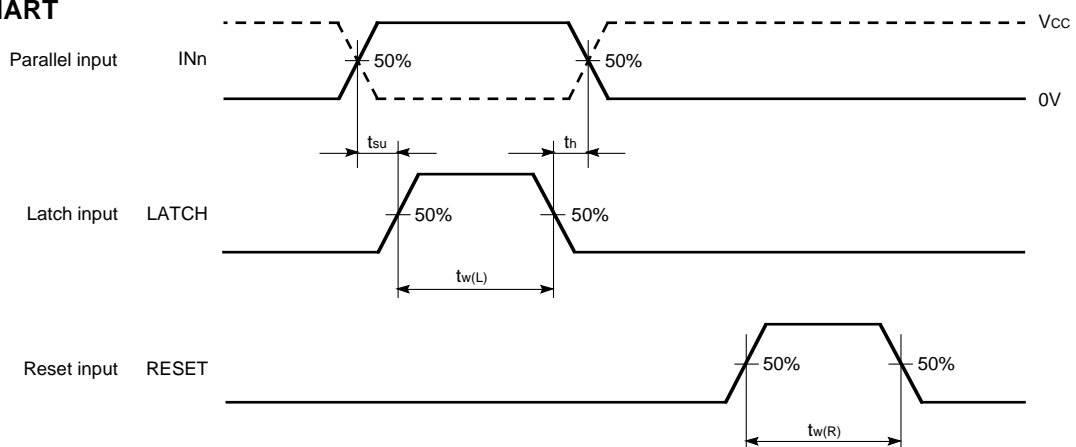
TIMING CHART



TIMING REQUIREMENTS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tw(L)	Latch pulse width		0.1			μs
tw(R)	Reset pulse width		0.1			μs
tsu	Data setup time		0.05			μs
th	Data hold time		0.1			μs

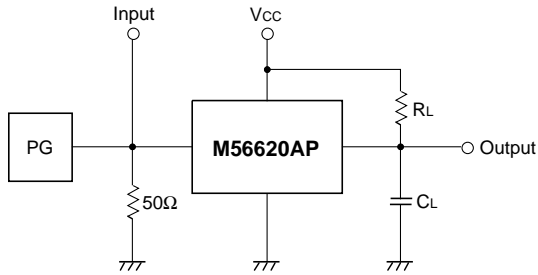
TIMING CHART



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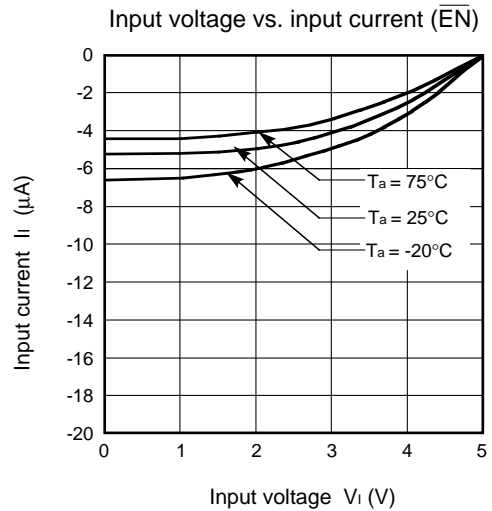
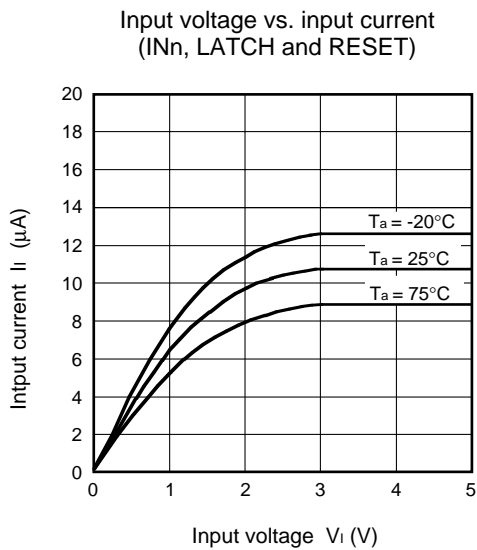
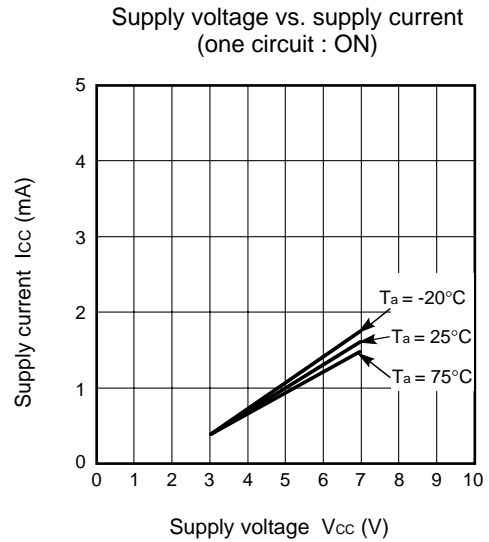
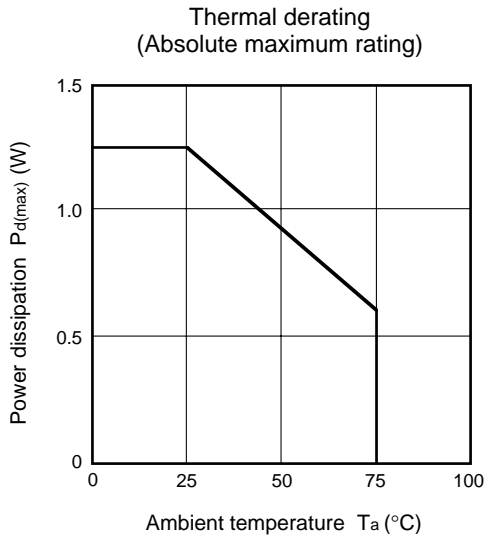
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TEST CIRCUIT



- The input waveform: $t_r \leq 20\text{ns}$, $t_f \leq 20\text{ns}$
- The capacitance C_L includes the wiring stray capacitance and probe input capacitance.

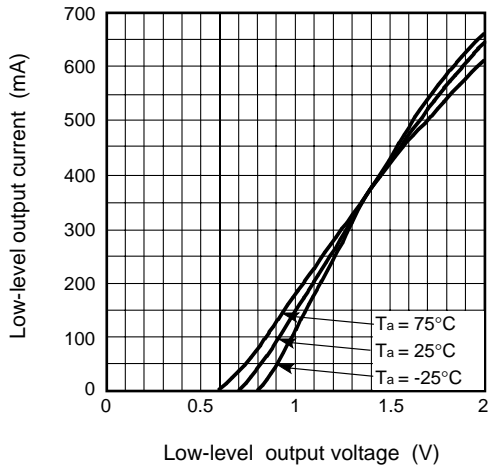
TYPICAL CHARACTERISTICS



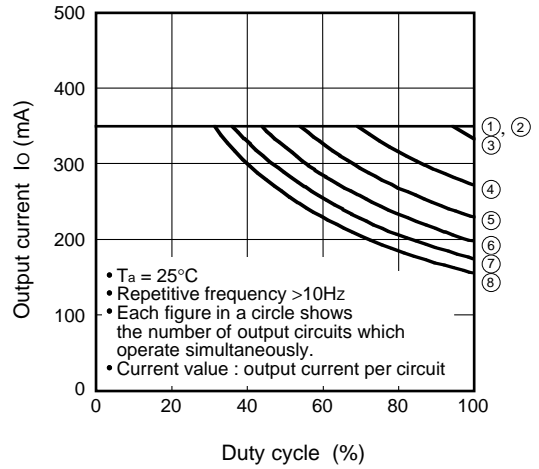
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Bi-CMOS 8-BIT PARALLEL-INPUT LATCHED DRIVER

Low-level output voltage vs. current



Duty cycle vs. allowable output current



Duty cycle vs. allowable output current

