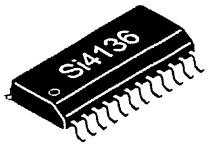
SILICON LABORATORIES

Si4136

ISM RF Synthesizer With Integrated VCOs For Wireless Communications

Features

- Dual-Band RF Synthesizers
  - RF_1 VCO Fixed Frequency Range of 2300 MHz to 2600 MHz
  - RF_2 VCO Fixed Frequency Range of 2000 MHz to 2400 MHz
- IF Synthesizer
  - IFOUT Center Frequency of 62.5 MHz to 1000 MHz
  - Integrated VCOs, Loop Filters, Varactors, and Resonators
- Only Two Passive External Components Required
- Low Phase Noise
- 5 µA Standby Current @ 3 V
- 15.7 mA Typical Supply Current at 3.6 V
- 3.0 V to 3.6 V Operation
- Low Profile 24-pin TSSOP Package



Ordering Information:

See page 27.

Applications

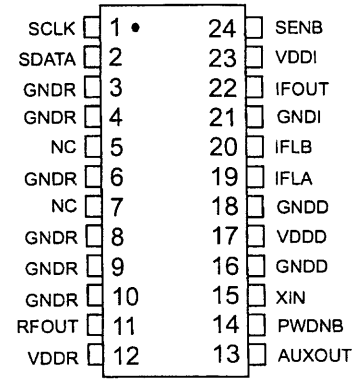
- ISM Band Communications
- Wireless LAN and WAN
- SMR Applications
- Dual-Band Applications

Description

The Si4136 is a monolithic integrated circuit that performs both IF and RF synthesis for wireless communications applications. The Si4136 includes three VCOs, loop filters, reference and VCO dividers, and phase detectors. Variables for dividers and power down settings are programmable through a three-wire serial interface.

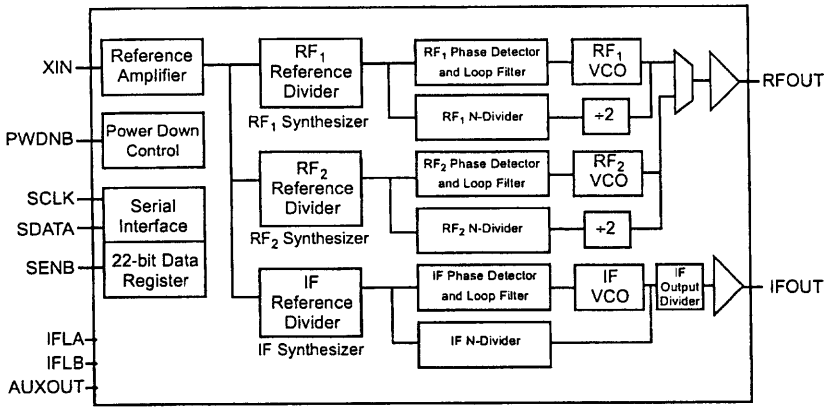
Pin Assignments

Si4136



Patents pending

Functional Block Diagram



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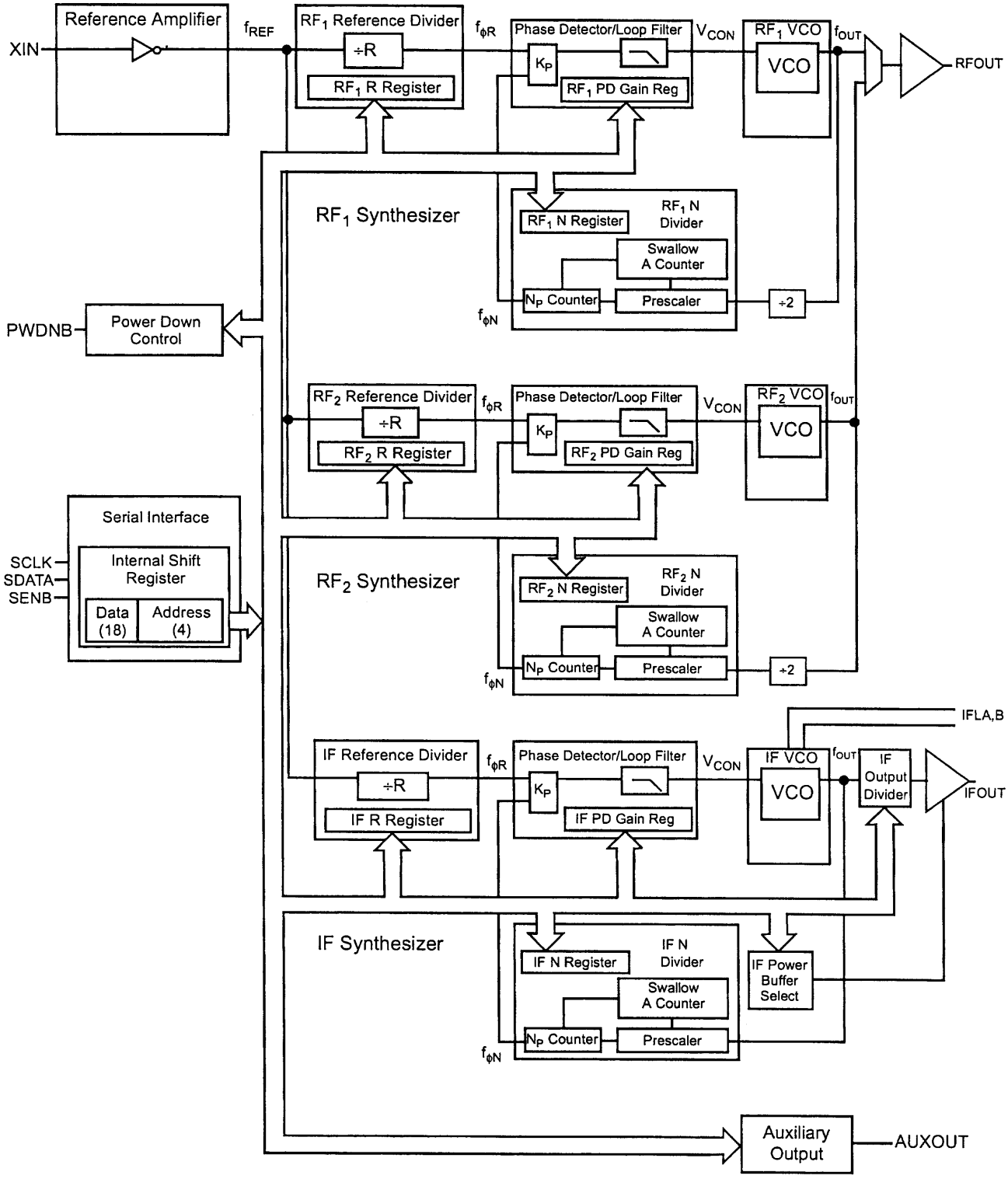

Figure 1. Si4136 Detailed Block Diagram

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Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature—Commercial	T_A		0	25	70	°C
Ambient Temperature—Industrial	T_A		–40	25	85	°C
Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Supply Voltages Difference	V_Δ	$(V_{DDR} - V_{DDD})$, $(V_{DDI} - V_{DDD})$	—	—	0.3	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.

Table 2. DC Characteristics

(V_{DD} = 3.0 to 3.6 V, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF_1 Mode Supply Current[1]	I_{DDRF1}	Typ: 3.6 V at 25°C	—	15.7	—	mA
RF_2 Mode Supply Current[2]	I_{DDRF2}	Typ: 3.6 V at 25°C	—	15.4	—	mA
IF Mode Supply Current[3]	I_{DDD}	Typ: 3.6 V at 25°C	—	10	—	mA
Standby Current	I_{PWDN}	PWDNB = 0, XPDM = 0	—	5	—	µA
		PWDNB = 0, XPDM = 1	—	—	500	µA
High Level Input Voltage[4]	V_{IH}		0.7 V_{DD}	—	—	V
Low Level Input Voltage[4]	V_{IL}		—	—	0.3 V_{DD}	V
High Level Input Current[4]	I_{IH}	V_{IH} = 3.6 V, V_{DD} = 3.6 V	–1	—	1	µA
Low Level Input Current[4]	I_{IL}	V_{IL} = 0 V, V_{DD}= 3.6 V	–1	—	1	µA
High Level Output Voltage[5]	V_{OH}	I_{OH} = –500 µA	V_{DD}–0.4	—	—	V
Low Level Output Voltage[5]	V_{OL}	I_{OH} = 500 µA	—	—	0.4	V

Notes:
1. RF_{OUT} = 2.4 GHz.
2. RF_{OUT} = 2.1 GHz.
3. IF_{OUT} = 800 MHz, LPWR = 0.
4. For signals SCLK, SDATA, SENB, and PWDNB.
5. For signal AUXOUT.

Table 3. AC Characteristics

(V_{DD} = 3.0 to 3.6 V, T_A = –40 to 85°C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Cycle Time	t_{clk}	Figure 2	40	—	—	ns
SCLK Rise Time	t_r	Figure 2	—	—	50	ns
SCLK Fall Time	t_f	Figure 2	—	—	50	ns
SCLK High Time	t_h	Figure 2	10	—	—	ns
SCLK Low Time	t_l	Figure 2	10	—	—	ns
SDATA Setup Time to SCLK↑[2]	t_{su}	Figure 3	5	—	—	ns
SDATA Hold Time from SCLK↑[2]	t_{hold}	Figure 3	0	—	—	ns
SENB↓ to SCLK↑ Delay Time[2]	t_{en1}	Figure 3	10	—	—	ns
SCLK↑ to SENB↑ Delay Time[2]	t_{en2}	Figure 3	12	—	—	ns
SENB↑ to SCLK↑ Delay Time[2]	t_{en3}	Figure 3	12	—	—	ns
SENB Pulse Width	t_w	Figure 3	10	—	—	ns
Power Up Request to Synthesizer Ready[3,4] Time	t_{pup}	Figure 5, Figure 6	—	$80/f_\phi$	$100/f_\phi$	
Power Up Request to Synthesizer Ready[3,5] Time	t_{pup}	Figure 5, Figure 6	—	$40/f_\phi$	$50/f_\phi$	
Power Down Request to Synthesizer Off[6] Time	t_{pdn}	Figure 5, Figure 6	—	—	100	ns

Notes:

1. All timing is referenced to the 50% level of the waveform, unless otherwise noted.
2. Timing is not referenced to 50% level of the waveform. See Figure 3.
3. From power up request (PWDNB↑ or SENB↑ during a write of 1 to bits PDAB, PDIB, and PDRB in Register 2) to RF and IF synthesizers ready (settled to within 0.1 ppm frequency error).
4. Applies to RF PLLS. For RF_1 f_ϕ > 500 kHz settling time is longer.
5. Applies to IF PLL.
6. From power down request (PWDNB↓, or SENB↑ during a write of 0 to bits PDAB, PDIB, and PDRB in Register 2) to supply current equal to I_{PWDN}.

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 4.0	V
Input Current[2]	I_{IN}	±10	mA
Input Voltage[2]	V_{IN}	–0.3 to V_{PD}+0.3	V
Storage Temperature Range	T_{STG}	–55 to 150	°C

Note:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For signals SCLK, SDATA, SENB, PWDNB and XIN.
3. THIS DEVICE IS A HIGH PERFORMANCE RF INTEGRATED CIRCUIT WITH AN ESD RATING OF < 2 kV. HANDLING AND ASSEMBLY OF THIS DEVICE SHOULD ONLY BE DONE AT ESD-PROTECTED WORKSTATIONS.

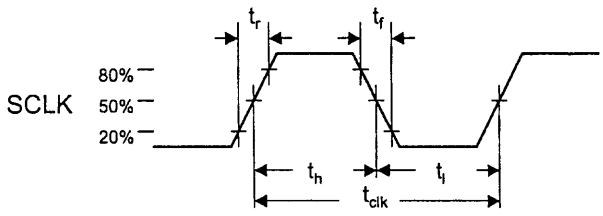


Figure 2. SCLK Timing Diagram

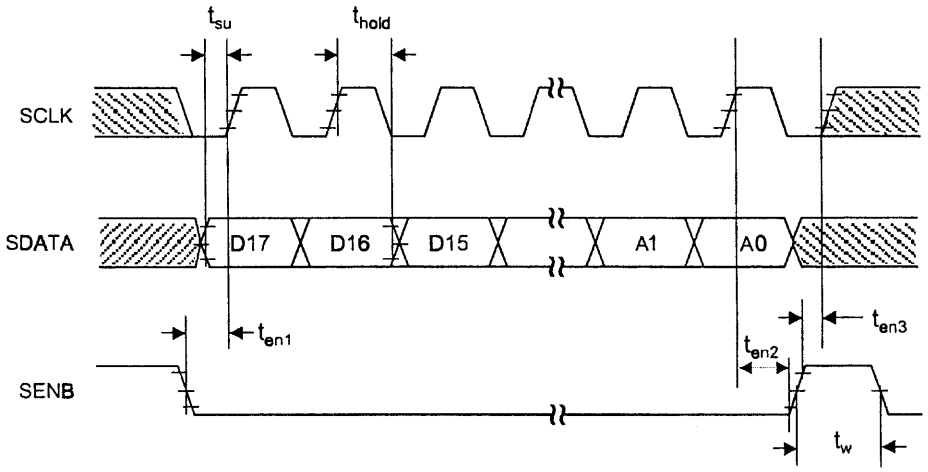


Figure 3. Serial Interface Timing Diagram

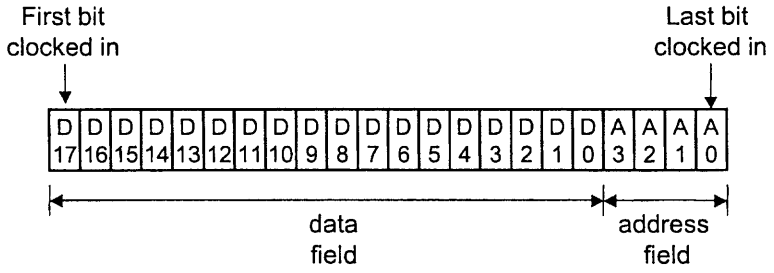


Figure 4. Serial Interface Format

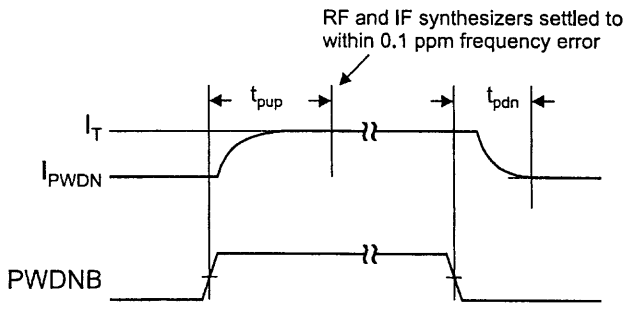


Figure 5. Hardware Power Management Timing Diagram

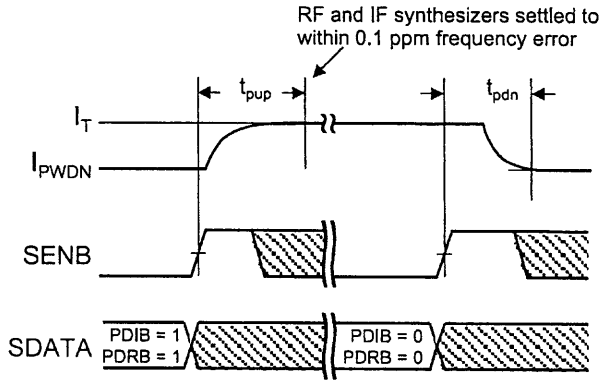


Figure 6. Software Power Management Timing Diagram

Table 5. Reference Amplifier Characteristics
(V_{DD} = 3.0 to 3.6 V, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
XIN Input Frequency	f_{REF}		2	—	20	MHz
Reference Amplifier Sensitivity	V_{REF}		0.5	—	V_{DD} +0.3 V	V_{P-P}

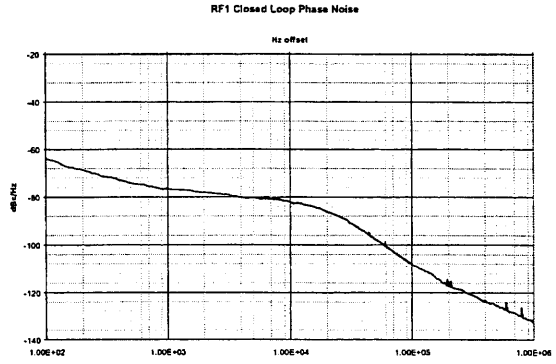
Table 6. RF and IF Synthesizer Characteristics

(V_{DD} = 3.0 to 3.6 V, T_A = –40 to 85°C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Phase Detector Frequency	f_ϕ	$f_\phi = f_{REF}/2R$ for RF_1 and RF_2 Active $f_\phi = f_{REF}/R$ for IF Active	0.010	—	1.0	MHz
RF_{OUT} Tuning Range Limits[2]	f_{RFOUT}	RF_1 Active	2.3	—	2.6	GHz
		RF_2Active	2.0	—	2.4	GHz
IF VCO Center Frequency Range	f_{CEN}		500	—	1000	MHz
IF_{OUT} Center Frequency Range with Divider			62.5	—	1000	MHz
IF Tuning Range from f_{CEN}		Note: L ±10%	–5	—	5	%
RF_1 VCO Pushing		Open loop	—	TBD	—	MHz/V
RF_2 VCO Pushing			—	TBD	—	MHz/V
IF VCO Pushing			—	TBD	—	MHz/V
RF_1 VCO Pulling		VSWR = 2:1, all phases, open loop	—	TBD	—	MHz
RF_2 VCO Pulling			—	TBD	—	MHz
IF VCO Pulling			—	TBD	—	MHz
RF_1 Phase Noise[3]		1 MHz offset	—	–131	—	dBc/Hz
RF_1 Integrated Phase Error[3]		100 Hz to 100 kHz	—	1.5	—	degrees rms
RF_2 Phase Noise[4]		1 MHz offset	—	–131	—	dBc/Hz
RF_2 Integrated Phase Error[4]		100 Hz to 100 kHz	—	1.2	—	degrees rms
IF_{OUT} Phase Noise @ 500 MHz		100 kHz offset	—	–118	—	dBc/Hz
RF_1 Harmonic Suppression[3]		Second Harmonic	—	–28	–20	dBc
RF_2 Harmonic Suppression[4]			—	–23	–20	dBc
IF Harmonic Suppression[5]			—	–26	–20	dBc
RF_1 Output Power Level[3]	P_{ORF1}	Z_L = 50 Ω,	–13	–7	0	dBm
RF_2 Output Power Level[4]	P_{ORF2}	Z_L = 50 Ω	–15	–9	0	dBm
IF Output Power Level[5]	P_{OIF}	Z_L = 50 Ω, 800 MHz	–7	–3	1	dBm
IF Output Voltage Level[5]	V_{OIF}	Z_L = 200 Ω, 200 MHz	0.18	0.25	0.3	V_{RMS}
RF_1 Output Reference Spurs[3]		Offset = 200 kHz	—	–65	—	dBc
		Offset = 400 kHz	—	–70	—	dBc
		Offset = 600 kHz	—	–75	—	dBc
RF_2 Output Reference Spurs[4]		Offset = 200 kHz	—	–65	—	dBc
		Offset = 400 kHz	—	–70	—	dBc
		Offset = 600 kHz	—	–75	—	dBc

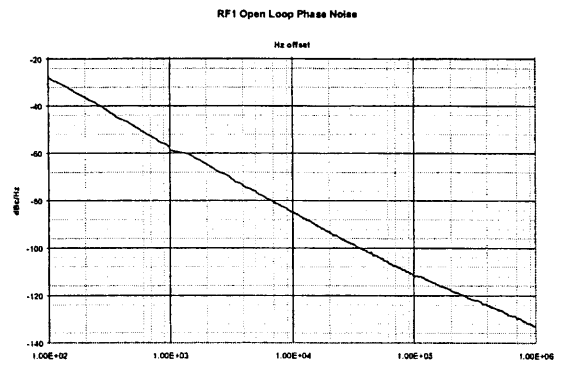
Notes:

1. f_ϕ(RF) = 200 kHz, f_ϕ(IF) = 1 MHz, IF_{OUT} = 0.8 GHz, LPWR = 0, for all parameters unless otherwise noted.
2. RF VCO tuning range limits are fixed by inductance of internally bonded wires.
3. RF_{OUT} = 2.4 GHz.
4. RF_{OUT} = 2.1 GHz.
5. IF_{OUT} = 800 MHz.



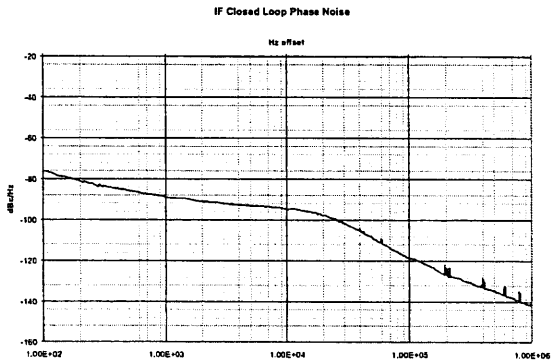
RF1 @ 2400 MHz
f ref = 200 kHz

Figure 7. RF1 Closed Loop Phase Noise



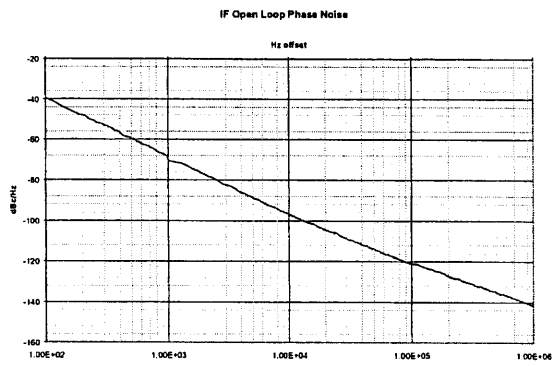
RF1 @ 2400 MHz

Figure 8. RF1 Open Loop Phase Noise



IF @ 550 MHz
f ref = 200 kHz

Figure 9. IF Closed Loop Phase Noise



IF @ 550 MHz

Figure 10. IF Open Loop Phase Noise

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Functional Description

The Si4136 is a monolithic integrated circuit that performs IF and dual-band RF synthesis for wireless communications applications. This integrated circuit (IC), along with two external components, is all that is necessary to implement the frequency synthesis function in wireless communications equipment.

The Si4136 has three complete phase-locked loops (PLLs). They each include integrated voltage-controlled oscillators (VCOs). The low phase noise of the VCOs makes the Si4136 suitable for use in demanding communications applications. Also integrated are phase detectors, loop filters, and reference and output frequency dividers. The IC is programmed through a three-wire serial interface.

One PLL is provided for IF synthesis. The center frequency of this circuit's VCO is set by connection of an external inductance. The PLL can adjust the IF output frequency by ±5% of the VCO center frequency. Inaccuracies in the value of the external inductance are compensated for by the Si4136's proprietary self-tuning algorithm. This algorithm is initiated each time the PLL is powered-up (by either the PWDNB pin or by software) and/or each time a new output frequency is programmed.

Two other PLLs are provided for RF synthesis. These RF PLLs share a common output pin, but only one PLL is active at a given time (as determined by the setting of an internal register). The active PLL is the last one written. The center frequency of the VCO in each PLL is set by the internally bonded inductance. Inaccuracies in these inductances are, again, compensated for by the self-tuning algorithm. The algorithm is run following power-up, following a change in the programmed output frequency.

The RF PLLs contain a divide-by-2 circuit before the N-divider. As a result, the phase detector frequency ($f\phi$) is equal to half the desired channel spacing. For example, for a 200 kHz channel spacing, $f\phi$ would equal 100 kHz. The IF PLL does not contain the divide-by-2 circuit before the N-divider. In this case, $f\phi$ is equal to the desired channel spacing.

Each RF VCO is optimized over a particular frequency range. The RF_1 VCO is optimized to operate from 2.3 GHz to 2.6 GHz, while the RF_2 VCO is optimized to operate between 2.0 GHz and 2.4 GHz. The IF VCO can have its center frequency set as low as 500 MHz and as high as 1000 MHz. An IF output divider is provided to divide down the IF output frequencies, if needed. The divider is programmable, capable of dividing by 1, 2, 4, or 8.

The unique PLL architecture used in the Si4136 produces transient responses that are comparable in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs.

Serial Interface

A timing diagram for the serial interface is shown in Figure 3 on page 7. Figure 4 on page 7 shows the format of the serial interface.

The Si4136 is programmed serially with 22-bit words comprising 18-bit data fields and 4-bit address fields. When the serial interface is enabled (i.e., when SENB is low) data and address bits on the SDATA pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of SENB into the internal data register addressed in the address field. The serial interface is disabled when SENB is high.

Table 12 on page 18 summarizes the data register functions and addresses. It is not necessary (although it is permissible) to clock into the internal shift register any leading bits that are "don't cares."

Setting the VCO Center Frequencies

The IF PLL can tune ±5% from the center frequency of the VCO. The IF center frequency is established by the value of an external inductance connected to the VCO. Please note, the RF center frequency is set by an internal inductance and cannot be changed. The RF_1 and RF_2 PLLS have fixed operating ranges due to the inductance set by the internally bonded wires. Each center frequency is established by the value of the total inductance (internal and/or external) connected to the respective VCO. Manufacturing tolerance of ±10% for the external inductance is acceptable for the IF VCO. The Si4136 will compensate for inaccuracies in each inductance by executing a self-tuning algorithm following PLL power-up or following a change in the programmed output frequency.

Because the tank inductance is in the low nH range, the inductance of the package needs to be considered in determining the correct external inductance. The total inductance (L_{TOT}) presented to the IF VCO is the sum of the external inductance (L_{EXT}) and the package inductance (L_{PKG}). The IF VCO has a nominal capacitance (C_{NOM}) in parallel with the total inductance, and the center frequency is as follows:

$$f_{CEN} = \frac{1}{2\pi\sqrt{L_{TOT} \cdot C_{NOM}}}$$

$$= \frac{1}{2\pi\sqrt{(L_{PKG} + L_{EXT}) \cdot C_{NOM}}}$$

Table 7 summarizes the characteristics of the IF VCO.

Table 7. VCO Characteristics

VCO	Inductor Pins	Center Frequency Range (MHz)	Cnom (pF)	Lpkg (nH)	Lext Range (nH)
IF	IFLA, B	500–1000	6.0	2.8	14.1–1.4

As a design example, suppose it is desired to synthesize frequencies in a 30 MHz band between 735 MHz and 765 MHz. The center frequency should be defined as midway between the two extremes, or 750 MHz. The PLL will be able to adjust the VCO output frequency ±5% of the center frequency, or ±37.5 MHz of 750 MHz (i.e., from approximately 713 MHz to 788 MHz, more than enough for this example). The IF VCO has a C_{NOM} of 6.0 pF, and a 7.5 nH inductance (correct to two digits) in parallel with this capacitance will yield the desired center frequency. An external inductance of 4.7 nH should be connected between IFLA and IFLB, as shown in Figure 14 on page 16. This, in addition to 2.8 nH of package inductance, will present the correct total inductance to the VCO. In manufacturing, the external inductance can vary ±10% of its nominal value and the Si4136 will correct for the variation with the self-tuning algorithm.

In most cases, the requisite value of the external inductance is small enough to allow a PC board trace to be utilized. During initial board layout, a length of trace approximating the desired inductance can be used. Data read from an Si4136 register following self-tuning can be used as a design guide in determining the actual inductance represented by the trace. Also, this data can be used in production for self-testing. Use of this feature is detailed in an appendix at the end of this data sheet.

Self-Tuning Algorithm

The self-tuning algorithm is initiated immediately following power-up of a PLL or, if the PLL is already powered, following a change in its programmed output frequency. This algorithm attempts to tune the VCO so that its free-running frequency is near the desired output frequency. In so doing, the algorithm will compensate for manufacturing tolerance errors in the value of the external inductance connected to the IF VCO. It will also reduce the frequency error for which the PLL must correct to get the precise desired output frequency. The self-tuning algorithm will leave the VCO oscillating at a frequency in error by somewhat less than 1% of the desired output frequency.

After self-tuning, the VCO oscillation frequency is controlled by the PLL. The PLL will complete frequency locking, eliminating any remaining frequency error. Thereafter, it will maintain frequency-lock, compensating for effects caused by temperature and supply voltage variations.

The Si4136's self-tuning algorithm will compensate for component value errors at any temperature within the specified temperature range. However, the ability of the PLL to compensate for drift in component values that occur AFTER self-tuning is limited. For external inductances with temperature coefficients around ±150 ppm/degree C, the PLL will be able to maintain lock for changes in temperature of approximately ±30 °C.

In applications where the PLL is regularly powered-down or the frequency is periodically programmed this limitation is of no concern since the VCO is re-tuned when it is powered up. In applications where the ambient temperature can drift substantially after self-tuning, it may be necessary to monitor the lock-detect bar (LDETB) signal on the AUXOUT pin for an indication that a PLL is about to run out of locking capability (see the AUXILIARY OUTPUT section below for how to select LDETB). The LDETB signal is normally low after self-tuning is completed but will rise when either the IF or RF PLL nears the limit of its compensation range (LDETB will also be high when either PLL is executing the self-tuning algorithm). The output frequency will still be locked when LDETB goes high, but the PLL will eventually lose lock if the temperature continues to change in the same direction. Therefore, if LDETB goes high both the IF and RF PLLs should promptly be re-tuned by initiating the self-tuning algorithm.

Output Frequencies

The IF and RF output frequencies are set by programming the R- and N-Divider registers. Each PLL has its own R and N registers so that each can be programmed independently. Programming either the R- or N-Divider register for RF1 or RF2 automatically selects the associated output.

The reference frequency on the XIN pin is divided by R and this signal is input to the PLL's phase detector. The other input to the phase detector is the PLL's VCO output frequency divided by 2N for the RF PLLs or N for the IF PLL. The PLL acts to make these frequencies

equal. That is, after an initial transient

$$f_{OUT}/2N = f_{REF}/R \text{ (for the RF PLLs)}$$

and

$$f_{OUT}/N = f_{REF}/R \text{ (for the IF PLL)}$$

consequently,

$$f_{OUT} = (2N/R)*f_{REF} \text{ (for the RF PLLs)}$$

$$f_{OUT} = (N/R)*f_{REF} \text{ (for the IF PLL)}$$

The integers R are set by programing the RF_1 R-Divider register (register 6), the RF_2 R-Divider register (register 7) and the IF R-Divider register (register 8).

The integers N are set by programing the RF_1 N-Divider register (register 3), the RF_2 N-Divider register (register 4), and the IF N-Divider register (register 5).

Each N-Divider is implemented as a conventional high speed divider. That is, it consists of a dual-modulus prescaler, a swallow counter, and a lower speed synchronous counter.

PLL Loop Dynamics

The transient response for each PLL is determined by its phase detector update rate f_ϕ (equal to f_{REF}/R) and the phase detector gain programmed for each RF_1, RF_2, or IF synthesizer (see register 1). Four different settings for the phase detector gain are available for each PLL. The highest gain is programmed by setting the two phase detector gain bits to 00, and the lowest by setting the bits to 11. The values of the available gains, relative to the highest gain, are listed in Table 8.

Table 8. Gain Values (Register 1)

K_P Bits	Relative P.D. Gain
00	1
01	1/2
10	1/4
11	1/8

In general, a higher phase detector gain will decrease in-band phase noise and increase the speed of the PLL transient until the point at which stability begins to be compromised. The optimal gain depends on N. Table 9 lists recommended settings for different values of N.

Table 9. Optimal K_P Settings

N	RF_1 K_{P1}<1:0>	RF_2 K_{P2}<1:0>	IF K_{PI}<1:0>
≤2047	00	00	00
2048 to 4095	00	01	01
4096 to 8191	01	10	10
8192 to 16383	10	11	11
≥16384	11	11	11

The VCO gain and loop filter characteristics are not programmable.

The settling time for each PLL is directly proportional to its phase detector update period T_ϕ (T_ϕ equals $1/f_\phi$). During the first 13 update periods the Si4136 executes the self-tuning algorithm. Thereafter the PLL controls the output frequency. Because of the unique architecture of the Si4136 PLLs, the time required to settle the output frequency to 0.1 ppm error is only about 25 update periods. Thus, the total time after power-up or a change in programmed frequency until the synthesized frequency is well settled—including time for self-tuning—is around 40 update periods.

Note: This settling time analysis holds for RF_1 $f_\phi \leq 500$ kHz. For RF_1 $f_\phi > 500$ kHz, the settling time is larger.

RF and IF Outputs (RF_{OUT} and IF_{OUT})

The RF_{OUT} and IF_{OUT} pins are driven by amplifiers that buffer the RF VCOs and IF VCO, respectively. The RF output amplifier receives its input from either the RF_1 or RF_2 VCO, depending upon which R- or N-Divider register was last written. For example, programming the N-Divider register for RF_1 automatically selects the RF_1 VCO output.

Figure 16 on page 17 shows an application diagram for the Si4136. The RF output signal must be coupled to its load through an AC coupling capacitor. The matching network is made to provide an adequate match to an external 50 Ω load for both the RF_1 and RF_2 frequency bands. The matching network also filters the output signal to reduce harmonic distortion.

The IF_{OUT} pin must also be coupled to its load through an AC coupling capacitor. The IF output level is dependent upon the load. Figure 13 on page 15 displays the output level versus load resistance for a variety of output frequencies. For resistive loads greater than 500 Ω the output level saturates and the bias currents in the IF output amplifier are higher than they need be. The LPWR bit in the Main Configuration

register (register 0) can be set to 1 to reduce the bias currents and therefore reduce the power dissipated by the IF amplifier. For loads less than 500 Ω LPWR should be set to 0 to maximize the output level.

For IF frequencies greater than 500 MHz, a matching network is required in order to drive a 50 Ω load. See Figure 11 below.

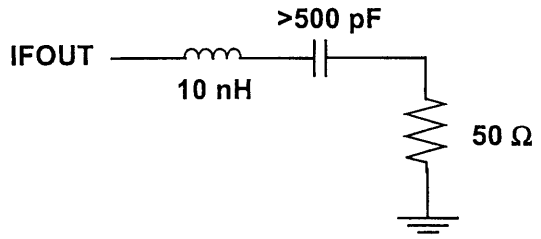


Figure 11. IF Frequencies > 500 MHz

For frequencies less than 500 MHz, the IF output buffer can directly drive a 200 Ω resistive load or higher. For resistive loads greater than 500 Ω (f < 500 MHz) the LPWR bit can be set to reduce the power consumed by the IF output buffer. See Figure 12 below.

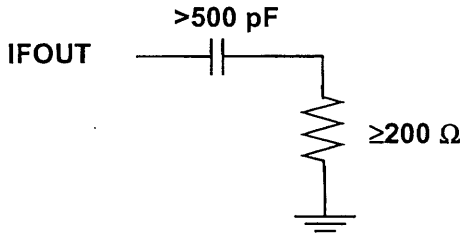


Figure 12. IF Frequencies < 500 MHz

Reference Frequency Amplifier

The Si4136 provides a reference frequency amplifier. If the driving signal has CMOS levels it can be connected directly to the XIN pin. Otherwise, the reference frequency signal should be AC coupled to the XIN pin through a 100 pF capacitor.

Power Down Modes

Table 10 summarizes the power down functionality. The Si4136 can be powered down by taking the PWDNB pin low or by setting bits in the Power Down register (register 2). When the PWDNB pin is low, the Si4136 will be powered down regardless of the Power Down register settings. When the PWDNB pin is high, power management is under control of the Power Down register bits.

It may be desirable to defeat power down of the reference frequency amplifier. In such a case the XPDM (XTAL Power Down Mode) bit in the Main Configuration register (register 0) should be set to 1. The reference frequency amplifier will then remain powered up even when the PWDNB pin is asserted (i.e., low), excepting when all three of the Power Down Register bits (PDAB, PDIB, and PDRB) are low. This exception exists so that, even in this mode, the reference amplifier can be forced to power down if sufficient time occurs for a power down and power up sequence. Alternatively, of course, the reference amplifier power down defeat mode can be exited by setting XPDM to 0.

With the PWDNB pin high, the XPDM bit has no effect. The reference frequency amplifier, IF, and RF sections of the Si4136 circuitry can be individually powered down by setting the Power Down register bits PDAB, PDIB, and PDRB low, respectively. Note that the reference frequency amplifier will also be powered up if either the PDRB and PDIB bits are high, even if the PDAB bit is low. Also, setting the AUTOPDB bit to 1 in the Main Configuration register (register 0) is equivalent to setting all three of the bits in the Power Down register to 1.

The serial interface remains available and can be written to in all power down modes.

Auxiliary Output (AUXOUT)

The AUXOUT pin can be used to monitor a variety of signals. The signal appearing on AUXOUT is selected by setting the AUXSEL bits in the Main Configuration Register (Register 0). The possible outputs are listed in the description of the Main Configuration Register.

Some of these signals may only be useful for evaluation purposes (in particular, the PLL R- and N-Divider outputs). Two signals, though, have more general use. The first is the LDETB signal, which can be selected by setting the AUXSEL bits to 011. As discussed above, this signal can be used to indicate that the IF or RF PLL is about to lose lock due to excessive ambient temperature drift and should be re-tuned. The second is the Reference Clock output. This is a buffered version of the signal on the XIN pin, with the exception that it will be held low when the reference frequency amplifier is powered down.

Table 10. Power Down Configuration

PWDNB Pin	XPDM	AUTOPDB	PDAB	PDIB	PDRB	Reference Frequency Amplifier	IF Circuitry	RF Circuitry
PWDNB = 0	0	Don't Care				OFF	OFF	OFF
	1	Any High				ON	OFF	OFF
	1	0	0	0	0	OFF	OFF	OFF
PWDNB = 1	x	0	0	0	0	OFF	OFF	OFF
	x	0	x	0	1	ON	OFF	ON
	x	0	x	1	0	ON	ON	OFF
	x	0	x	1	1	ON	ON	ON
	x	0	1	0	0	ON	OFF	OFF
	x	1	x	x	x	ON	ON	ON

Note: The XPDM bit has no effect when the PWDNB pin is high.

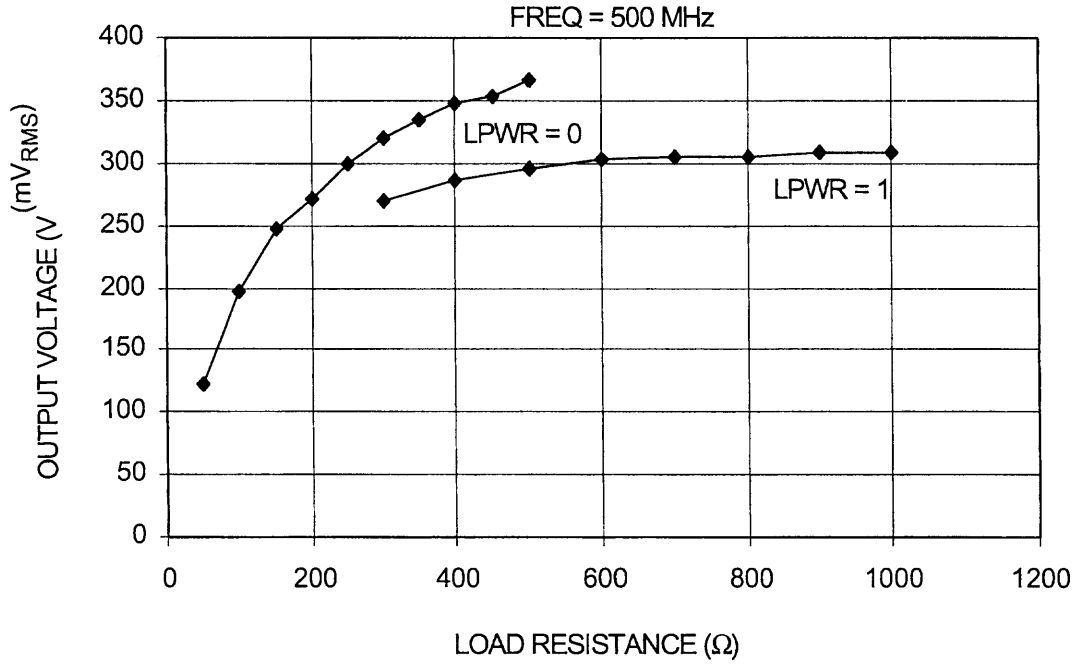


Figure 13. IF Output Voltage vs. Load Resistance

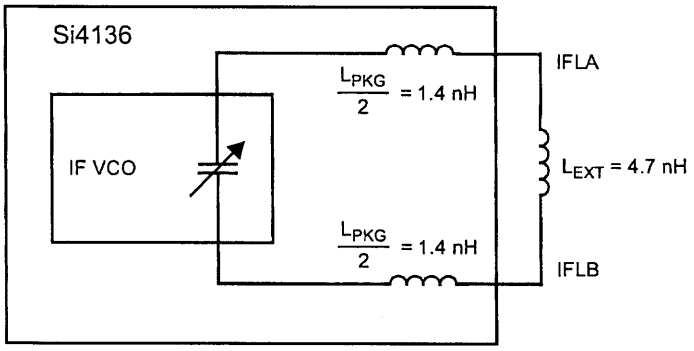


Figure 14. Example of IF External Inductor

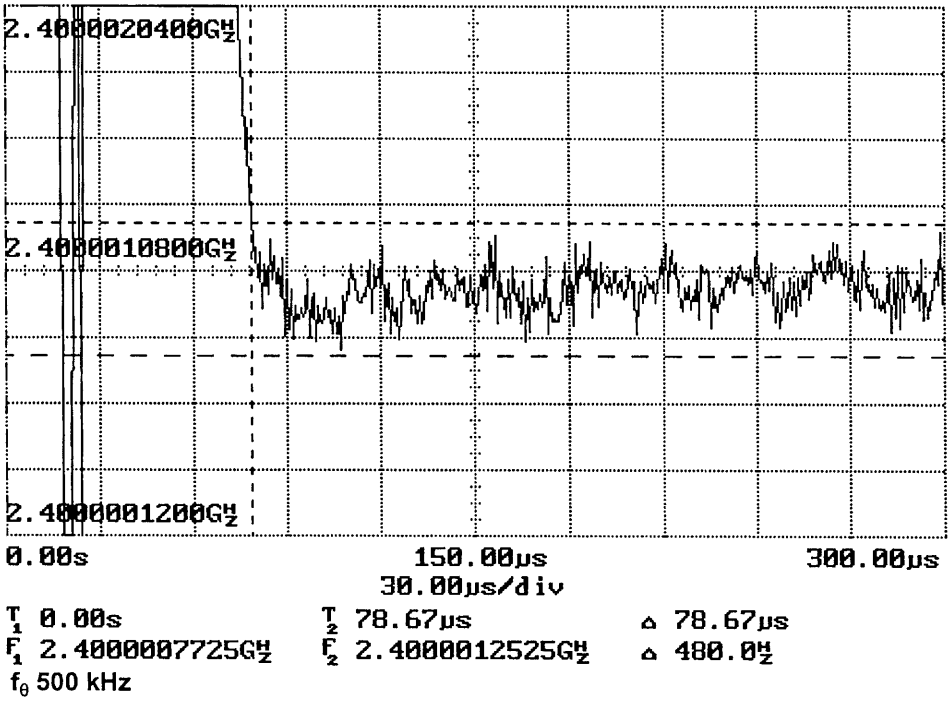


Figure 15. Typical Transient Response

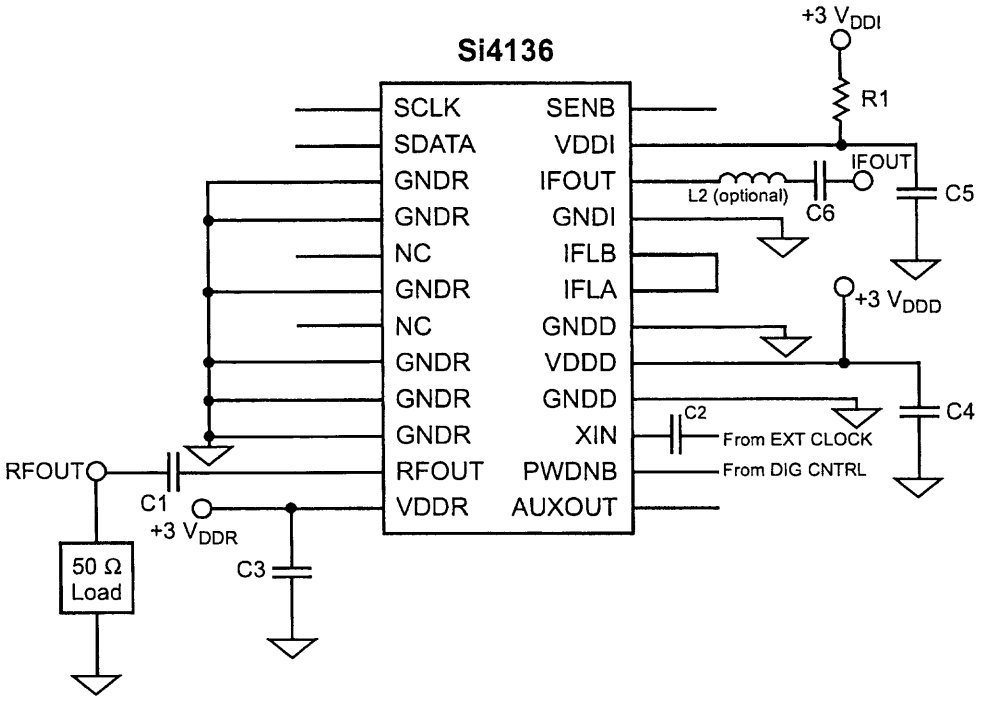


Figure 16. Application Diagram

Table 11. Typical Component Values

Symbol	Value
C1	>470 pF
C2	100 pF
C3, C4, C5	22 nF
C6	>560 pF
L2[1]	40 nH
R1[2]	25 Ω

Notes:
1. Only needed for IFOUT frequency >500 MHz.
2. Required for IF VCO frequency <600 MHz and IFDIV ≠ 00.

Control Registers

Table 12. Register Summary

Register	Name	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Main Configuration	X	X	X	AUXSEL			IFDIV		0	0	0	0	LPWR	XPDM	AUTO PDB	0	0	0
1	Phase Detector Gain	X	X	X	X	X	X	X	X	X	X	X	X	K_{PI}		K_{P2}		K_{P1}	
2	Power Down	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PDAB	PDIB	PDRB
3	RF_1 N Divider	N_{RF1}																	
4	RF_2 N Divider	X	N_{RF2}																
5	IF N Divider	X	X	N_{IF}															
6	RF_1 R Divider	X	X	X	X	X	R_{RF1}												
7	RF_2 R Divider	X	X	X	X	X	R_{RF2}												
8	IF R Divider	X	X	X	X	X	R_{IF}												
9	Reserved																		
. . .																			
15	Reserved																		

Note: X = Don't Care. Registers 9–15 are reserved. Writes to these registers may result in unpredictable behavior.

Register 0. Main Configuration Address Field = A[3:0] = 0000

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	AUXSEL			IFDIV		0	0	0	0	LPWR	XPDM	AUTO PDB	0	0	0

Bit	Name	Function
17:15	Reserved	Don't care.
14:12	AUXSEL	**Auxiliary Output Pin Definition.** 000 = TEST—Reserved. 001 = TEST—Force output low. 010 = TEST—CMOS level of f_{REF}. 011 = TEST—Lock Detect - LDETB. 100 = TEST—CMOS level of $f_{\phi R}$ of active RF synthesizer. 101 = TEST—CMOS level of $f_{\phi R}$ of IF synthesizer. 110 = TEST—CMOS level of $f_{\phi N}$ of active RF synthesizer. 111 = TEST—CMOS level of $f_{\phi N}$ of IF synthesizer.
11:10	IFDIV	**IF Output Divider** 00 = IF_{OUT} = IFVCO Frequency 01 = IF_{OUT}= IFVCO Frequency/2 10 = IF_{OUT} = IFVCO Frequency/4 11 = IF_{OUT} = IFVCO Frequency/8
9:6	Reserved	Program to zero.
5	LPWR	**Output Power-Level Settings for IF Synthesizer Circuit.** 0 = R_{LOAD} < 500 Ω—normal power mode. 1 = R_{LOAD} ≥ 500 Ω—low power mode.
4	XPDM	**Reference Amplifier Power-Down Mode.** 0 = Reference amplifier powered down when PWDNB pin = 0 or AUTOPDB, PDAB, PDIB, and PDRB bits are set to 0. 1 = Reference amplifier on when PWDNB pin = 0.
3	AUTOPDB	**Auto Power Down** 0 = Software powerdown is controlled by Register 2. 1 = Equivalent to setting all bits in Register 2 = 1.
2:0	Reserved	Program to zero.

Register 1. Phase Detector Gain Address Field (A[3:0]) = 0001

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	X	X	X	X	X	X	X	X	X	K_{PI}		K_{P2}		K_{P1}	

Bit	Name	Function
17:6	Reserved	Don't care.
5:4	K_{PI}	**IF Phase Detector Gain Constant.*** N Value K_{PI} <2048 = 00 2048–4095 = 01 4096–8191 = 10 >8191 = 11
3:2	K_{P2}	**RF_2 Phase Detector Gain Constant.*** N Value K_{P2} <2048 = 00 2048–4095 = 01 4096–8191 = 10 >8191 = 11
1:0	K_{P1}	**RF_1 Phase Detector Gain Constant.*** N Value K_{P1} <4096 = 00 4096–8191 = 01 8192–16383 = 10 >16383 = 11

Register 2. Power Down Address Field (A[3:0]) = 0010

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PDAB	PDIB	PDRB

Bit	Name	Function
17:3	Reserved	Don't care.
2	PDAB	**Power Down Reference Amplifier.** 0 = Reference amplifier powered down when PDIB and PDRB = 0. 1 = Reference amplifier on. **Note:** Enabling any PLL with PDIB or PDRB will automatically power on the reference amplifier regardless of PDAB.
1	PDIB	**Power Down IF Synthesizer.** 0 = IF synthesizer powered down. 1 = IF synthesizer on.
0	PDRB	**Power Down RF Synthesizer.** 0 = RF synthesizer powered down. 1 = RF synthesizer on.

Register 3. RF_1 N Divider Address Field (A[3:0]) = 0011

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_{RF1}																	

Bit	Name	Function
17:0	N_{RF1}	**N Divider for RF_1 Synthesizer.** N_{RF1} must ≥ 992.

Register 4. RF_2 N Divider Address Field = A[3:0] = 0100

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	N_{RF2}																

Bit	Name	Function
17	Reserved	Don't care.
16:0	N_{RF2}	**N Divider for RF_2 Synthesizer.** N_{RF2} must ≥ 240.

Register 5. IF N Divider Address Field (A[3:0]) = 0101

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	N_{IF}															

Bit	Name	Function
17:16	Reserved	Don't care.
15:0	N_{IF}	**N Divider for IF Synthesizer.** N_{IF} must ≥ 56.

Register 6. RF_1 R Divider Address Field (A[3:0]) = 0110

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	X	X	R_{RF1}												

	Name	Function
17:13	Reserved	Don't care.
12:0	R_{RF1}	**R Divider for RF_1 Synthesizer.** R_{RF1} can be any value from 7 to 8189 if K_{P1} = 00 8 to 8189 if K_{P1} = 01 10 to 8189 if K_{P1} = 10 14 to 8189 if K_{P1} = 11

Register 7. RF_2 R Divider Address Field (A[3:0]) = 0111

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	X	X	R_{RF2}												

Bit	Name	Function
17:13	Reserved	Don't care.
12:0	R_{RF2}	**R Divider for RF_2 Synthesizer.** R_{RF2} can be any value from 7 to 8189 if K_{P2} = 00 8 to 8189 if K_{P2} = 01 10 to 8189 if K_{P2} = 10 14 to 8189 if K_{P2} = 11

Register 8. IF R Divider Address Field (A[3:0]) = 1000

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	X	X	R_{IF}												

Bit	Name	Function
17:13	Reserved	Don't care.
12:0	R_{IF}	**R Divider for IF Synthesizer.** R_{IF} can be any value from 7 to 8189 if K_{P1} = 00 8 to 8189 if K_{P1} = 01 10 to 8189 if K_{P1} = 10 14 to 8189 if K_{P1} = 11

APPENDIX—EVALUATING SELF-TUNING RESULTS

Introduction

The center frequency of the IF VCO is set by the value of an external inductance. The self-tuning algorithm will compensate for manufacturing tolerance errors in the value of the inductance, but it is important to design the nominal value of the inductance so as to maximize the compensation range of the Si4136. It also may be useful during production to check the margin available to the algorithm for individual units as part of a self-test strategy. It is possible to read the results of self-tuning after the self-tuning algorithm has run for use as an aid in these analyses.

Internal registers contain the results of the self-tuning algorithm. There is a separate register for each PLL. Figure 17 illustrates how the contents of these registers can be read using the serial interface and the AUXOUT pin. Writing the 22-bit word '0001DE'H to the serial interface will enable access to the IF results. Subsequent to SENB rising—which disables the serial input—data in the accessed register is loaded into an internal output shift register on the next rising edge of the SCLK pin. The data will then be clocked out on the AUXOUT pin by falling edges of SCLK.

Each output word is 18 bits long. The first 7 bits are all 0, and the next 11 bits are the binary digits of a number representing the self-tuning result, with the most significant bit (MSB) being first out and the least significant bit (LSB) being last out. Interpretation of the results is discussed below.

Reading the self-tuning results from AUXOUT suspends any other use of this pin selected by the AUXSEL bits in the Main Configuration register (register 0). The original functionality for AUXOUT will be restored following a write through the serial interface to any internal register.

Designing External Inductances

To use this feature to help optimize the design of the external inductance, the Si4136 should be programmed to synthesize a variety of test frequencies near the application's center frequency. Five different frequencies equally distributed between the maximum and minimum frequencies to be synthesized is an acceptable variety. Choose frequencies within ±2% of the IF.

For each test frequency, the self-tuning algorithm will be initiated immediately upon programming a new N or R value if the PLL is powered up. If the PLL is powered down, the algorithm will be initiated following power-up. After completion of the algorithm, the result can be read from the AUXOUT pin, as described above.

Each 11 bit result will be in the range of '000'H to '7FF'H. The arithmetic average of all results for the PLL under study should be in the middle of this range. An average that is higher indicates that the external inductance is too small, and, conversely, a lower average indicates that it is too large. An average between '380'H and '480'H indicates that the design of the external inductance is acceptably accurate as a nominal design, at least for use with the Si4136 unit under test. Repeated tests with the same inductance but with other Si4136 units can then be run to insure that the design is well centered.

Production Self-Test

In production, the combination of actual external inductance, the characteristics of the particular Si4136 unit, and the maximum and minimum frequencies to be synthesized will lead to variability in the self-tuning results. A check for margin in the self-tuning capability of the IF PLL can be made at room temperature to insure that enough range remains to compensate for temperature drift mechanisms (compensation range necessary for supply voltage variations is much less than that necessary for temperature variations). Checks should be made at both the maximum and minimum frequency. After programming the maximum frequency to be synthesized, the 11-bit result should be greater than '040'H. After programming the minimum frequency to be synthesized, the 11-bit result should be less than '780'H. (These limits assume an external inductance temperature coefficient within ±150 ppm/°C.)

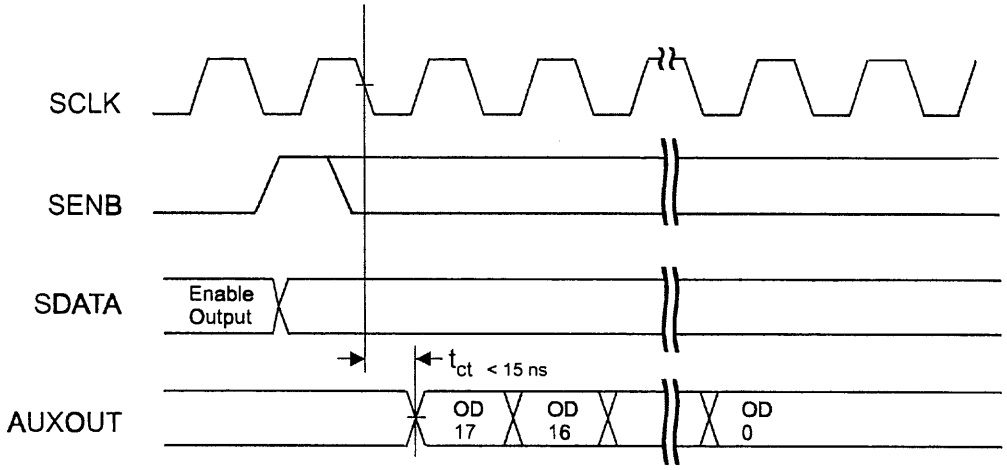
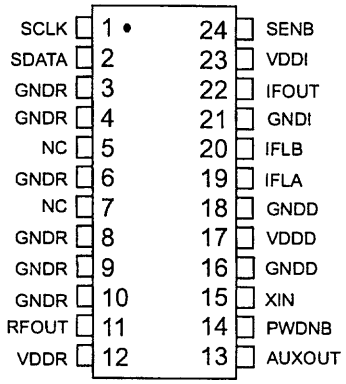


Figure 17. AUXOUT Timing Diagram

Pin Descriptions—Si4136

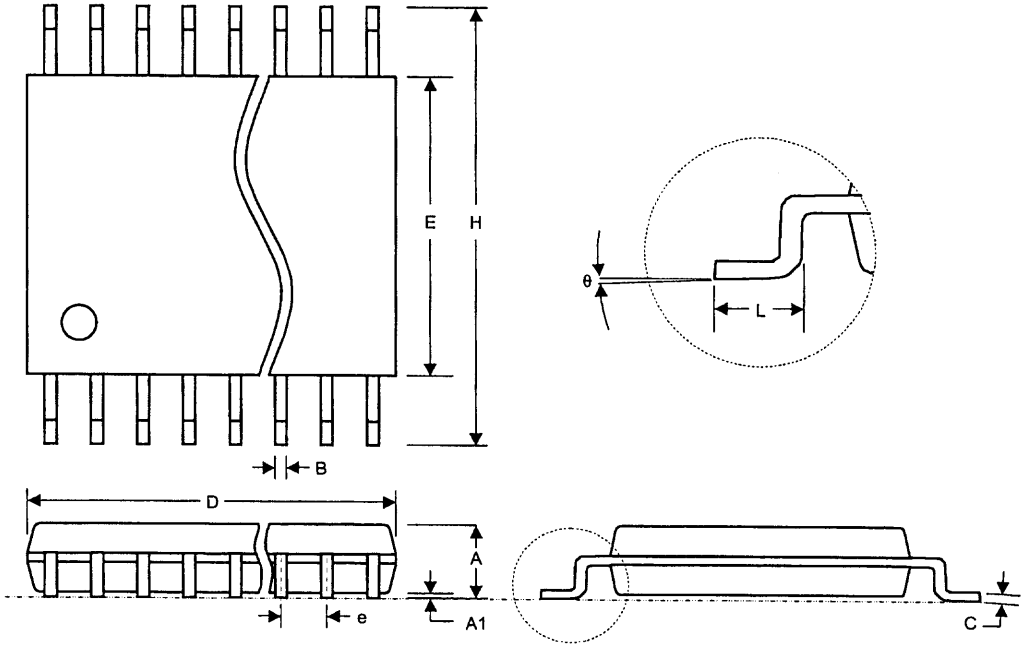


AUXOUT	Auxiliary Output
GNDD	Common Ground for digital circuitry
GNDI	Common Ground for IF analog circuitry
GNDR	Common Ground for RF analog circuitry
IFLA	Pin for inductor connection to IF VCO
IFLB	Pin for inductor connection to IF VCO
IFOUT	Intermediate frequency (IF) output of the IF VCO
NC	No Connection
PWDNB	Power Down Pin
RFOUT	Radio frequency (RF) output of the selected RF VCO
SCLK	Serial Clock
SDATA	Serial Data
SENB	Enable Serial Port
VDDD	Supply voltage for digital circuitry
VDDI	Supply voltage for IF analog circuitry
VDDR	Supply voltage for RF analog circuitry
XIN	Reference Frequency Amplifier Input

Ordering Guide

Ordering Part Number	Description	Temperature
Si4136-BT	2.6 GHz/2.4 GHz/IF OUT	–40 to 85°C

Package Outline



24-pin Thin Shrink Small Outline Package (TSSOP)

Package Diagram Dimensions

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	—	0.047	—	1.1
A1	0.002	0.006	0.05	0.15
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.303	0.311	7.70	7.90
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.018	0.030	0.45	0.75
θ	0°	8°	0°	8°

NOTES:

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Contact Information

Silicon Laboratories Inc.

4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: productinfo@silabs.com
Internet: www.silabs.com

SILICON LABORATORIES