Panasonic

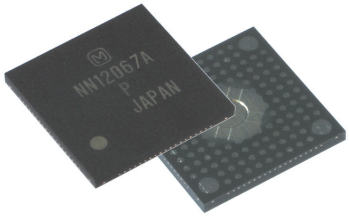
Product News

将CCD外围电路单片封装

用于CCD照相机的模拟前端处理IC NN12067A

■ 概 要

NN12067A型IC，内置定时信号产生器和垂直驱动器(对应本公司CCD)，用于CCD照相机的模拟前端处理(CDS、GCA、A/D转换器)。通过内置专用定时信号产生器和垂直驱动器，可以缩短CCD照相机的开发设计时间，并可以节省空间。



MLGA107-L2-0909

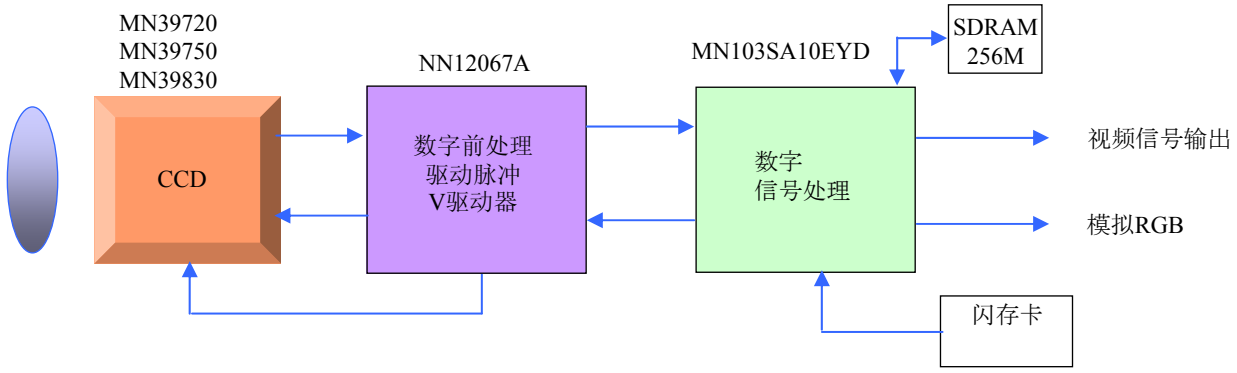
■ 特 长

- GCA的增益范围极宽：-2dB ～ 34dB
- 与本公司历来产品相比，信噪比提高了5dB
- 附带水平驱动器
- 附带频闪同步脉冲输出
- 具备电子变焦功能、电子快门功能
- 内置17条通道的垂直驱动器和1条通道的SUB驱动器
- 内置SSG
- 最大驱动频率:36MHz
- 主时钟:可以设定为fck/2fck
- TG:半可编程
- 采用小型LLGA封装

■ 用 途

CCD照相机(数码相机、手机照相机等)

■系统框图



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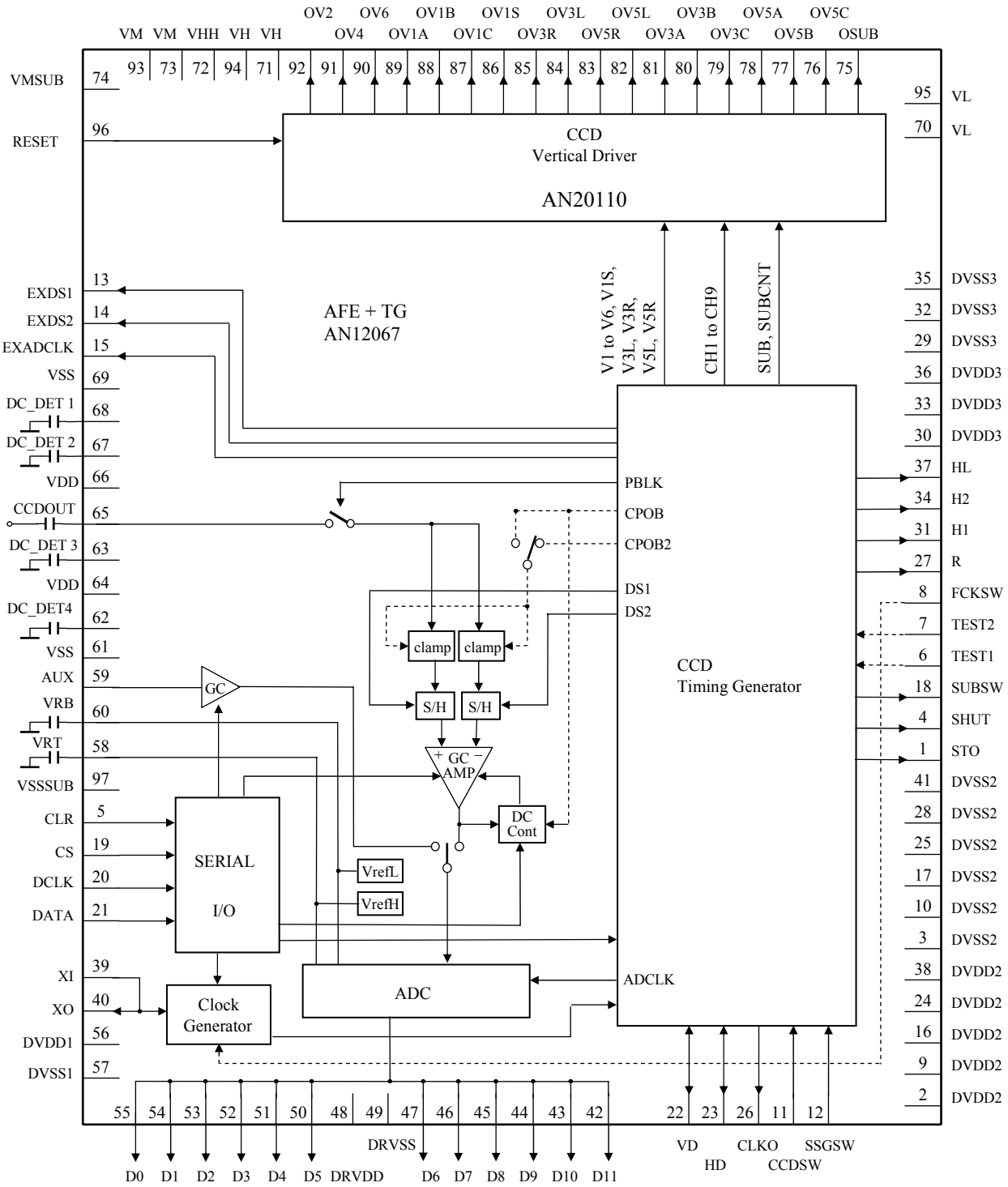
■ Block Diagram



■ Pin Arrangement (Top View)

TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N
13	97		52	49	87	84	46	43	82	79	39	97	
12			53	50	88	85	45	42	81	41	38		
11	90	89	51	48	86	47	44	83	80	40	76	78	77
10	54	92	91	⊠	⊠				⊠	⊠	73	75	74
9	93	56	55	⊠						⊠	36	37	72
8	94	58	57								33	35	34
7	95	60	59								71	31	32
6	62	63	61								70	29	30
5	65	66	64	⊠						⊠	26	27	28
4	68	69	67	⊠	⊠				⊠	⊠	N.C.	25	24
3	96	N.C.	N.C.	2	5	8	11	14	16	19	21	N.C.	N.C.
2	97		1	4	7	10	12	15	18	N.C.	23	97	
1				3	6	9	13	N.C.	17	20	22		

TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N
13	VSSSUB		D3	DRVSS	OV1C	OV3L	D7	D10	OV5L	OV3C	XI	VSSSUB	
12			D2	D5	OV1B	OV3R	D8	D11	OV3A	DVSS2	DVDD2		
11	OV6	OV1A	D4	DRVDD	OV1S	D6	D9	OV5R	OV3B	XO	OV5C	OV5A	OV5B
10	D1	OV2	OV4	⊠	⊠				⊠	⊠	VM	OSUB	VMSUB
9	VM	DVDD1	D0	⊠						⊠	DVDD3	HL	VHH
8	VH	VRT	DVSS1								DVDD3	DVSS3	H2
7	VL	VRB	AUX								VH	H1	DVSS3
6	DC_DET4	DC_DET3	VSS								VL	DVSS3	DVDD3
5	CCDOUT	VDD	VDD	⊠						⊠	CLKO	R	DVSS2
4	DC_DET1	VSS	DC_DET2	⊠	⊠				⊠	⊠	N.C.	DVSS2	DVDD2
3	RESET	N.C.	N.C.	DVDD2	CLR	FCKSW	CCDSW	EXDS2	DVDD2	CS	DATA	N.C.	N.C.
2	VSSSUB		STO	SHUT	TEST2	DVSS2	SSGSW	EXADCLK	SUBSW	N.C.	HD	VSSSUB	
1				DVSS2	TEST1	DVDD2	EXDS1	N.C.	DVSS2	DCLK	VD		

⊠ Thermal / dummy land　　□ No land　　N.C. Land without wire connection

The direction recognition mark corresponds to the direction of A1 land

NN12067A
XXXXX
JAPAN

■ Pin Descriptions1

No.	Pin name	Pin	Type	Description
1	STO	C2	I/O	Strobe trigger output
2	DV_{DD2}	D3	—	Power supply for timing generator block
3	DV_{SS2}	D1	—	Ground for timing generator block
4	SHUT	D2	Output	Mechanical shutter control pulse
5	CLR	E3	Input	All clear input
6	TEST1	E1	Input	Test input 1 (Normally set low)
7	TEST2	E2	Input	Test input 2 (Normally set low)
8	FCKSW	F3	Input	Master clock setting input
9	DV_{DD2}	F1	—	Power supply for timing generator block
10	DV_{SS2}	F2	—	Ground for timing generator block
11	CCDSW	G3	Input	CCD setting input
12	SSGSW	G2	Input	SSG setting input
13	EXDS1	G1	I/O	Pre-charge S/H pulse output
14	EXDS2	H3	I/O	Data S/H pulse output
15	EXADCLK	H2	I/O	A/D clock output
16	DV_{DD2}	J3	—	Power supply for timing generator block
17	DV_{SS2}	J1	—	Ground for timing generator block
18	SUBSW	J2	I/O	SUB bias voltage control pulse output
19	CS	K3	Input	Data latch input for serial data communications
20	DCLK	K1	Input	Clock input for serial data communications
21	DATA	L3	Input	Data input for serial data communications
22	VD	L1	I/O	Vertical sync pulse input/output
23	HD	L2	I/O	Horizontal sync pulse input/output
24	DV_{DD2}	N4	—	Power supply for timing generator block
25	DV_{SS2}	M4	—	Ground for timing generator block
26	CLKO	L5	Output	FCK clock output
27	R	M5	Output	fR pulse output (positive logic)
28	DV_{SS2}	N5	—	Ground for timing generator block
29	DV_{SS3}	M6	—	Ground for fH driver and fR driver
30	DV_{DD3}	N6	—	Power supply for fH driver and fR driver
31	H1	M7	Output	fH1 pulse output (positive logic)
32	DV_{SS3}	N7	—	Ground for fH driver and fR driver
33	DV_{DD3}	L8	—	Power supply for fH driver and fR driver
34	H2	N8	Output	fH2 pulse output (positive logic)

■ Pin Descriptions2

No.	Pin name	Pin	Type	Description
35	DV_{SS3}	M8	—	Ground for fH driver and fR driver
36	DV_{DD3}	L9	—	Power supply for fH driver and fR driver
37	HL	M9	Output	fHL pulse output (positive logic)
38	DV_{DD2}	L12	—	Power supply for timing generator block
39	XI	L13	Input	Crystal oscillator input (FCK or 2FCK)
40	XO	K11	Output	Crystal oscillator output (FCK/2FCK) with 3 times multiplier and external feedback resistor
41	DV_{SS2}	K12	—	Ground for timing generator block
42	D11	H12	Output	A/D output (MSB)
43	D10	H13	Output	A/D output
44	D9	G11	Output	A/D output
45	D8	G12	Output	A/D output
46	D7	G13	Output	A/D output
47	D6	F11	Output	A/D output
48	DRV_{DD}	D11	—	Digital driver power supply for signal processing block
49	DRV_{SS}	D13	—	Digital driver ground for signal processing block
50	D5	D12	Output	A/D output
51	D4	C11	Output	A/D output
52	D3	C13	Output	A/D output
53	D2	C12	Output	A/D output
54	D1	A10	Output	A/D output
55	D0	C9	Output	A/D output (LSB)
56	DV_{DD1}	B9	—	Power supply for signal processing block
57	DV_{SS1}	C8	—	Ground for signal processing block
58	VRT	B8	—	VRT
59	AUX	C7	—	External signal input
60	VRB	B7	—	VRB
61	V_{SS}	C6	—	Analog ground for signal processing block
62	DC_DET4	A6	—	Bias stabilization 2
63	DC_DET3	B6	—	Bias stabilization 1
64	V_{DD}	C5	—	Analog power supply for signal processing block
65	CCDOUT	A5	—	CDS signal input
66	V_{DD}	B5	—	Analog power supply for signal processing block
67	DC_DET2	C4	—	GCA output DC level stabilization

■ Pin Descriptions3

No.	Pin name	Pin	Type	Description
68	DC_DET1	A4	—	CDS output DC level stabilization
69	V_{SS}	B4	—	Analog ground for signal processing block
70	V_L	L6	—	(V-Driver) Low-level power supply
71	V_H	L7	—	(V-Driver) High-level power supply for vertical driver
72	V_{HH}	N9	—	(V-Driver) High-level power supply for fSUB driver
73	V_M	L10	—	(V-Driver) Middle-level power supply for vertical driver
74	V_{MSUB}	N10	—	(V-Driver) Middle-level power supply for fSUB driver
75	OSUB	M10	Output	(V-Driver) SUB pulse output
76	OV5C	L11	Output	(V-Driver) fV5C transfer pulse output
77	OV5B	N11	Output	(V-Driver) fV5B transfer pulse output
78	OV5A	M11	Output	(V-Driver) fV5A transfer pulse output
79	OV3C	K13	Output	(V-Driver) fV3C transfer pulse output
80	OV3B	J11	Output	(V-Driver) fV3B transfer pulse output
81	OV3A	J12	Output	(V-Driver) fV3A transfer pulse output
82	OV5L	J13	Output	(V-Driver) fV5L transfer pulse output
83	OV5R	H11	Output	(V-Driver) fV5R transfer pulse output
84	OV3L	F13	Output	(V-Driver) fV3L transfer pulse output
85	OV3R	F12	Output	(V-Driver) fV3R transfer pulse output
86	OV1S	E11	Output	(V-Driver) fV1S transfer pulse output
87	OV1C	E13	Output	(V-Driver) fV1C transfer pulse output
88	OV1B	E12	Output	(V-Driver) fV1B transfer pulse output
89	OV1A	B11	Output	(V-Driver) fV1A transfer pulse output
90	OV6	A11	Output	(V-Driver) fV6 transfer pulse output
91	OV4	C10	Output	(V-Driver) fV4 transfer pulse output
92	OV2	B10	Output	(V-Driver) fV2 transfer pulse output
93	V_M	A9	—	(V-Driver) Middle-level power supply for vertical driver
94	V_H	A8	—	(V-Driver) High-level power supply for vertical driver
95	V_L	A7	—	(V-Driver) Low-level power supply
96	RESET	A3	Input	(V-Driver) Reset pulse input
97	V_{SSSUB}	A1, A13 N1, N13	—	Ground for analog front end chip substrate

■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Supply voltage 1	V_{DD}, DRV_{DD}, DV_{DD1}, DV_{DD2}	4.6	V	*1
2	Supply voltage 2	DV_{DD3}	4.6	V	*1
3	Supply voltage 3	$V_{HH} - V_L$	25	V	*1
4	Supply voltage 4	$V_H - V_L$	25	V	*1
5	Supply voltage 5	V_L	– 9.0	V	*1
6	Supply voltage 6	V_{MSUB}	(VL+2.0) to 5.5	V	*1
7	Supply current	I_{CC}	—	mA	
8	Power dissipation	P_D	249	mW	*2
9	Operating ambient temperature	T_{opr}	– 20 to + 75	°C	*3
10	Storage temperature	T_{stg}	– 50 to + 125	°C	*3

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2 : The above power dissipation shows the package individual power dissipation at Ta = 75°C, in free-air.
Refer to the P_d-T_a diagram on sheet No. 45, and use this IC under the condition not exceeding the allowable value.
*3 : Ta = 25°C except storage temperature and operating ambient temperature .
*4 : This IC operates with the load capacitance of less than 5 500 pF, but this IC is tested only with load of sheet No.20. Care should be taken.

■ Operating supply voltage range

Parameter	Symbol	Range	Unit	Notes
Supply voltage 1	V_{DD}, DRV_{DD}, $DV_{DD1,}$ DV_{DD2}	2.9 V to 3.6	V	*1
Supply voltage 2	DV_{DD3}	2.9 V to 3.6	V	*1
Supply voltage 3	V_{HH}	11.3 V to 15.5	V	*1
Supply voltage 4	V_H	11.3 V to 15.5	V	*1
Supply voltage 5	V_L	–8.5 V to –4.0	V	*1
Supply voltage 6	V_{MSUB}	(V_L+2.0) to 5.0	V	*1
Supply voltage 7	V_M	—	—	*2

Note) *1 :The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2 : V_M should be used at the same potential as the ground pins.