

# DATA SHEET

## **TDA3608Q; TDA3608TH** Multiple voltage regulators with switch

Product specification  
Supersedes data of 2000 Oct 13  
File under Integrated Circuits, IC01

2001 Jun 29

## Multiple voltage regulators with switch

## TDA3608Q; TDA3608TH

### FEATURES

#### General

- Two  $V_P$ -state controlled regulators (regulator 1 and regulator 3) and a power switch
- Regulator 2 and reset circuit operate during load dump and thermal shutdown
- Separate control pins for switching regulator 1, regulator 3 and power switch
- Supply voltage range from  $-18$  to  $+50$  V
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1, regulator 3 and power switch are switched off)
- Hold output circuit for regulator 1 (only valid when regulator 3 output voltage  $>1.3$  V)
- Reset and hold outputs (open-collector outputs)
- Adjustable reset delay time
- High ripple rejection
- Backup capacitor connection to supply regulator 2 and reset circuit up to 25 V.

#### Protections

- Reverse polarity safe (down to  $-18$  V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be short circuited)
- ESD protection on all pins
- Thermal protection
- Load dump protection
- Foldback current limit protection for regulator 1, regulator 2 and regulator 3

- Delayed foldback current limit protection for power switch (at short-circuit); delay time fixed by reset delay capacitor
- All regulator outputs and power switch are DC short-circuited safe to ground and  $V_P$ .

### GENERAL DESCRIPTION

The TDA3608 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. It contains:

- Two fixed output voltage regulators with a foldback current protection (regulator 1 and regulator 3) and one fixed output voltage regulator (regulator 2) intended to supply a microcontroller, which also operates during load dump and thermal shutdown
- A power switch with protections, operated by an enable input
- Reset and hold outputs that can be used to interface with the microcontroller; the reset output can be used to call up the microcontroller and the hold output indicates that the regulator 1 output voltage is available and within the range
- A supply pin which can withstand load dump pulses and negative supply voltages
- Regulator 2 which is switched on at a backup voltage higher than 6.5 V and switched off when the regulator 2 output drops below 1.9 V
- A provision for the use of a reserve (backup) supply capacitor that will hold enough energy for regulator 2 (5 V continuous) to allow a microcontroller to prepare for loss of voltage.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3608Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6
TDA3608TH	HSOP20	plastic, heatsink small outline package; 20 leads; low stand-off height	SOT418-2

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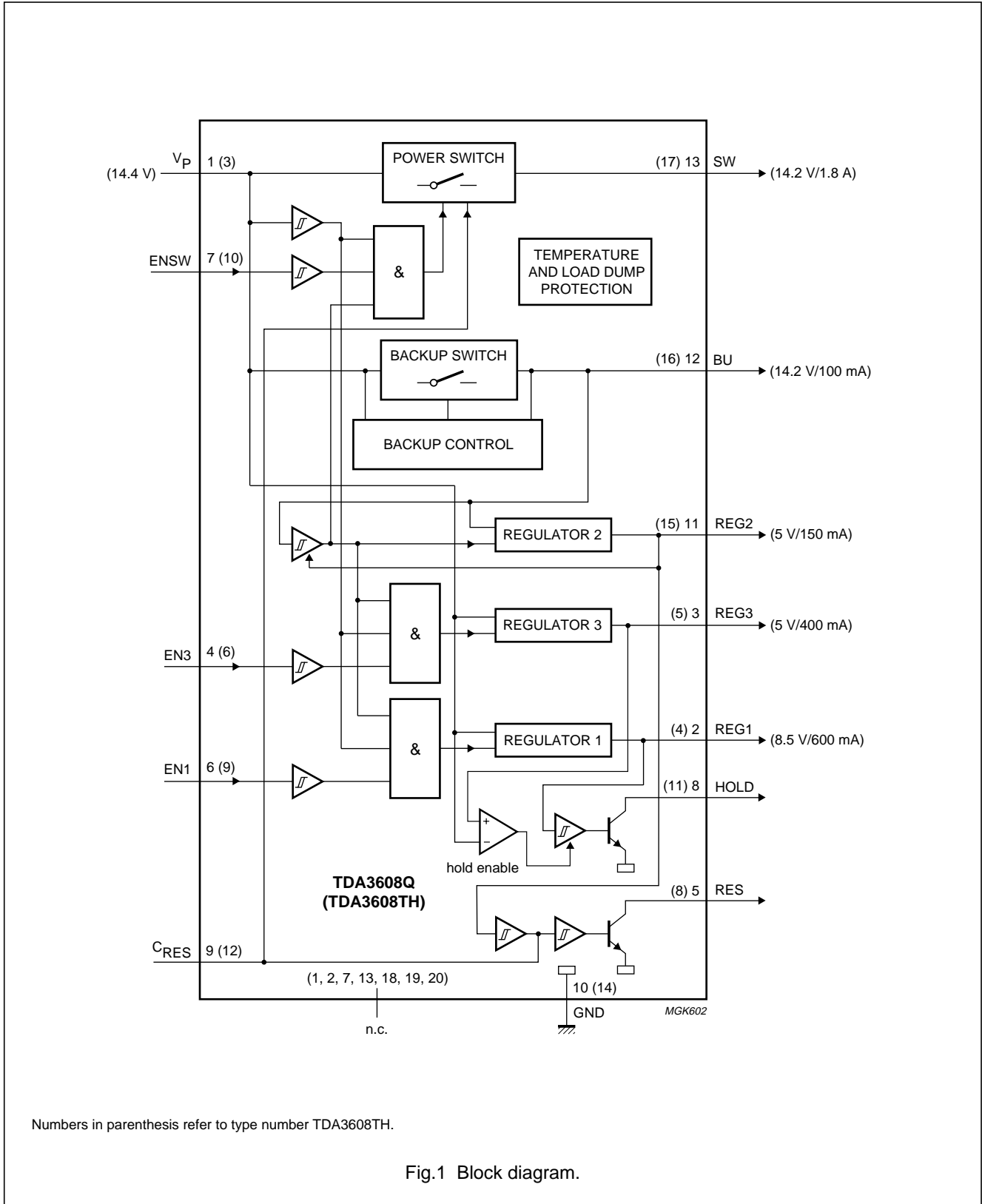
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_P$	supply voltage	operating	9.5	14.4	18	V
		regulator 2 on	2.4	14.4	18	V
		reverse polarity; non-operating	–	–	–18	V
		jump start for $t \leq 10$ minutes	–	–	30	V
		load dump protection for $t \leq 50$ ms and $t_r \geq 2.5$ ms	–	–	50	V
$I_q$	quiescent supply current	standby mode; $V_P = 12.4$ V	–	500	600	$\mu$ A
$T_j$	junction temperature		–40	–	+150	$^{\circ}$ C
<b>Voltage regulators</b>						
$V_{REG1}$	output voltage of regulator 1	$1 \text{ mA} \leq I_{REG1} \leq 600 \text{ mA}$	8.15	8.5	8.85	V
$V_{REG2}$	output voltage of regulator 2	$0.5 \text{ mA} \leq I_{REG2} \leq 150 \text{ mA}$	4.75	5.0	5.25	V
$V_{REG3}$	output voltage of regulator 3	$1 \text{ mA} \leq I_{REG3} \leq 400 \text{ mA}$	4.75	5.0	5.25	V
<b>Power switch</b>						
$V_{drop}$	dropout voltage	$I_{SW} = 1 \text{ A}$	–	0.45	0.7	V
		$I_{SW} = 1.8 \text{ A}$	–	1.0	1.8	V
$I_M$	peak current		2	–	–	A

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BLOCK DIAGRAM



Numbers in parenthesis refer to type number TDA3608TH.

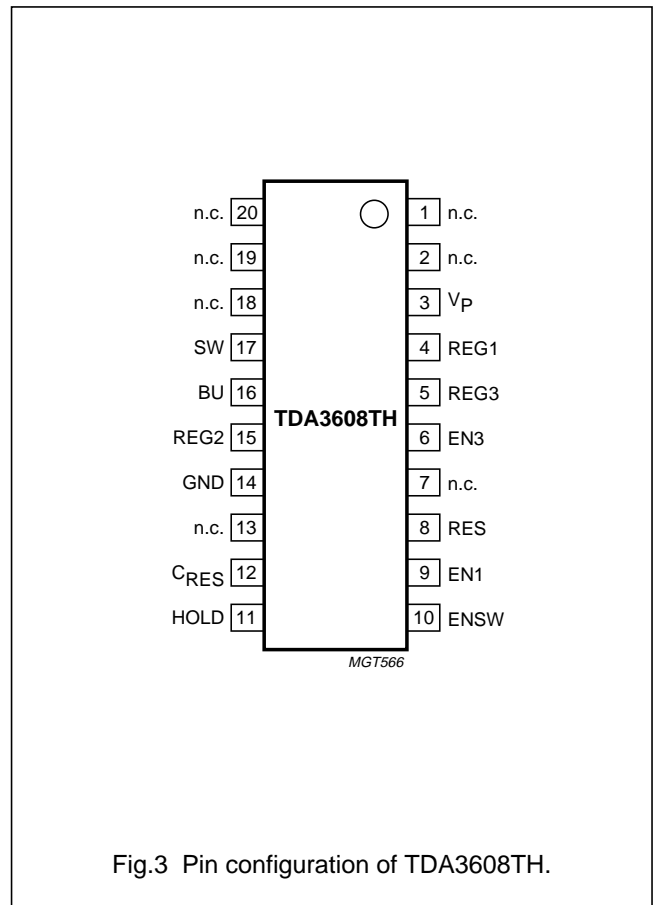
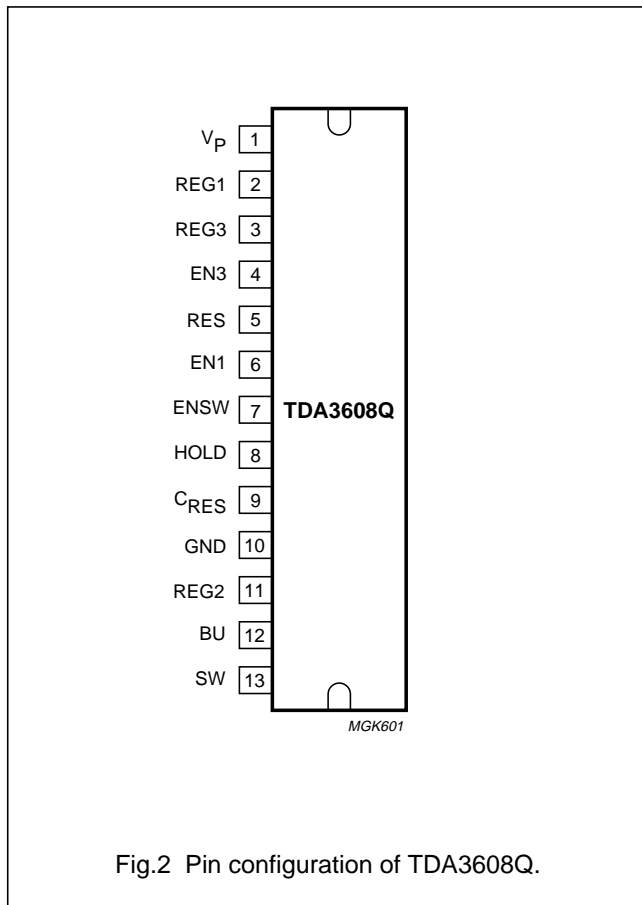
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN		DESCRIPTION
	TDA3608Q	TDA3608TH	
V <sub>P</sub>	1	3	supply voltage
REG1	2	4	regulator 1 output
REG3	3	5	regulator 3 output
EN3	4	6	regulator 3 enable input
RES	5	8	reset output
EN1	6	9	regulator 1 enable input
ENSW	7	10	power switch enable input
HOLD	8	11	hold output
C <sub>RES</sub>	9	12	reset delay capacitor connection
GND	10	14	ground
REG2	11	15	regulator 2 output
BU	12	16	backup capacitor connection
SW	13	17	power switch output
n.c.	–	1, 2, 7, 13, 18, 19 and 20	not connected



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### FUNCTIONAL DESCRIPTION

The TDA3608 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. Because of low-voltage operation of the car radio, low-voltage drop regulators are used in the TDA3608.

#### Backup supply

The charge of the backup capacitor connected to pin BU can be used to supply regulator 2 for a short period when the supply voltage  $V_P$  drops to 0 V (the time depends on the value of the capacitor).

#### Regulator 1

When the output voltage of regulator 2 and the supply voltage ( $V_P > 4.5$  V) are both available, regulator 1 can be operated by means of enable pin EN1 (see Fig.4).

#### Regulator 2

Regulator 2 switches on (see Fig.5) when the backup voltage exceeds 6.5 V for the first time and switches off when the output voltage of regulator 2 drops below 1.9 V (this is far below an engine start).

#### Regulator 3

When the output voltage of regulator 2 and the supply voltage ( $V_P > 4.5$  V) are both available, regulator 3 can be operated by means of enable pin EN3 (see Fig.4).

#### Reset

When regulator 2 is switched on and the output voltage of this regulator is within its voltage range, the reset output (see Fig.5) will be enabled (pin RES goes HIGH through an external pull-up resistor) to generate a reset to the microcontroller.

The reset cycles can be extended by means of an external capacitor connected to pin  $C_{RES}$ . This start-up feature is included to secure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of regulator 2 during the start-up sequence.

#### Hold

Regulator 1 has an open-collector hold output (see Fig.4) indicating that the output voltage is settled at 8.5 V. Pin HOLD is held HIGH by an external pull-up resistor. When the supply voltage  $V_P$  drops or during high load, the output voltage drops out-of-regulation and pin HOLD goes LOW.

The hold output is only activated when  $V_{REG3} > 1.3$  V. When pin HOLD is connected via a pull-up resistor to the output of regulator 3 spikes will be minimized to 1.3 V (maximum value) because the hold output is only disabled when  $V_{REG3} < 1.3$  V.

Pin HOLD will be forced LOW when the load dump protection is activated and also in the standby mode.

#### Power switch

The power switch can be controlled by means of enable pin ENSW (see Fig.6).

#### Protections

All output pins are fully protected.

The regulators are protected against load dump (regulator 1 and regulator 3 switch off at  $V_P > 18$  V) and short-circuit (foldback current protection).

The power switch contains a foldback current protection, but this protection is delayed at a short-circuit condition by the reset delay capacitor. During this time the output current is limited to at least 2 A (peak value) and 1.8 A (continuous value) at  $V_P \leq 18$  V. During the foldback mode the current is limited to 0.5 A (typical value).

The timing diagram is shown in Fig.7.

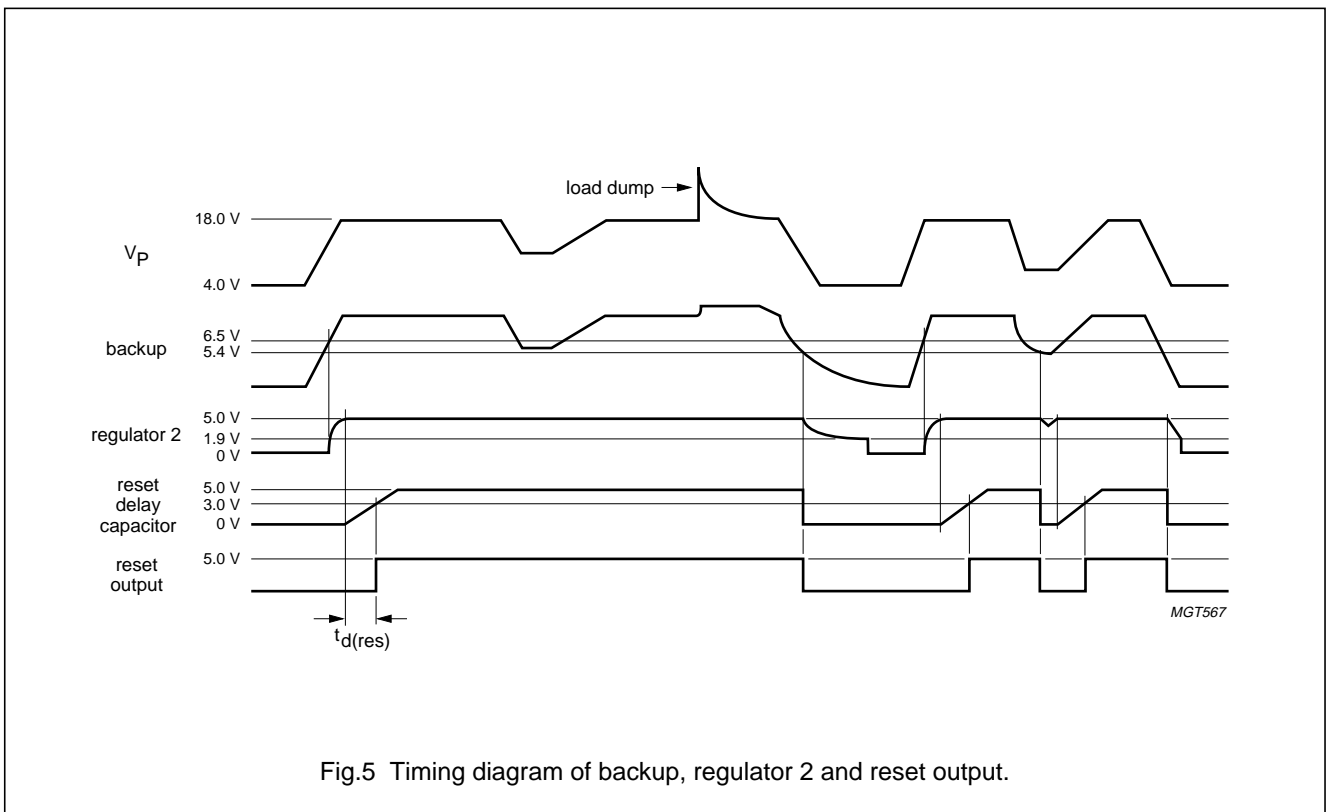
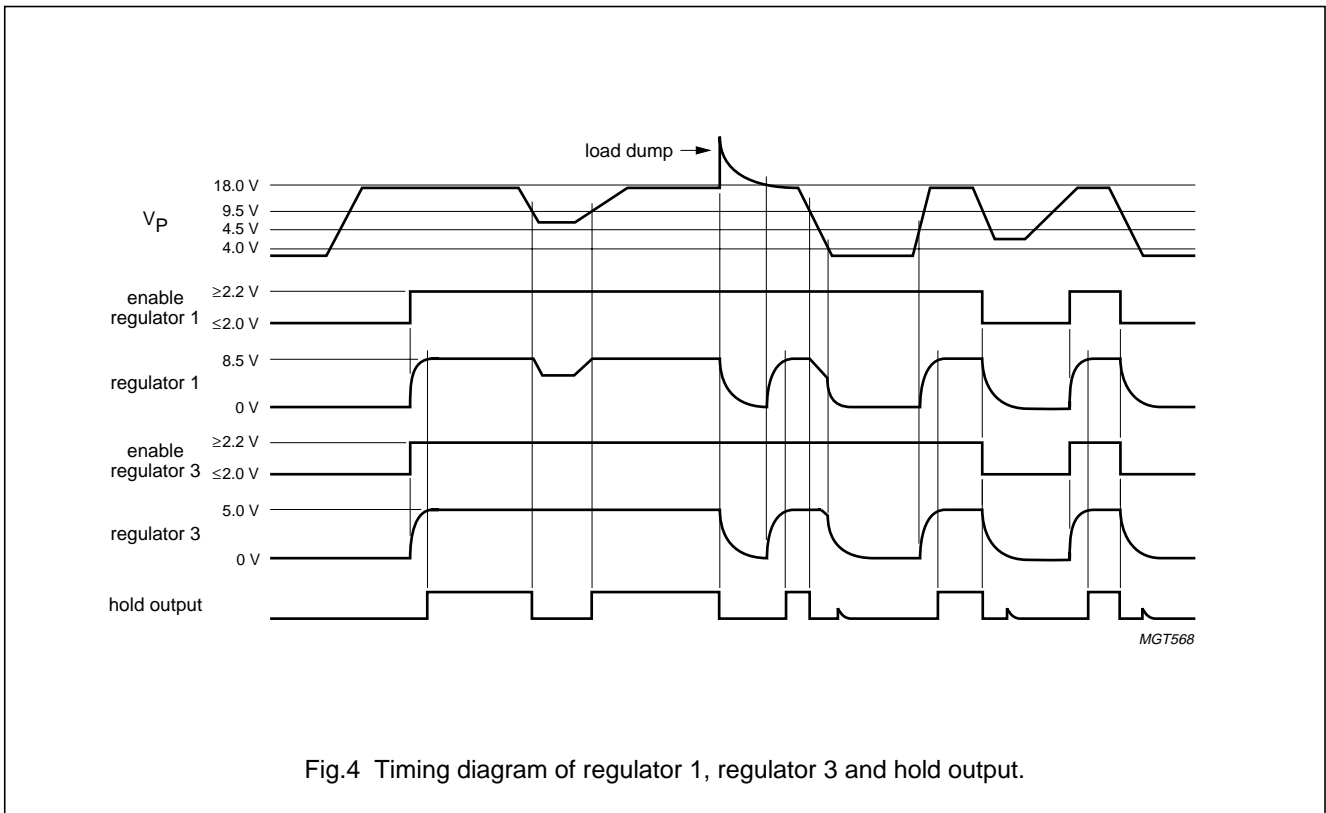
The foldback protection is activated when  $V_{SW} < 4$  V. When regulator 2 is out-of-regulation and generates a reset, the power switch is in the foldback mode immediately when  $V_{SW} < 4$  V.

In the standby mode the voltage on the reset delay capacitor is about 4 V and the voltage on the power switch output is  $V_P - 0.45$  V (typical value) at  $I_{SW} = 1$  A. During an overload condition or short-circuit the reset delay capacitor will be charged to a higher voltage. The power switch is in the high current mode while the capacitor is charged, after this the switch is in the foldback mode ( $V_{SW} < 4$  V). While the reset delay capacitor is charged the power switch output can reach its correct output voltage. Now the voltage on the reset delay capacitor is decreased rapidly to 4 V. The reset output voltage is not influenced by this change of voltages. The time of the high current mode depends on the value of the reset delay capacitor.

At  $V_P > 18$  V the power switch is clamped at maximum 17.2 V (to avoid that external connected circuitry is being damaged by an overvoltage) and the power switch will switch off at load dump.

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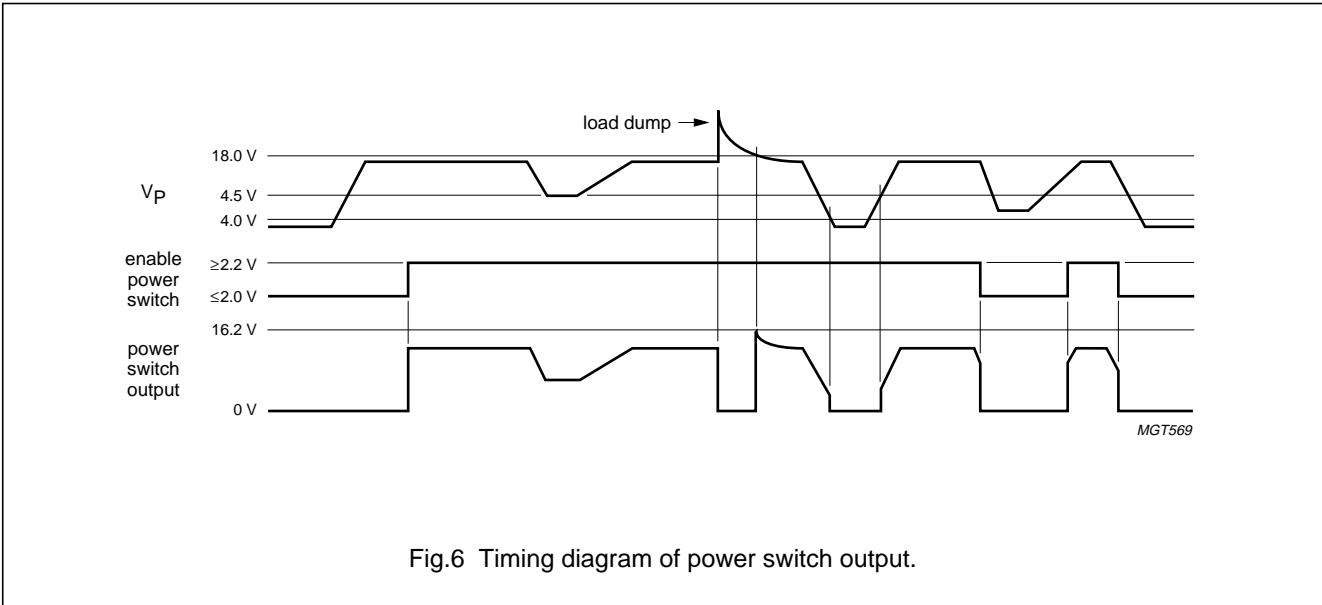


Fig.6 Timing diagram of power switch output.

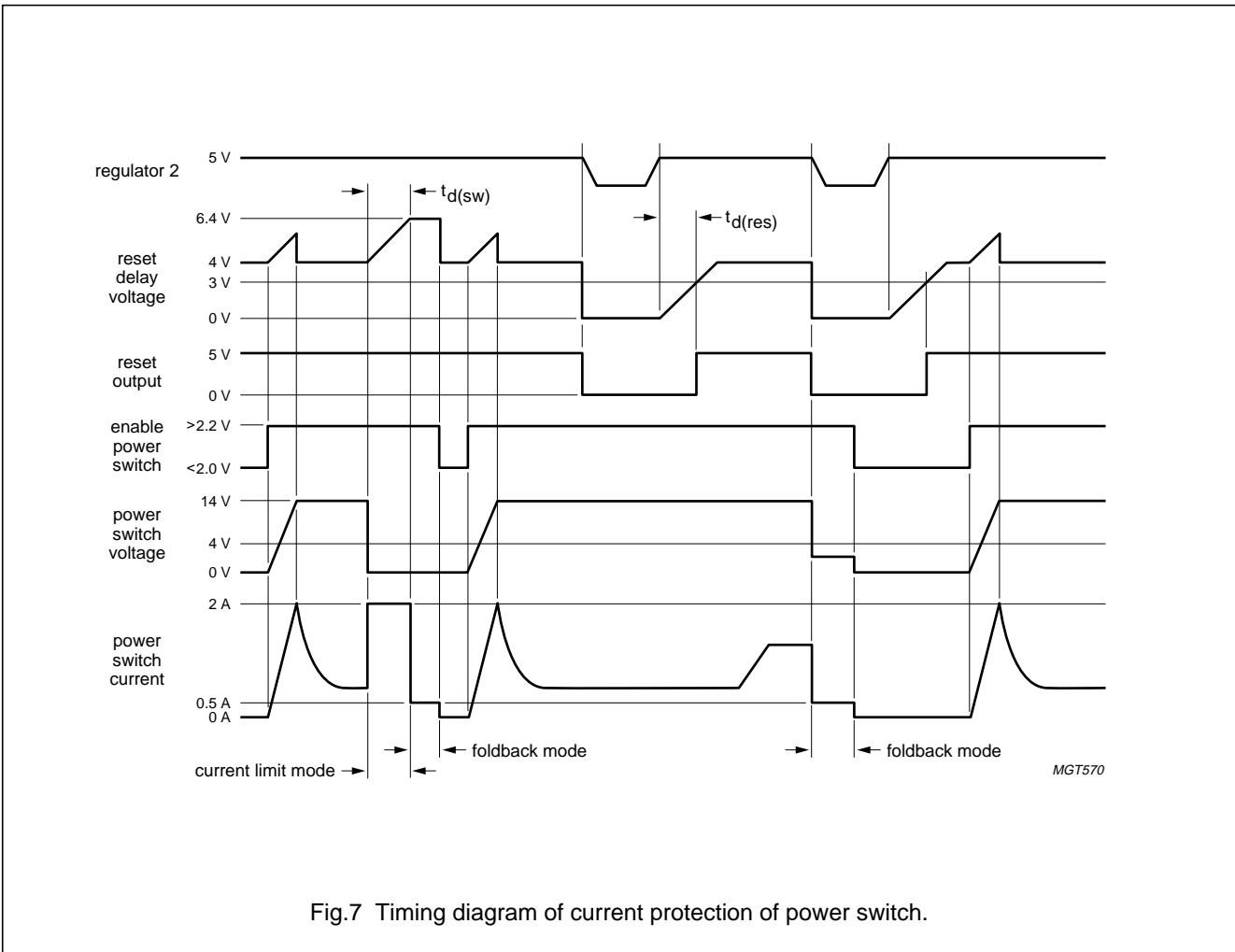


Fig.7 Timing diagram of current protection of power switch.



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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>P</sub>	supply voltage	operating	–	18	V
		reverse polarity; non-operating	–	–18	V
		jump start for t ≤ 10 minutes	–	30	V
		load dump protection for t ≤ 50 ms and t <sub>r</sub> ≥ 2.5 ms	–	50	V
P <sub>tot</sub>	total power dissipation		–	62	W
T <sub>stg</sub>	storage temperature	non-operating	–55	+150	°C
T <sub>amb</sub>	ambient temperature	operating	–40	+85	°C
T <sub>j</sub>	junction temperature	operating	–40	+150	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-c)</sub>	thermal resistance from junction to case TDA3608Q TDA3608TH		2 3.5	K/W K/W
		in free air	50	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	50	K/W

**CHARACTERISTICS**V<sub>P</sub> = 14.4 V; T<sub>amb</sub> = 25 °C; measured in test circuit of Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
V <sub>P</sub>	supply voltage	operating	9.5	14.4	18	V
		regulator 2 on; note 1	2.4	14.4	18	V
		jump start for t ≤ 10 minutes	–	–	30	V
		load dump protection for t ≤ 50 ms and t <sub>r</sub> ≥ 2.5 ms	–	–	50	V
I <sub>q</sub>	quiescent supply current	standby mode; note 2 V <sub>P</sub> = 12.4 V	–	500	600	μA
		V <sub>P</sub> = 14.4 V	–	520	–	μA
<b>Schmitt trigger supply voltage for regulator 1, regulator 3 and power switch</b>						
V <sub>thr</sub>	rising threshold voltage		4.0	4.5	5.0	V
V <sub>thf</sub>	falling threshold voltage		3.5	4.0	4.5	V
V <sub>hys</sub>	hysteresis voltage		–	0.5	–	V
<b>Schmitt trigger supply voltage for regulator 2</b>						
V <sub>thr</sub>	rising threshold voltage		6.0	6.5	7.1	V
V <sub>thf</sub>	falling threshold voltage		1.7	1.9	2.2	V
V <sub>hys</sub>	hysteresis voltage		–	4.6	–	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Schmitt trigger voltage for enable input (regulator 1, regulator 3 and power switch)</b>						
$V_{thr}$	rising threshold voltage		1.7	2.2	2.7	V
$V_{thf}$	falling threshold voltage		1.5	2.0	2.5	V
$V_{hys}$	hysteresis voltage	$I_{REG} = I_{SW} = 1 \text{ mA}$	0.1	0.2	0.5	V
$I_{LI}$	input leakage current	$V_{EN} = 5 \text{ V}$	1	5	10	$\mu\text{A}$
<b>Schmitt trigger voltage for reset</b>						
$V_{thr}$	rising threshold voltage of regulator 2	$V_P$ rising; $I_{REG2} = 50 \text{ mA}$ ; note 3	–	$V_{REG2} - 0.15$	$V_{REG2} - 0.075$	V
$V_{thf}$	falling threshold voltage of regulator 2	$V_P$ falling; $I_{REG2} = 50 \text{ mA}$ ; note 3	4.3	$V_{REG2} - 0.35$	–	V
$V_{hys}$	hysteresis voltage		0.1	0.2	0.3	V
<b>Schmitt trigger voltage for hold</b>						
$V_{thr}$	rising threshold voltage of regulator 1	$V_P$ rising; note 3	–	$V_{REG1} - 0.15$	$V_{REG1} - 0.075$	V
$V_{thf}$	falling threshold voltage of regulator 1	$V_P$ falling; note 3	7.7	$V_{REG1} - 0.35$	–	V
$V_{hys}$	hysteresis voltage		0.1	0.2	0.3	V
<b>Reset and hold output</b>						
$I_{sinkL}$	LOW-level sink current	$V_o \leq 0.8 \text{ V}$	2	–	–	$\text{mA}$
$I_{LO}$	output leakage current	$V_o = 5 \text{ V}$ ; $V_P = 14.4 \text{ V}$	–	–	2	$\mu\text{A}$
$t_r$	rise time	note 4	–	7	50	$\mu\text{s}$
$t_f$	fall time	note 4	–	1	50	$\mu\text{s}$
<b>Reset delay capacitor circuit</b>						
$I_{ch}$	charge current		2	3	4	$\mu\text{A}$
$I_{dch}$	discharge current		500	800	–	$\mu\text{A}$
$V_{thr(res)}$	rising threshold voltage for delayed reset pulse		2.8	3.0	3.2	V
$V_{thr(sw)}$	rising threshold voltage for delayed power switch foldback mode	note 5	–	6.4	–	V
$t_{d(res)}$	reset delay time	$C7 = 47 \text{ nF}$ ; note 6	32	47	70	ms
<b>Regulator 1; <math>I_{REG1} = 5 \text{ mA}</math>; unless otherwise specified</b>						
$V_{REG1(off)}$	output voltage with regulator off		–	1	400	mV
$V_{REG1}$	output voltage	$1 \text{ mA} \leq I_{REG1} \leq 600 \text{ mA}$	8.15	8.5	8.85	V
		$9.5 \text{ V} \leq V_P \leq 18 \text{ V}$	8.15	8.5	8.85	V
$\Delta V_{line}$	line regulation	$9.5 \text{ V} \leq V_P \leq 18 \text{ V}$	–	2	75	mV
$\Delta V_{load}$	load regulation	$1 \text{ mA} \leq I_{REG1} \leq 600 \text{ mA}$	–	20	50	mV
$I_q$	quiescent current	$I_{REG1} = 600 \text{ mA}$	–	25	60	$\text{mA}$
SVRR	supply voltage ripple rejection	$f_i = 3 \text{ kHz}$ ; $V_i = 2 \text{ V (p-p)}$	60	70	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{drop}$	dropout voltage	$V_P = 8.5 \text{ V}$ ; $I_{REG1} = 550 \text{ mA}$ ; note 7	–	0.4	0.7	V
$I_m$	current limit	$V_{REG1} > 7.5 \text{ V}$ ; see Fig.8; note 8	0.65	1.2	–	A
$I_{sc}$	short-circuit current	$R_L \leq 0.5 \Omega$ ; see Fig.8; note 9	250	800	–	mA
<b>Regulator 2; <math>I_{REG2} = 5 \text{ mA}</math>; unless otherwise specified</b>						
$V_{REG2}$	output voltage	$0.5 \text{ mA} \leq I_{REG2} \leq 150 \text{ mA}$	4.75	5.0	5.25	V
		$I_{REG2} = 300 \text{ mA}$ ; note 10	4.75	5.0	5.25	V
		$7 \text{ V} \leq V_P \leq 18 \text{ V}$	4.75	5.0	5.25	V
		$18 \text{ V} \leq V_P \leq 50 \text{ V}$ ; $I_{REG2} \leq 150 \text{ mA}$	4.75	5.0	5.25	V
$\Delta V_{line}$	line regulation	$6 \text{ V} \leq V_P \leq 18 \text{ V}$	–	2	50	mV
		$18 \text{ V} \leq V_P \leq 50 \text{ V}$	–	15	75	mV
$\Delta V_{load}$	load regulation	$1 \text{ mA} \leq I_{REG2} \leq 150 \text{ mA}$	–	20	50	mV
		$1 \text{ mA} \leq I_{REG2} \leq 300 \text{ mA}$	–	–	100	mV
SVRR	supply voltage ripple rejection	$f_i = 3 \text{ kHz}$ ; $V_i = 2 \text{ V (p-p)}$	60	70	–	dB
$V_{drop}$	dropout voltage	normal supply; note 7				
		$V_P = 4.75 \text{ V}$ ; $I_{REG2} = 100 \text{ mA}$	–	0.4	0.6	V
		$V_P = 5.75 \text{ V}$ ; $I_{REG2} = 200 \text{ mA}$	–	0.8	1.2	V
		backup supply; note 11				
		$V_{BU} = 4.75 \text{ V}$ ; $I_{REG2} = 100 \text{ mA}$	–	0.2	0.5	V
		$V_{BU} = 5.75 \text{ V}$ ; $I_{REG2} = 200 \text{ mA}$	–	0.8	1.0	V
$I_m$	current limit	$V_{REG2} > 4.5 \text{ V}$ ; see Fig.9; note 8	0.32	0.37	–	A
$I_{sc}$	short-circuit current	$R_L \leq 0.5 \Omega$ ; see Fig.9; note 9	20	100	–	mA
<b>Regulator 3; <math>I_{REG3} = 5 \text{ mA}</math>; unless otherwise specified</b>						
$V_{REG3(off)}$	output voltage with regulator off		–	1	400	mV
$V_{REG3}$	output voltage	$1 \text{ mA} \leq I_{REG3} \leq 400 \text{ mA}$	4.75	5.0	5.25	V
		$7 \text{ V} \leq V_P \leq 18 \text{ V}$	4.75	5.0	5.25	V
$\Delta V_{line}$	line regulation	$7 \text{ V} \leq V_P \leq 18 \text{ V}$	–	2	50	mV
$\Delta V_{load}$	load regulation	$1 \text{ mA} \leq I_{REG3} \leq 400 \text{ mA}$	–	20	50	mV
$I_q$	quiescent current	$I_{REG3} = 400 \text{ mA}$	–	15	40	mA
SVRR	supply voltage ripple rejection	$f_i = 3 \text{ kHz}$ ; $V_i = 2 \text{ V (p-p)}$	60	70	–	dB
$V_{drop}$	dropout voltage	$V_P = 5.75 \text{ V}$ ; $I_{REG3} = 400 \text{ mA}$ ; note 7	–	1	1.5	V
$I_m$	current limit	$V_{REG3} > 4.5 \text{ V}$ ; see Fig.10; note 8	0.45	0.70	–	A
$I_{sc}$	short-circuit current	$R_L \leq 0.5 \Omega$ ; see Fig.10; note 9	100	400	–	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Power switch</b>						
$V_{\text{drop}}$	dropout voltage	$I_{\text{SW}} = 1 \text{ A}$ ; note 12	–	0.45	0.7	V
		$I_{\text{SW}} = 1.8 \text{ A}$ ; note 12	–	1.0	1.8	V
$V_{\text{cl}}$	clamping voltage	$V_{\text{P}} \geq 18 \text{ V}$	15	16.2	17.2	V
$V_{\text{fb}}$	flyback voltage behaviour	$I_{\text{SW}} = -100 \text{ mA}$	–	$V_{\text{P}} + 3$	22	V
$I_{\text{dc}}$	continuous current	$V_{\text{P}} = 16 \text{ V}$ ; $V_{\text{SW}} = 13.5 \text{ V}$	1.8	2.0	–	A
$I_{\text{M}}$	peak current	$V_{\text{P}} = 17 \text{ V}$ ; see Fig.11; note 13	2	–	–	A
$I_{\text{sc}}$	short-circuit current	$V_{\text{P}} = 14.4 \text{ V}$ ; $V_{\text{SW}} < 3.5 \text{ V}$ ; see Fig.11; note 14	–	0.5	–	A
<b>Backup switch</b>						
$I_{\text{dc}}$	continuous current		0.3	0.35	–	A
$V_{\text{cl}}$	clamping voltage	$V_{\text{P}} \geq 16.7 \text{ V}$	–	–	16	V
$I_{\text{r}}$	reverse current	$V_{\text{P}} = 0$ ; $V_{\text{BU}} = 12.4 \text{ V}$ ; note 15	–	–	900	mA

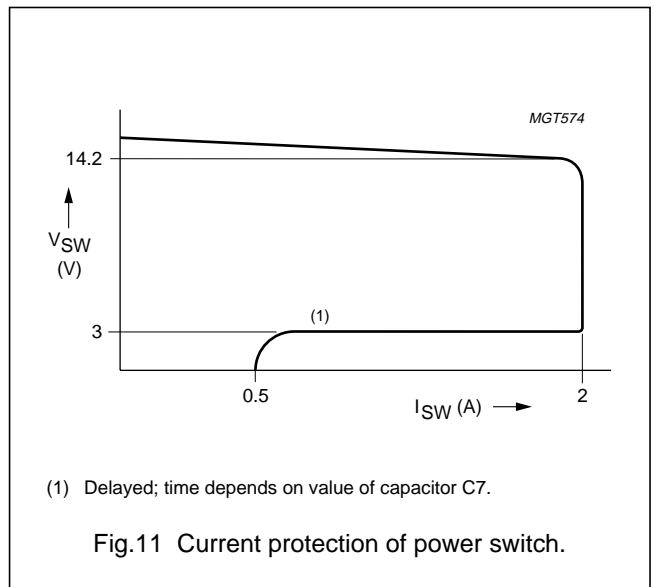
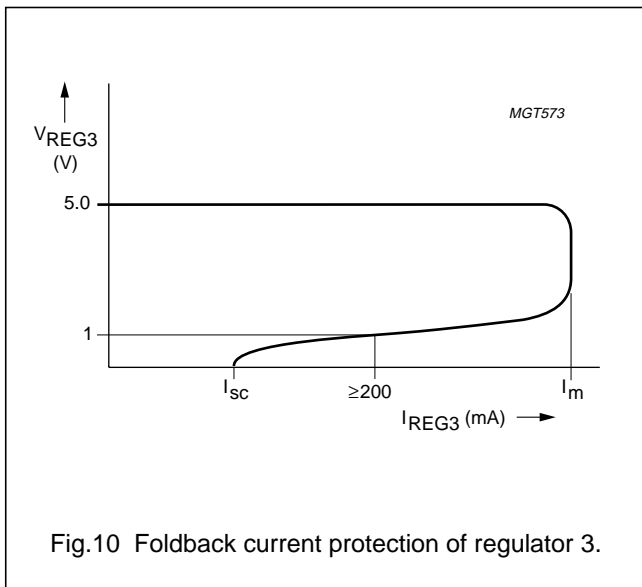
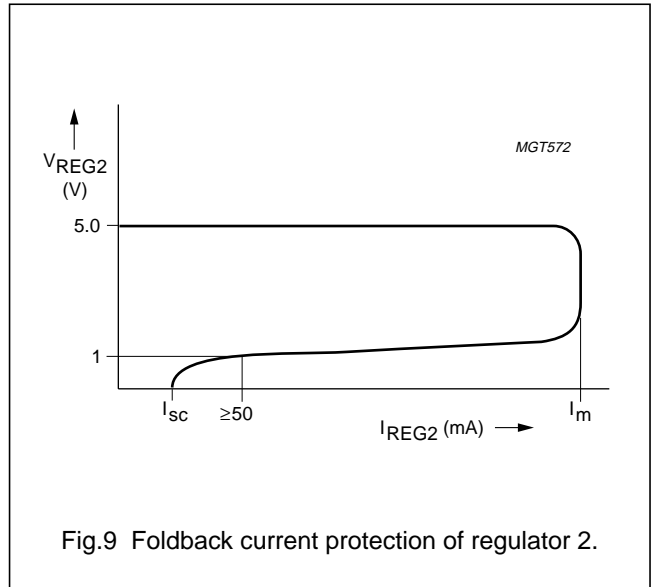
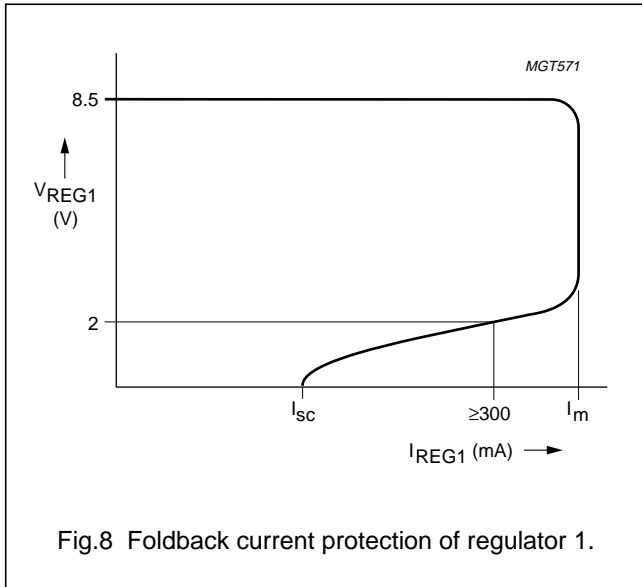
**Notes**

- The minimum value is the minimum operating voltage, only if  $V_{\text{P}}$  has exceeded 6.5 V.
- The quiescent current is measured in the standby mode. Therefore, the enable inputs of regulator 1, regulator 3 and the power switch are grounded and  $R_{\text{L(REG2)}} = \infty$ .
- The voltage of the regulator drops as a result of a  $V_{\text{P}}$  drop.
- The rise and fall time is measured with a 10 k $\Omega$  pull-up resistor and  $C_{\text{L}} = 50 \text{ pF}$ .
- This is the threshold voltage for the delay time of the power switch. The voltage on the reset delay capacitor increases only at low output voltage of the power switch (for example at short circuit). When the voltage on this capacitor exceeds this threshold voltage, the power switch is set to the foldback mode. The power switch is also protected by the temperature protection.
- Delay time calculation:
  - Reset pulse delay:  $t_{\text{d(res)}} = \frac{C}{I_{\text{ch}}} \times V_{\text{C(th1)}} = C \times 1000 \times 10^3$  [sec] The delay time is 47 ms for  $C = 47 \text{ nF}$ .
  - Power switch delay:  $t_{\text{d(sw)}} = \frac{C}{I_{\text{ch}}} \times V_{\text{C(th2)}} = C \times 500 \times 10^3$  [sec] The delay time is 23.5 ms for  $C = 47 \text{ nF}$ .
- The dropout voltage of regulator 1, regulator 2 and regulator 3 is measured between pin  $V_{\text{P}}$  and pins REG1, REG2 or REG3 respectively.
- During current limit, current  $I_{\text{M}}$  is held constant.
- The foldback current protection limits the dissipated power at short-circuit.
- The peak current of 300 mA can only be applied for short periods ( $t < 100 \text{ ms}$ ).
- The dropout voltage is measured between pins BU and REG2.
- The dropout voltage of the power switch is measured between pins  $V_{\text{P}}$  and SW.
- The maximum output current of the power switch is limited to 1.8 A when  $V_{\text{P}} > 18 \text{ V}$ .

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- 14. During short-circuit, current  $I_{sc}$  of the power switch is held constant to a lower value than the continuous current after a delay of at least 10 ms. Furthermore, a foldback function is activated after the delay. When  $V_{SW} < 3.5$  V, the short-circuit current is reduced to 0.5 A (typical value). The short-circuit protection of the power switch functions best when  $C1 = 220 \mu\text{F}$  and  $C2 = 10 \mu\text{F}$ .
- 15. The reverse current of the backup switch is the current which is flowing out of pin  $V_P$  at  $V_P = 0$  V.

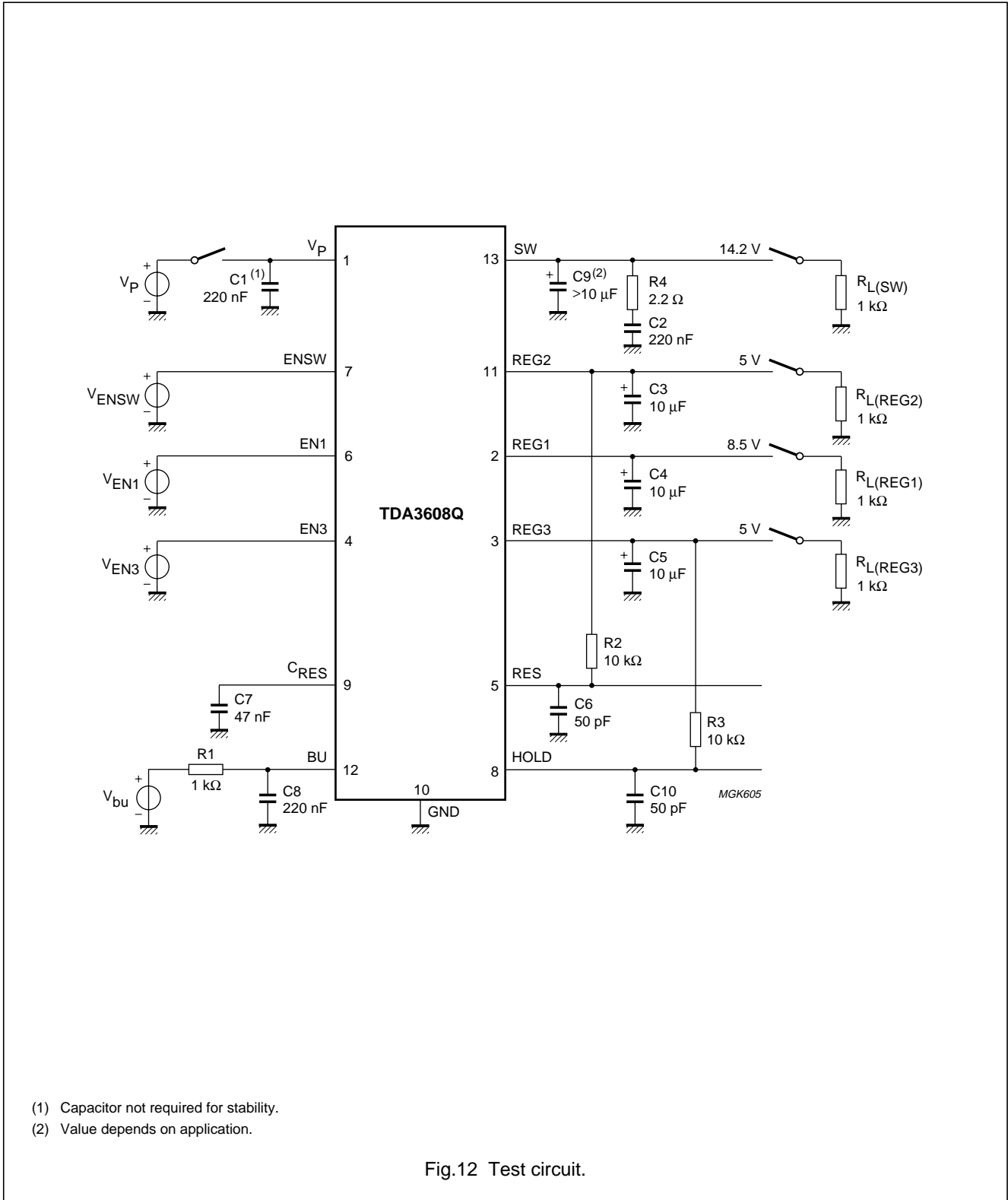


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TEST AND APPLICATION INFORMATION

Test information



(1) Capacitor not required for stability.  
 (2) Value depends on application.

Fig.12 Test circuit.

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Application information

NOISE

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (the output noise of the regulators is translated into a current noise by means of the output capacitors). Table 1 shows the noise figure with the corresponding output capacitor  $C_o$  for each regulator. The noise is minimal when a high frequency capacitor of 220 nF in parallel with an electrolytic capacitor of 100  $\mu\text{F}$  is connected directly to pins  $V_P$  and GND.

Table 1 Noise figure; note 1

REGULATOR	NOISE FIGURE ( $\mu\text{V}$ )		
	$C_o = 10 \mu\text{F}$	$C_o = 47 \mu\text{F}$	$C_o = 100 \mu\text{F}$
1	225	150	135
2	225	150	135
3	255	200	180

Note

1. Measured at a bandwidth of 200 kHz.

STABILITY

The regulators are made stable with the externally connected output capacitors. The output capacitors can be selected using the graphs of Figs 13 and 14. When an electrolytic capacitor is used, the temperature behaviour of this output capacitor can cause oscillations at low temperature. The next two examples show how an output capacitor value is selected.

Example 1

The regulator 1 is made stable with an electrolytic output capacitor of 220  $\mu\text{F}$  with  $\text{ESR} = 0.15 \Omega$ . At  $T_{\text{amb}} = -30 \text{ }^\circ\text{C}$  the capacitor value is decreased to 73  $\mu\text{F}$  and the ESR is increased to 1.1  $\Omega$ . The regulator remains stable at  $T_{\text{amb}} = -30 \text{ }^\circ\text{C}$  (see Fig.13).

Example 2

The regulator 2 is made stable with an electrolytic capacitor of 10  $\mu\text{F}$  with  $\text{ESR} = 3 \Omega$ . At  $T_{\text{amb}} = -30 \text{ }^\circ\text{C}$  the capacitor value is decreased to 3  $\mu\text{F}$  and the ESR is increased to 23.1  $\Omega$ . The regulator will be unstable at  $T_{\text{amb}} = -30 \text{ }^\circ\text{C}$  (see Fig.14).

Solution

Use a tantalum capacitor of 10  $\mu\text{F}$  or a larger electrolytic capacitor. The use of tantalum capacitors is recommended to avoid problems with stability at low temperatures.

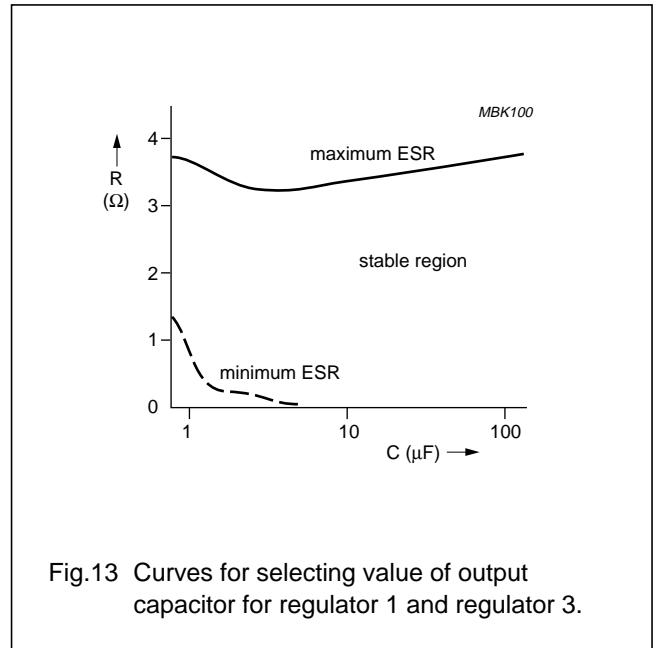


Fig.13 Curves for selecting value of output capacitor for regulator 1 and regulator 3.

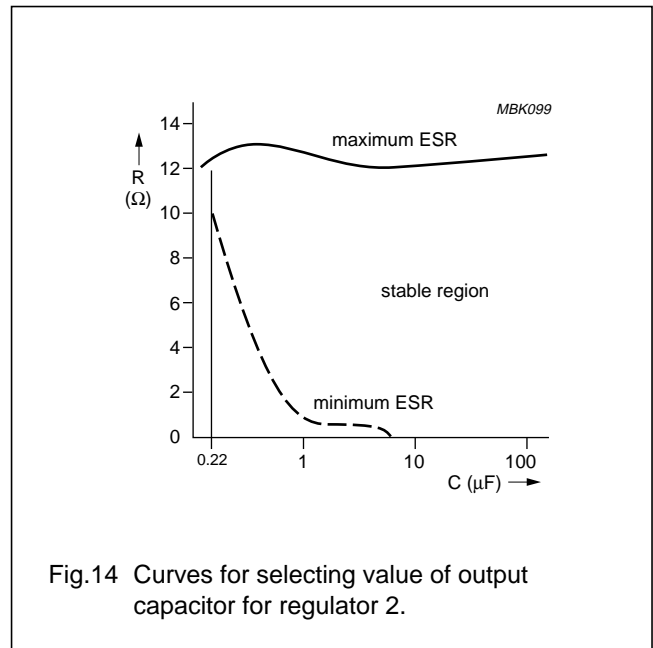


Fig.14 Curves for selecting value of output capacitor for regulator 2.

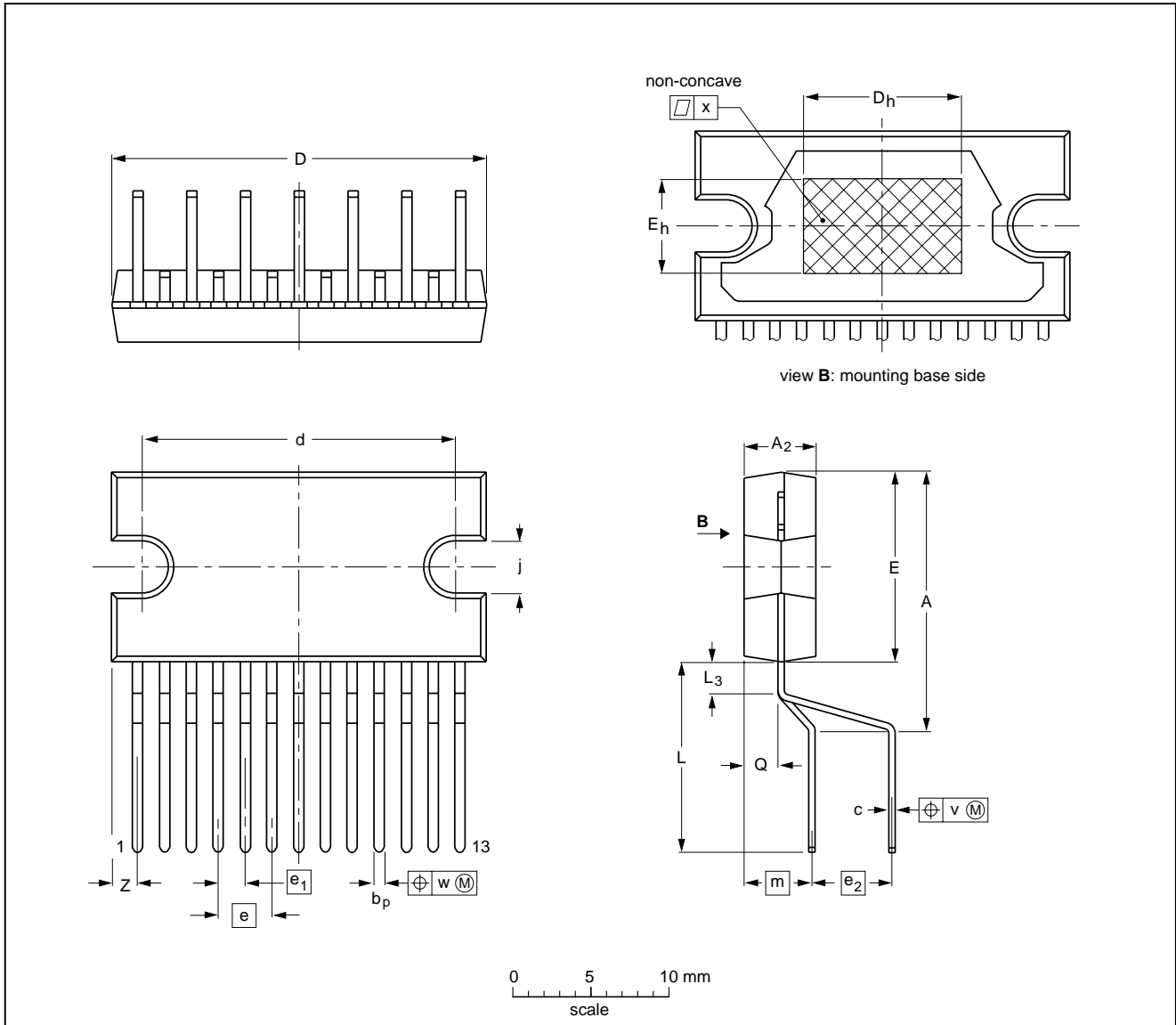
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PACKAGE OUTLINES

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)

SOT141-6



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>2</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	d	D <sub>h</sub>	E <sup>(1)</sup>	e	e <sub>1</sub>	e <sub>2</sub>	E <sub>h</sub>	j	L	L <sub>3</sub>	m	Q	v	w	x	z <sup>(1)</sup>
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						97-12-16 99-12-17

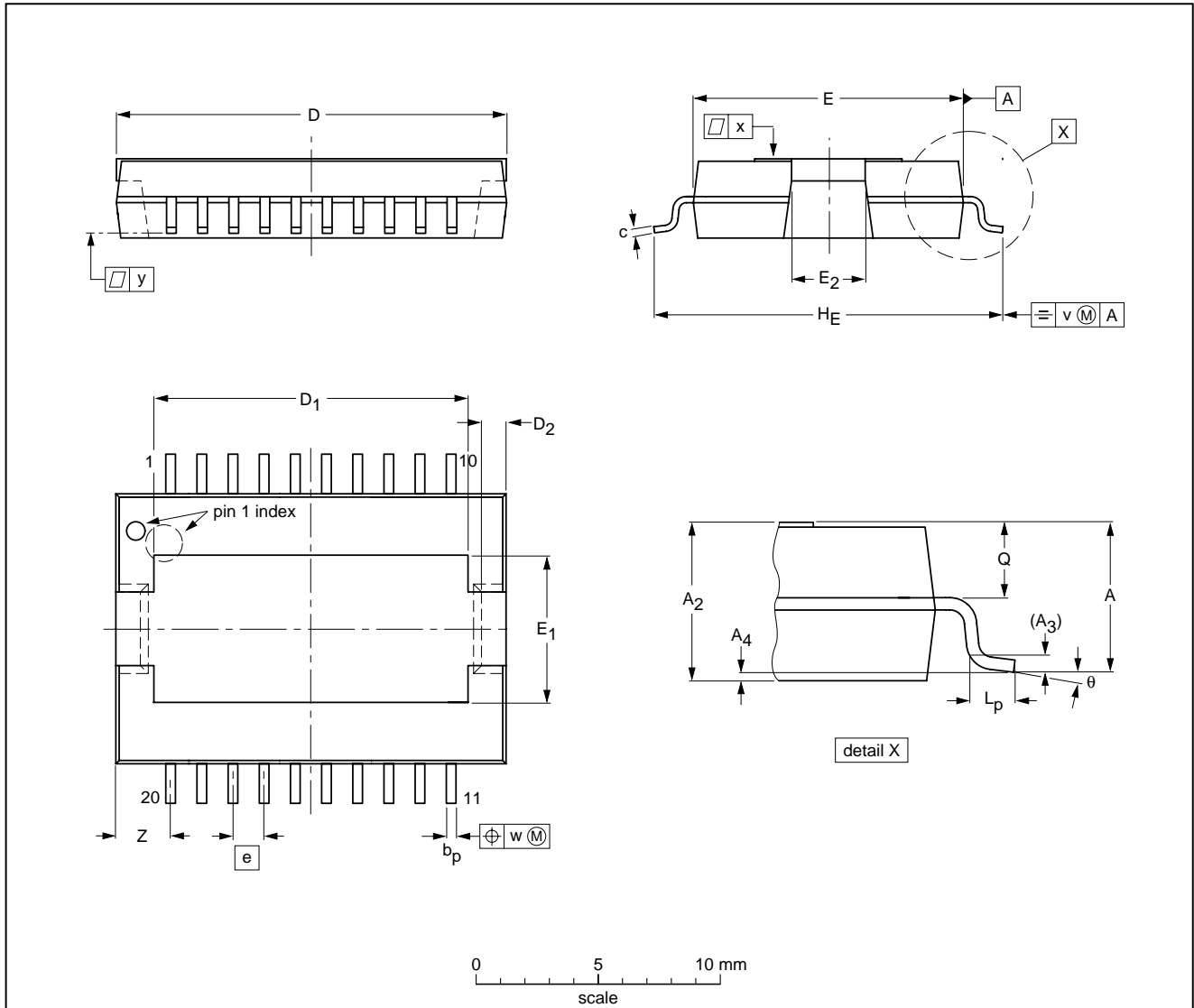


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HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height

SOT418-2



DIMENSIONS (mm are the original dimensions)

UNIT	A <sub>max.</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub> <sup>(1)</sup>	b <sub>p</sub>	c	D <sup>(2)</sup>	D <sub>1</sub>	D <sub>2</sub>	E <sup>(2)</sup>	E <sub>1</sub>	E <sub>2</sub>	e	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.12 -0.02	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

Notes

- Limits per individual lead.
- Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT418-2						98-02-25 99-11-12

## Multiple voltage regulators with switch

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### SOLDERING

#### Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Through-hole mount packages

##### SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### Surface mount packages

##### REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

##### WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW <sup>(1)</sup>	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable <sup>(2)</sup>	–	suitable
Surface mount	BGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(3)</sup>	suitable	–
	PLCC <sup>(4)</sup> , SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended <sup>(4)(5)</sup>	suitable	–
	SSOP, TSSOP, VSO	not recommended <sup>(6)</sup>	suitable	–

## Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “*Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*”.
- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 3 Figtree Drive, HOMEBUSH, NSW 2140,  
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

**Belgium:** see The Netherlands

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**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
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**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
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**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

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**France:** 7 - 9 Rue du Mont Valérien, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4728 6600, Fax. +33 1 4728 6638

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Hungary:** Philips Hungary Ltd., H-1119 Budapest, Fehervari ut 84/A,  
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**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
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Tel. +64 9 849 4160, Fax. +64 9 849 7811

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Tel. +55 11 821 2333, Fax. +55 11 821 2382

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**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
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**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
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ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

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