FUJITSU

FLOPPY DISK VFO

MB4107A

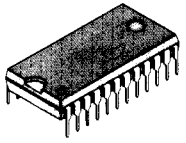
February 1989
Edition 2.0

FLOPPY DISK VFO

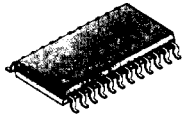
The Fujitsu MB4107A is a variable-frequency oscillator (VFO) IC for use in floppy-disk interfaces. It provides a complete data separation function, with a minimum of external parts and no adjustments, and can be used with a variety of disk controllers. It locks onto the read signal from the disk drive, which normally has jitter due to rotation speed variations and peak shifting, and produces a stable read signal for the controller. It also produces a window signal, which can be used to differentiate the clock and data pulses in the read signal.

The MB4107A includes functions for sync field detection, automatic loop filter gain switching, and address and index mark detection.

- The analog VFO (PLL) circuitry allows a wide read margin for the data separator.
- Can be connected to 8-inch ,5-inch and 3.5-inch floppy disk drives using the same external components.
- Handless both double-density (MFM) and single-density (FM) disks.
- Can be used with various floppy disk controllers such as the MB8876A, MB8877A, FD1791, and μPD 765.
- The discrimination function for gap and sync fields prevents incorrect locking on the gap field.
- The quick sync function (high gain) in the sync field is automatically switched to the stable tracking function (low gain).
- Because the sync pattern detector (data: 00_H, clock: FF_H) and the IBM format mark detector control PLL gain, the index, ID, and data fields can be locked onto without special control signals.
- A master clock is generated for the floppy disk controller, to prevent spikes when switching between each kind of floppy disks.
- External circuitry requires very few components, and no adjustments.
- Internal clock: 7 resistors, 5 capacitor, 1 crystal or ceramic resonator
  External clock: 5 resistors, 3 capacitors



PLASTIC PACKAGE
DIP-24P-M02



PLASTIC PACKAGE
FPT-24P-M02

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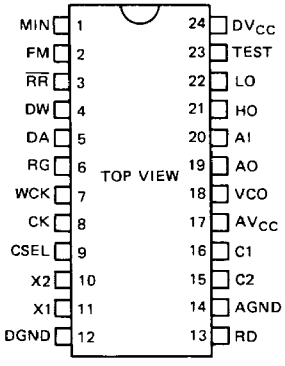
PIN ASSIGNMENT

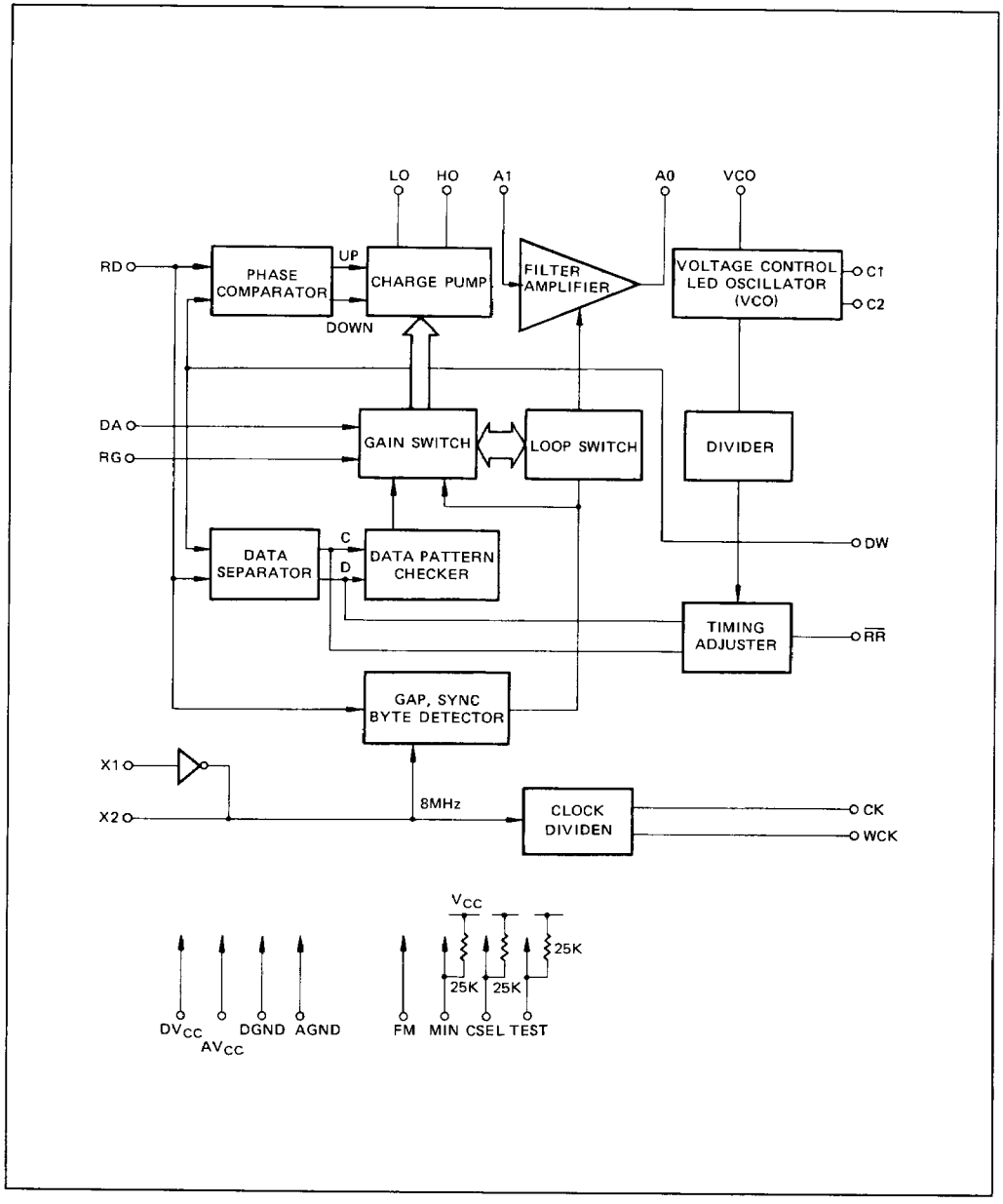


ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{CC}		7	V
Logic Input Voltage	V_{IN}		7	V
Power Dissipation	P_D	T ≦ 75°C	550	mW
Storage Temperature	T_{STG}		−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.


LO
HO
A1
A0
VCO
RD
PHASE COMPARATOR
UP
DOWN
CHARGE PUMP
FILTER AMPLIFIER
VOLTAGE CONTROL LED OSCILLATOR (VCO)
C1
C2
DA
RG
GAIN SWITCH
LOOP SWITCH
DIVIDER
DATA SEPARATOR
C
D
DATA PATTERN CHECKER
DW
TIMING ADJUSTER
RR
GAP, SYNC BYTE DETECTOR
X1
X2
8MHz
CLOCK DIVIDEN
CK
WCK
VCC
25K
25K
25K
DVCC
AVCC
DGND
AGND
FM
MIN
CSEL
TEST

PIN DESCRIPTION

Pin No.	Pin Name	Descriptions
1	MIN	Selects type of floppy disk as follows: – 8-inch floppy disk (STD) Low – 5-inch, 3.5-inch floppy disk 2D, 2DD (MIN) High 2HD, 2ED (3.5-inch 2MB) (STD) Low
2	FM	Selects the disk density as follows: – Single density (FM system) High – Double density (MFM system) Low
3	$\overline{RR}$	Read data signal for the FDC, including both clock and data pulses.
4	DW	Data window signal for separating the $\overline{RR}$ signal into data and clock pulses.
5	DA	Input for indicating a data field. When DA goes high, the PLL is kept as a low gain. Either RG or DA is used, but not both, and the unused pin is kept low.
6	RG	Read Gate (MB 8877A system) or VCO Sync (μPD765 system) input. When a high signal is applied to this pin, PLL is kept at a low gain.
7	WCK	The μPD 765 system FDC write clock pulse is output from this pin as follow: – STD 8-inch/MFM T = 1 μs – STD 8-inch/FM T = 2 μs – MIN 5-inch/MFM T = 2 μs – MIN 5-inch/FM T = 4 μs
8	CK	The FDC clock pulse is output from this pin as follows: – MB 8877A system/STD 8-inch 2 MHz – MB 8877A system/MIN 5-inch 1 MHz – μPD 765 system/STD 8-inch 8 MHz – μPD 765 system/MIN 5-inch 4 MHz
9	CSEL	Selects the FDC type shown below (an internal pull-up resistor is provided): – MB 8877A, FD 1791 system High – μPD 765 system Low
10	X2	(1) Inverter output for the quartz oscillator (2) This pin is open when a 8-MHz external clock is used.
11	X1	(1) Inverter input for the quartz oscillator (2) Input pin when an 8-MHz external clock is used.
12	DGND	Ground for digital circuits
13	RD	Input for the source read data from the FDD
14	AGND	Ground for analog circuits such as VCO and filter amplifier
15 16	C1 C2	An external capacitor for setting VCO oscillating frequency is connected to these pins.

PIN DESCRIPTION (continued)

Pin No.	Pin Name	Descriptions
17	AV_{CC}	Power supply for analog circuits such as the VCO and filter amplifier.
18	VCO	VCO control current input.
19	AO	Output pin for the low pass filter (LPF) amplifier in the VFO (PLL) circuit.
20	AI	Input pin for the LPF amplifier in the VFO (PLL) circuit
21	HO	Output pin to be externally connected to the LPF amplifier. This pin is selected at frequency lock after a sync field is detected. A high signal decreases the VCO frequency and a low signal increases it. (High gain)
22	LO	Output pin to be externally connected to the LPF amplifier. This pin is selected after frequency lock, for phase synchronization. A high signal delays the VCO phase, and a low signal advances it. (Low gain)
23	TEST	Used for the LSI function test. It is normally open or pulled up.
24	DV_{CC}	Power supply pin for digital circuits.

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Operating temperature range	T_{OP}	−20	25	75	°C

ELECTRICAL CHARACTERISTICS

1 – DC CHARACTERISTICS

Item	Symbol	Condition	Value			Unit	Applicable pin	Note
			Min	Typ	Max			
Supply current	I_{CC}	V_{CC} = 5.25 V	–	70	100	mA	V_{CC}	*4
High level input voltage	V_{IH}	V_{CC} = 4.75 to 5.25V	2.0	–	–	V	MIN, FM DA, RG CS, X1 RD	*3
Low level input voltage	V_{IL}		–	–	0.8	V		*3
High level input current	I_{IH}	V_{CC} = 5.25 V, V_I = 2.7 V	–	–	20	μA	FM, DA RG, X1 RD	–
Current at maximum input voltage	I_I	V_{CC} = 5.25 V, V_I = 7.0 V	–	–	0.1	mA		–
Low level input current	I_{IL}	V_{CC} = 5.25 V, V_I = 0.4 V	-400	-20	–	μA		–
Open-circuit input voltage	V_{IP}		4.85	5.0	–	V	MIN, CS	–
Low level input current	I_{ILP}	V_I = 0 V	-1.1	-0.6	–	mA		–
High level output voltage 1	V_{OH1}	V_{CC} = 4.75 V, I_{OH} = -1.2 mA	2.7	3.3	–	V	$\overline{RR}$, DW	*1 *3
Low level output voltage 1	V_{OL1}	V_{CC} = 4.75 V, I_{OL} = 12 mA	–	0.28	0.4	V		*2 *3
		V_{CC} = 4.75 V, I_{OL} = 24 mA	–	0.35	0.5	V		
Short-circuit output current 1	I_{OS1}	V_{CC} = 5.25 V	-30	–	-160	mA		*1 *3
High level output voltage 2	V_{OH2}	V_{CC} = 4.75 V, I_{OH} = -0.4 mA	2.7	3.3	–	V	WCK, CK	*1 *3
Low level output voltage 2	V_{OL2}	V_{CC} = 4.75 V, I_{OL} = 4 mA	–	0.28	0.4	V		*2 *3
		V_{CC} = 4.75 V, I_{OL} = 8 mA	–	0.35	0.5	V		
Short-circuit output current 2	I_{OS2}	V_{CC} = 5.25 V	-20	–	-110	mA		*1 *3
High level output voltage 3	V_{OH3}	V_{CC} = 4.75 V, I_{OH} = -0.4 mA	2.7	3.3	–	V	X2	*1 *3
Low level output voltage 3	V_{OL3}	V_{CC} = 4.75 V, I_{OL} = 1 mA	–	0.28	0.4	V		*2 *3
High output voltage	V_{HH}	I_{OH} = -1 mA	3.3	3.7	–	V	HO	*1
Low output voltage	V_{LH}	I_{OL} = 1 mA	–	2.0	2.4	V		*2
High output voltage	V_{HL}	I_{OH} = -0.2 mA	3.8	4.2	–	V	LO	*1
Low output voltage	V_{LL}	I_{OL} = 0.2 mA	–	1.5	1.9	V		*2
VCO free run frequency	f_{FR}		1.6	2.0	2.4	MHz		–

NOTE: *1 The output stage is set high. *2 The output stage is set low. *3 T_A = -20°C to 75°C

*4 V_{CC} is connected with A, V_{CC} & D, V_{CC}.

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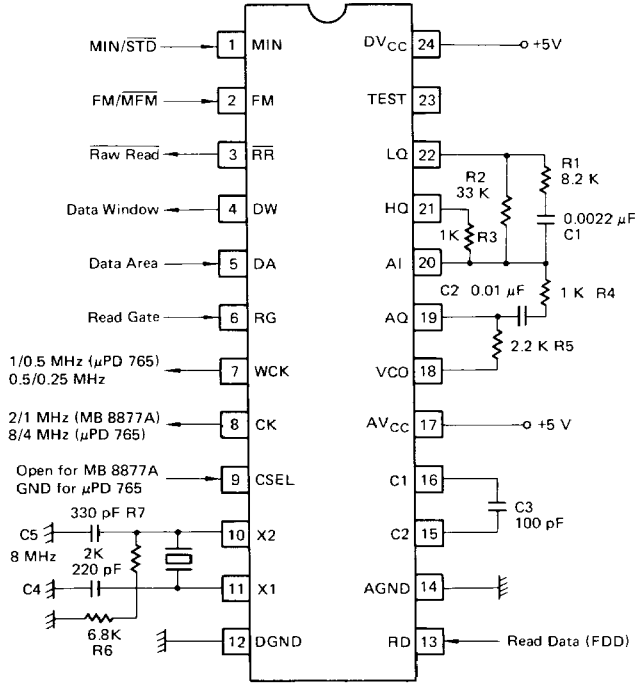
2 – AC CHARACTERISTICS

(V_{CC} = 5V, f_{X1} = 8MHz)

Item	Symbol	Condition		Value Min	Value Typ	Value Max	Unit	Applicable Pin
Rising Time	T_r	C_L = 25pF			3		ns	CK
Falling Time	T_f				2			
Frequency	f_{CK}	CSEL = "H" MB8876A	MIN = "L"		2		MHz	
			MIN = "H"		1			
		CSEL = "L" μPD765	MIN = "L"		8			
			MIN = "H"		4			
Duty Ratio	DR_{CK}	CSEL = "H"	C_L = 25pF		50		%	
		CSEL = "L"			50			
Rising Time	T_r	C_L = 25pF			3		ns	WCK
Falling Time	T_f				2			
Cycle Time	T_{CY}	MIN = "L"	MFM = "H"		1		μs	
			MFM = "L"		2			
		MIN = "H"	MFM = "H"		2			
			MFM = "L"		4			
"H" Level Width	T_{WH}	MIN = "L"	MFM = "H"		125		ns	
			MFM = "L"		125			
		MIN = "H"	MFM = "H"		250			
			MFM = "L"		250			
Rising Time	T_r	C_L = 25pF			3			DW
Falling Time	T_f				2			
Window Width ("H" Level Width)	T_W	MIN = "L"	MFM = "H"		1		μs	
			MFM = "L"		2			
		MIN = "H"	MFM = "H"		2			
			MFM = "L"		4			
Rising Time	T_r	C_L = 25pF			3		ns	$\overline{RR}$
Falling Time	T_f				2			
"L" Level Width	T_{WL}	MIN = "L"	MFM = "H"		0.25		μs	
			MFM = "L"		0.5			
		MIN = "H"	MFM = "H"		0.5			
			MFM = "L"		1			
Slip Off from DW Center	T_D				10		ns	
"H" Level Width	T_{WH}			50				RD
External Clock Duty Ratio	D_{EXT}	f_{X1} = 8MHz/9.6MHz		40	50	60	%	X1

STANDARD EXTERNAL CIRCUITS (MB4107A)



NOTE: 1. C_3 (±5%), R_5 (±1%), otherwise C (±10%), R (±5%)

2. Since the 8-MHz internal and 8-MHz external clocks require precision of ±1%, a ceramic resonator can be used when WCK and CK do not require a high precision.

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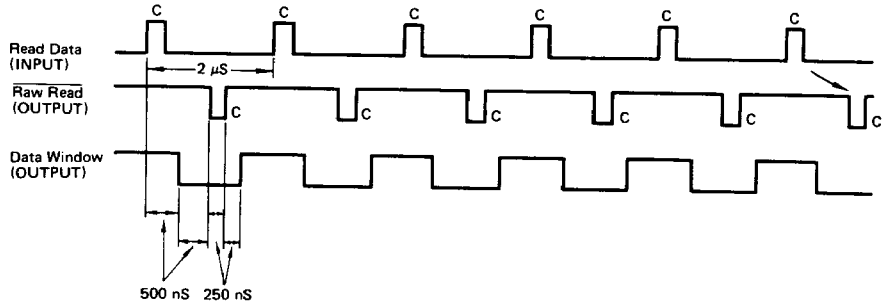
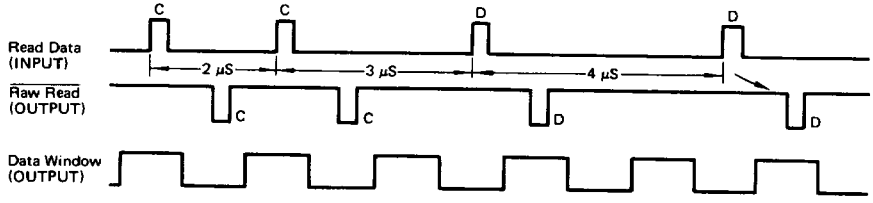
TIMING CHARTS

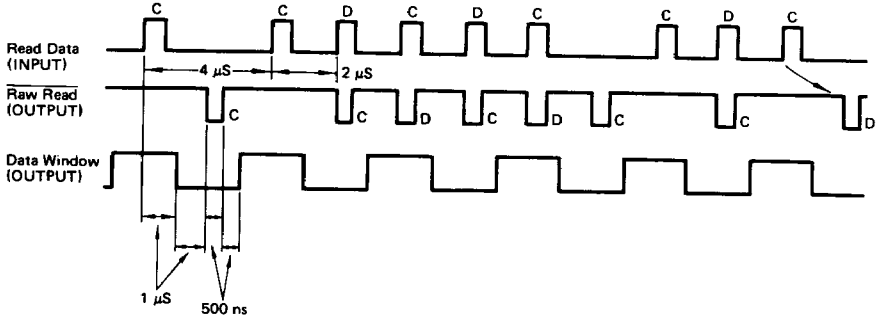
I 8 INCH, MFM, HIGH GAIN (SYNC FIELD)



II 8 INCH, MFM, LOW GAIN



III 8 INCH, FM, LOW GAIN.

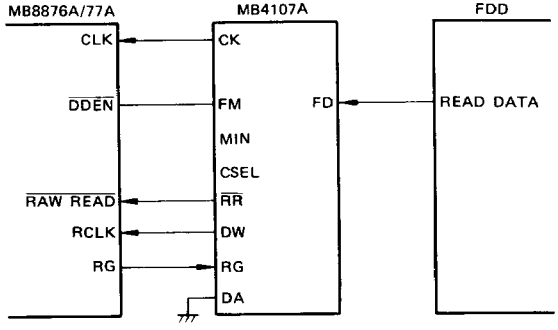


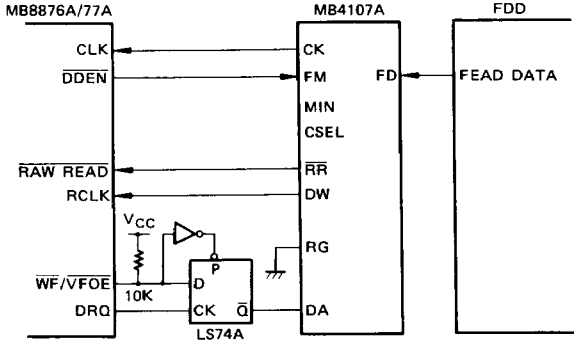
NOTES: 1. The above times are doubled for 5-inch floppy disks.
2. C = clock pulse, D = data pulse

STANDARD CONNECTION

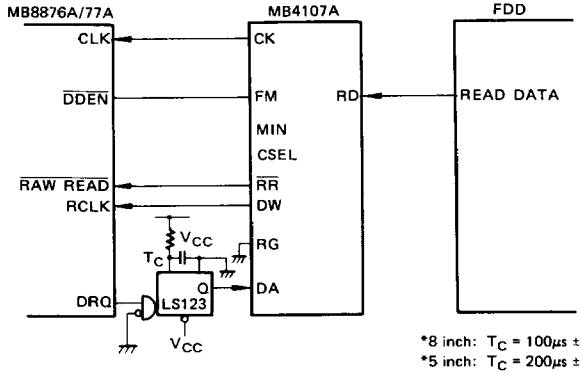
1. MB8876/77A

1-1) Read Gate





1-2) Data Request



*8 inch: T_C = 100μs ± 20%
*5 inch: T_C = 200μs ± 20%

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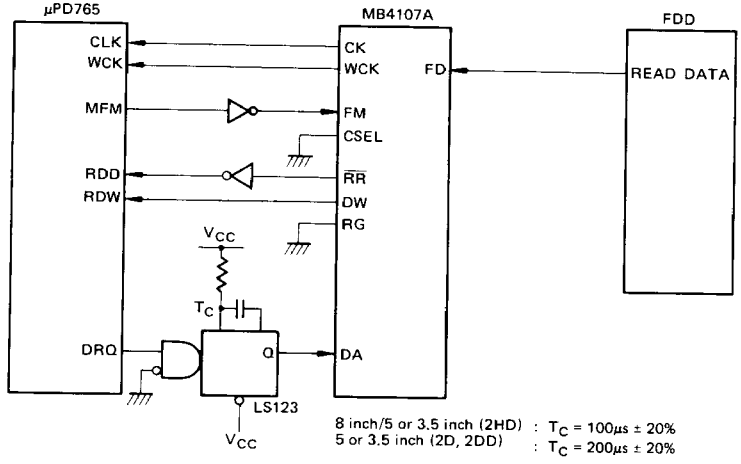
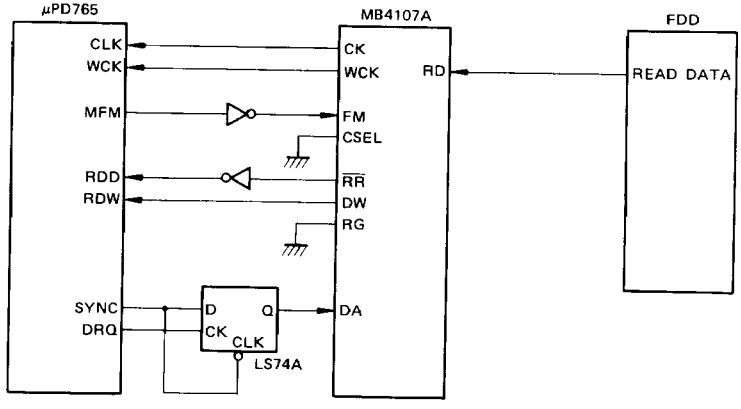
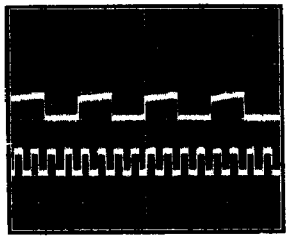
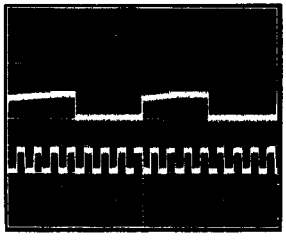
STANDARD CONNECTIONS (continued)

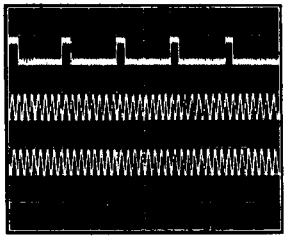
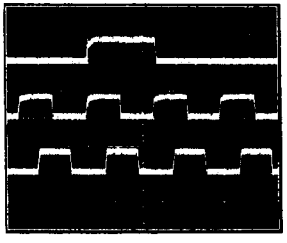
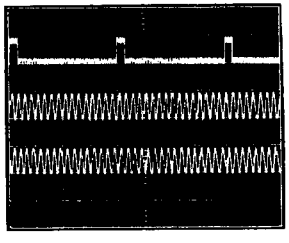
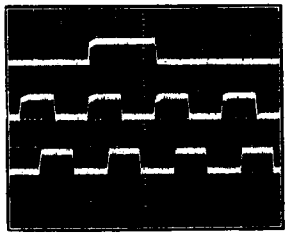
2. μPD765





CK, WCK TIMING (EXTERNAL CLOCK INPUT)

Mode	In/Output	Timing
CSEL = "H" MB8876A MB8877A STD MFM/FM	CK X1	
CSEL = "H" MB8876A MB8877A MIN MFM/FM	CK X1	

Mode	In/Output	Timing	Magnification
CSEL = "L" (μPD765) STD MFM	WCK CK X1		
CSEL = "L" (μPD765) STD FM	WCK CK X1		

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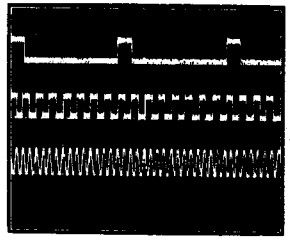
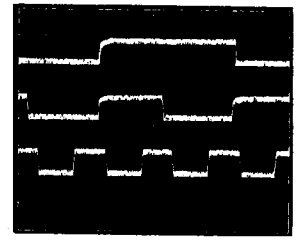
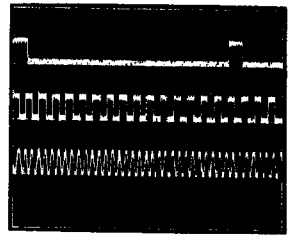
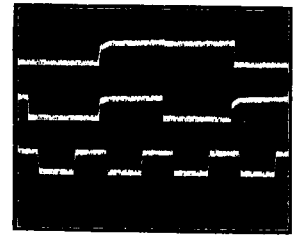
CK, WCK TIMING (EXTERNAL CLOCK INPUT) (continued)

Mode	In/Output	Timing	Magnification
CSEL = "L" (μPD765) MIN MFM	WCK CK X1		
CSEL = "L" (μPD765) MIN FM	WCK CK X1		

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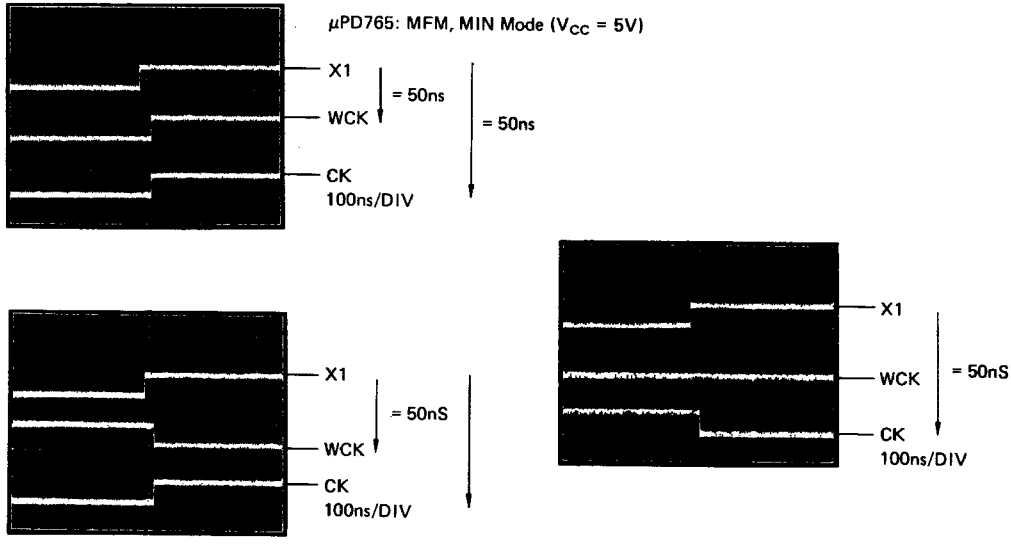
Delay of CW, WCK against input clock



TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 – f_{V10} vs. VAD

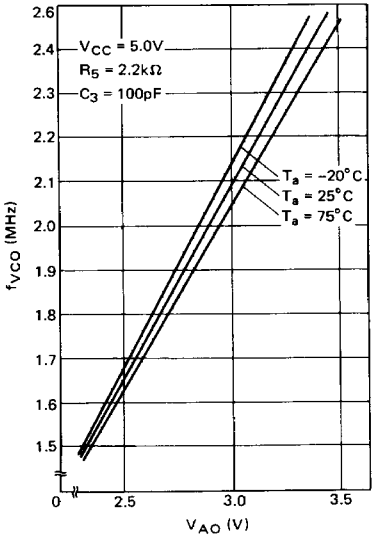


Fig. 2 – FREE RUN FREQUENCY vs. C_3

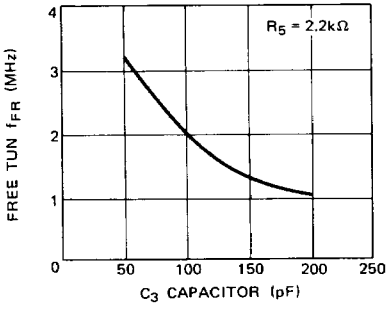


Fig. 3 – FREE RUN FREQUENCY vs. T_a

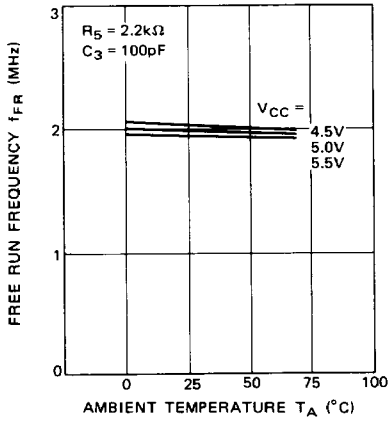
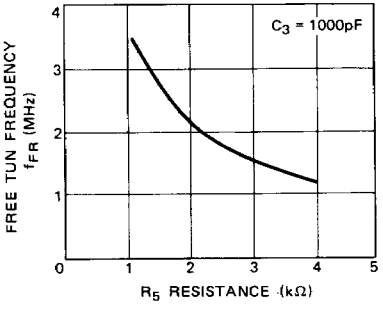


Fig. 4 – FREE RUN FREQUENCY vs. R_5



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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Fig. 5 – TIME MARGIN vs. T_a

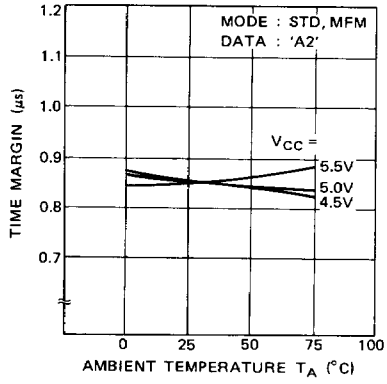


Fig. 6 – TIME MARGIN vs. FREE RUN FREQUENCY

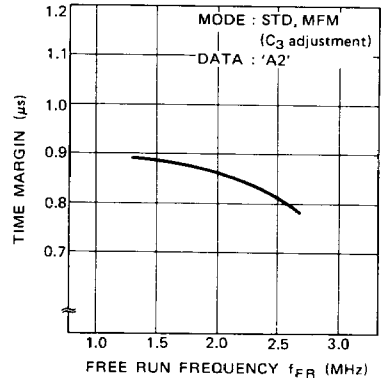
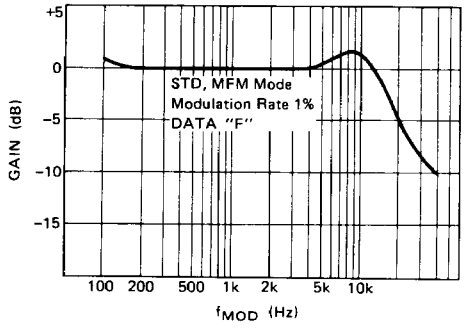


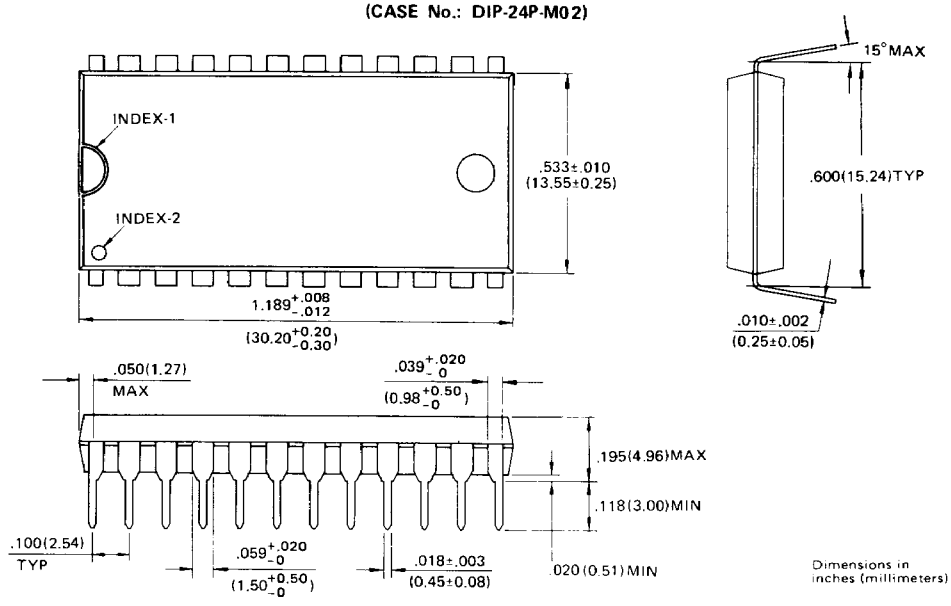
Fig. 7 – GAIN vs. f_{MOD}



6

PACKAGE DIMENSIONS

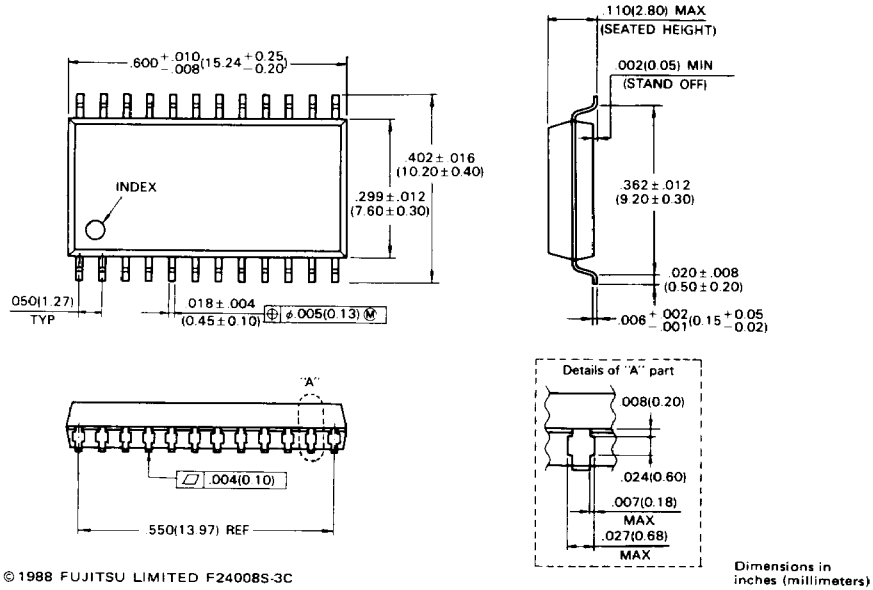
24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M02)



6

PACKAGE DIMENSIONS (continued)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)



Dimensions in
inches (millimeters)

6