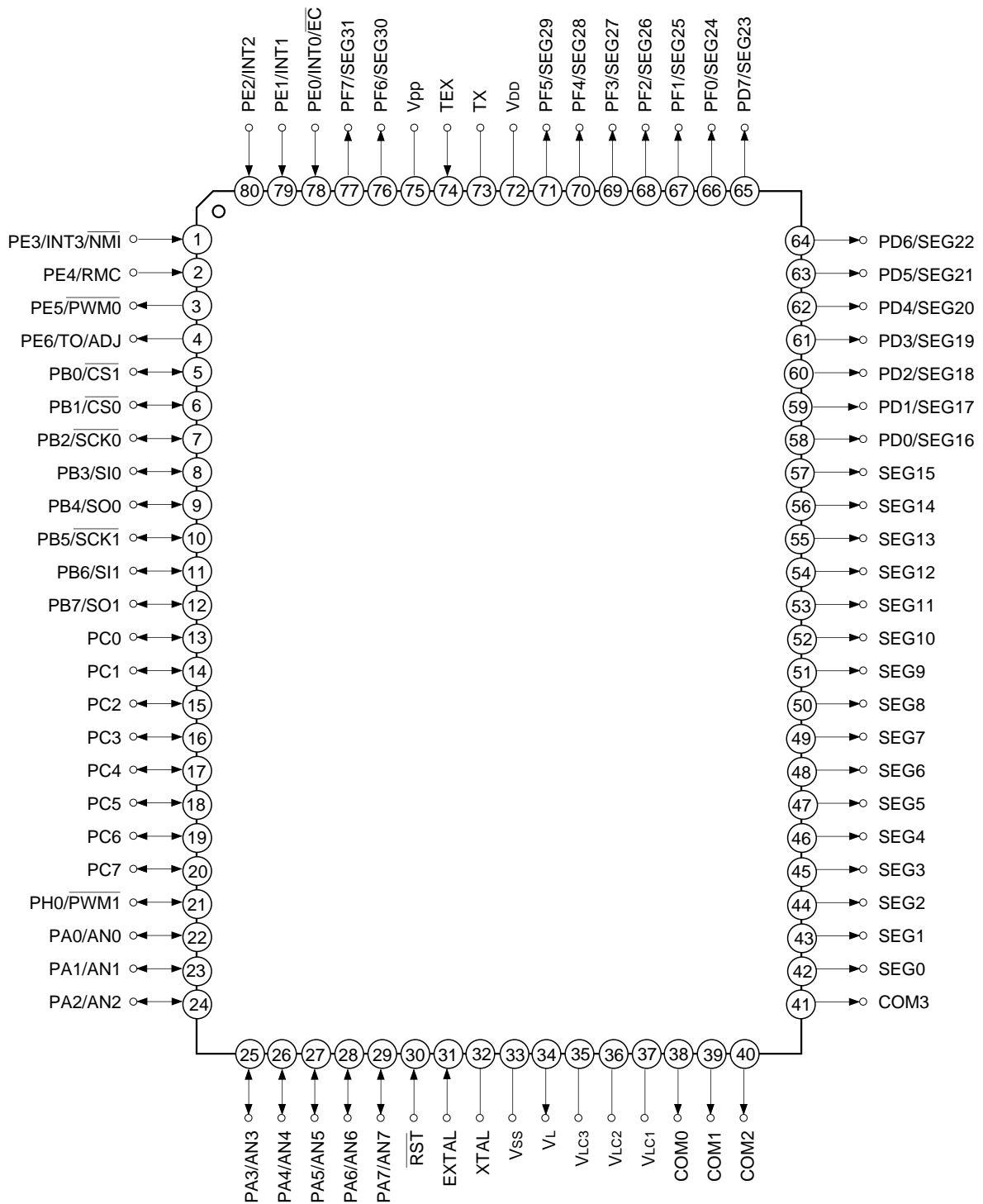


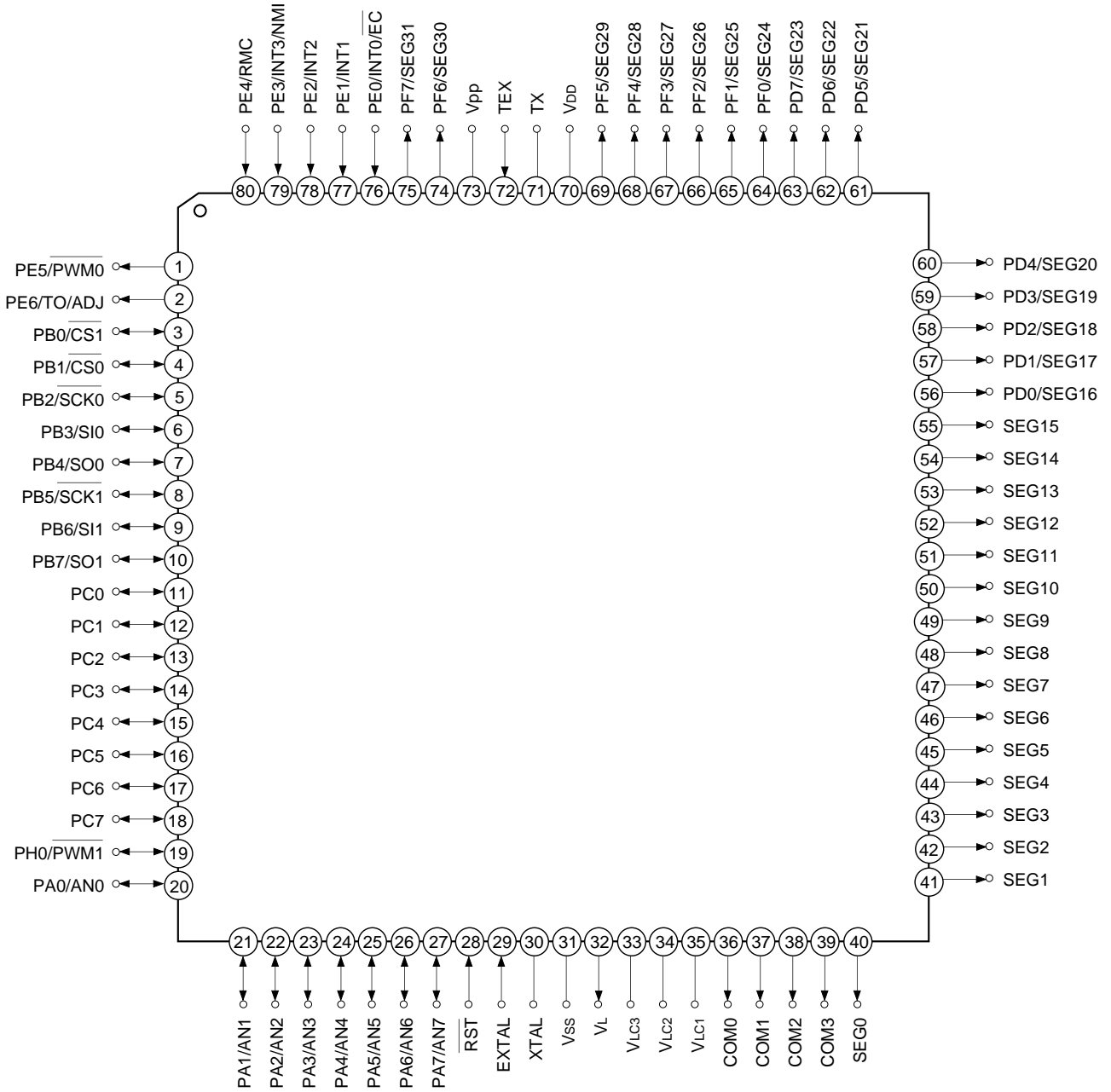
Block Diagram

Pin Assignment (Top View) CXP834P16 (QFP package)



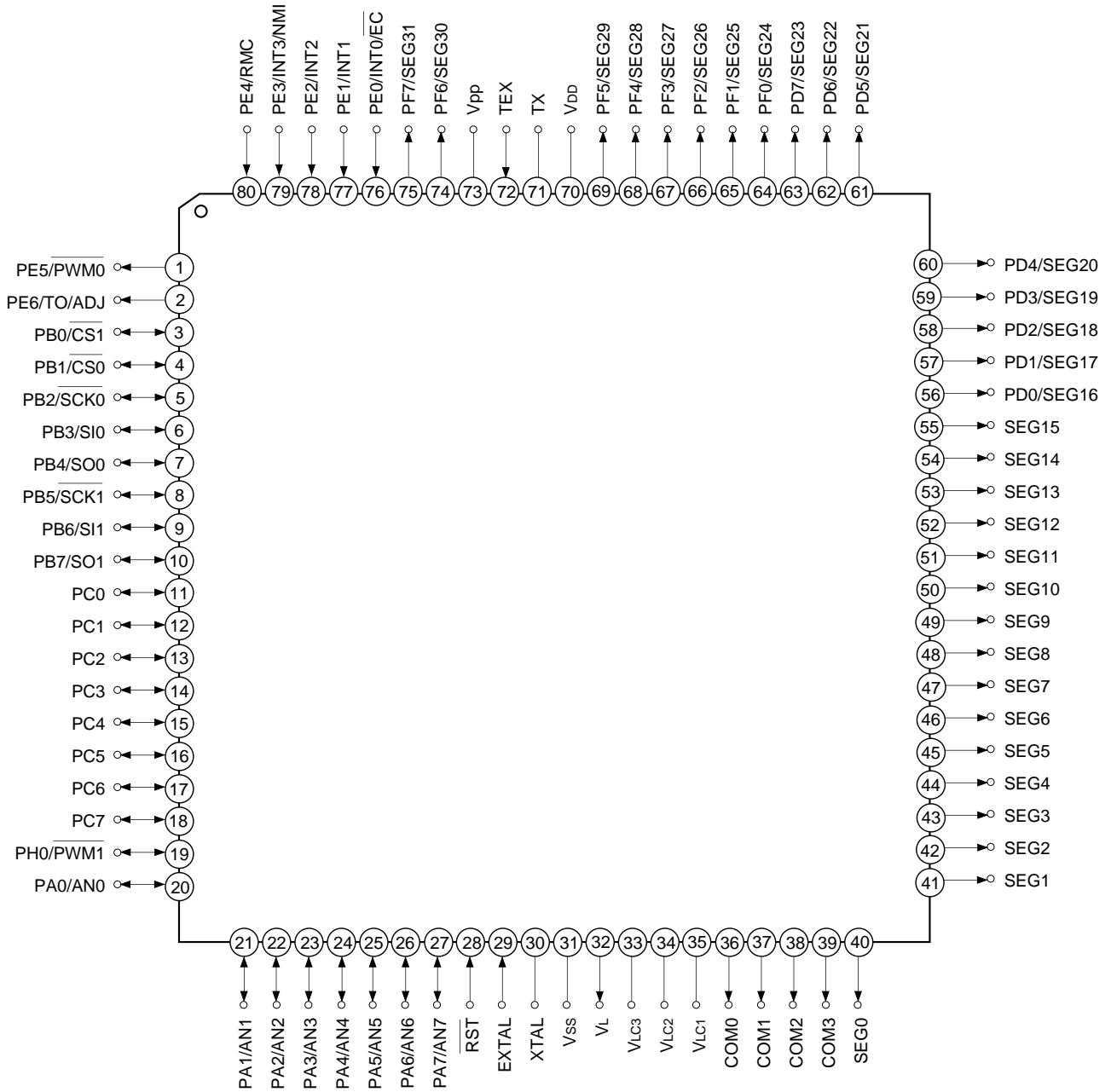
Note) Vpp (Pin 75) is always connected to VDD.

Pin Assignment (Top View) CXP834P16 (LQFP package)



Note) V_{pp} (Pin 73) is always connected to V_{DD}.

Pin Assignment (Top View) CXP834P17 (QFP package)



Note) V_{pp} (Pin 73) is always connected to V_{DD}.

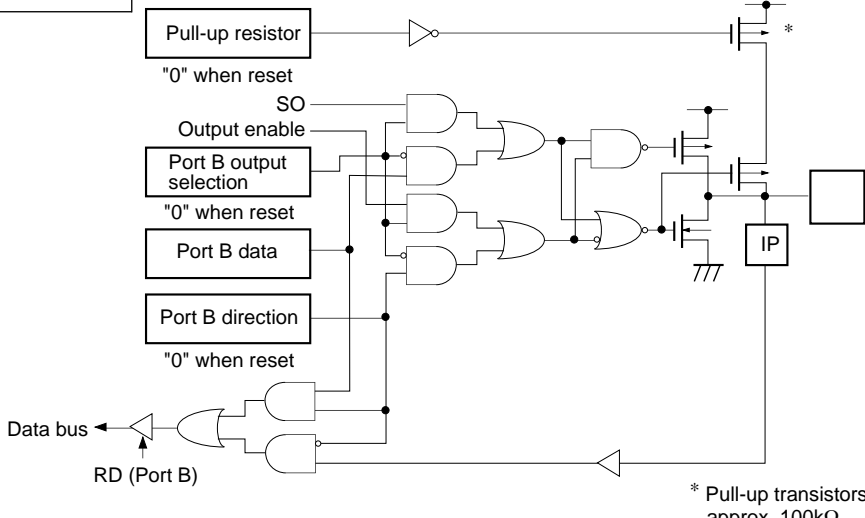
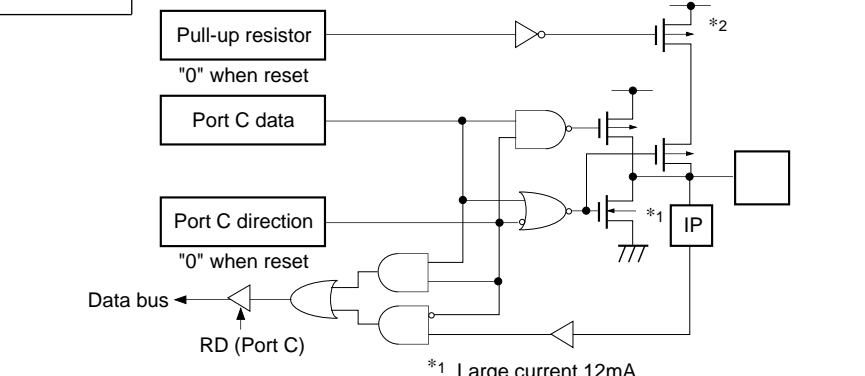
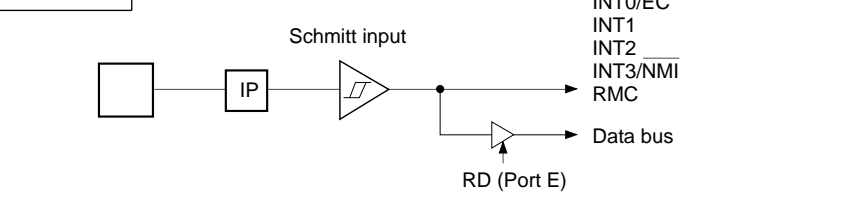
Pin Description

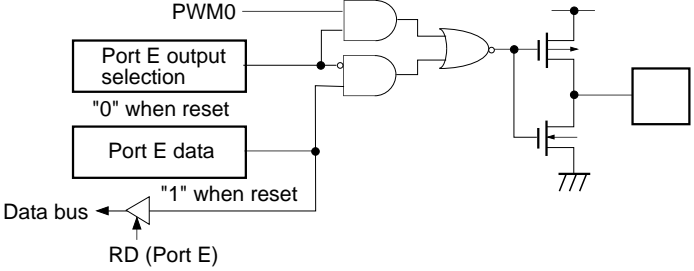
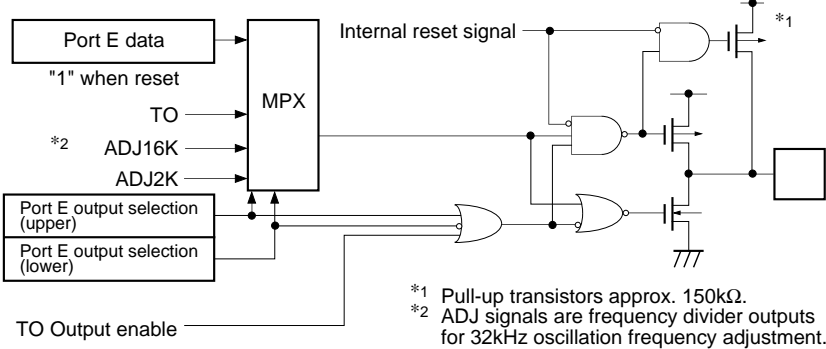
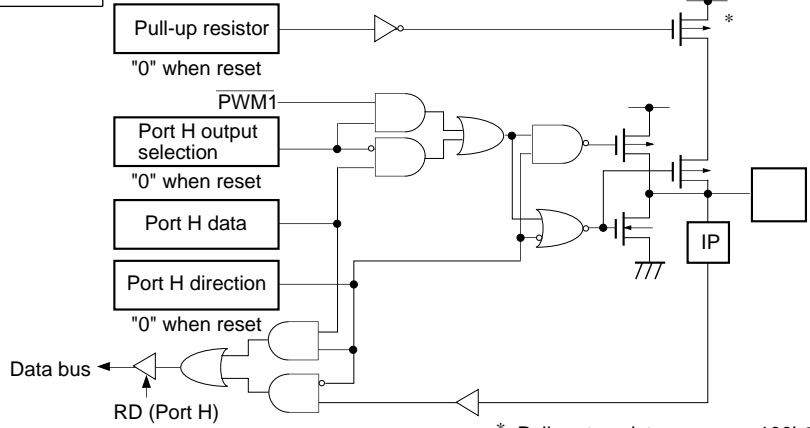
Symbol	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/ $\overline{CS1}$	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Chip select input for serial interface (CH1).
PB1/ $\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/ $\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/ $\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/INT0/ \overline{EC}	Input/Input/Input	(Port E) 7-bit port. Lower 5 bits are for inputs; upper 2 bits are for outputs. (7 pins)	External event inputs for timer/counter.
PE1/INT1	Input/Input		External interruption request input. (4 pins)
PE2/INT2	Input/Input		
PE3/INT3/ \overline{NMI}	Input/Input/Input		Non-maskable intrruption request input.
PE4/RMC	Input/Input		Remote control receiving circuit input.
PE5/ $\overline{PWM0}$	Output/Output		14-bit PWM output.
PE6/TO/ADJ	Output/Output/ Output		Rectangular wave output for 8-bit timer/counter and 32kHz oscillation frequency divider output.
PH0/ $\overline{PWM1}$	I/O/Output	(Port H) 1-bit I/O port. Incorporation of pull-up resistor can be set through the software. (1 pin)	8-bit PWM output.

Symbol	I/O	Functions	
PD0/SEG16 to PD7/SEG23	Output/Output	(Port D) 8-bit output port. (8 pins)	LCD segment signal output. (16 pins)
PF0/SEG24 to PF7/SEG31	Output/Output	(Port F) 8-bit output port. (8 pins)	
SEG0 to SEG15	Output	LCD segment signal output.	
COM0 to COM3	Output	LCD common signal output.	
V _{LC1} to V _{LC3}		LCD bias power supply.	
V _L	Output	Control pin to cut off the current flowing to external LCD bias resistor during standby.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock generation circuit. For usage as event counter, connect clock oscillation source to TEX, and leave TX open.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active, system reset.	
V _{pp}		Positive power supply for the on-chip programmable PROM; connect to V _{DD} for normal operation.	
V _{DD}		Positive power supply.	
V _{SS}		GND.	

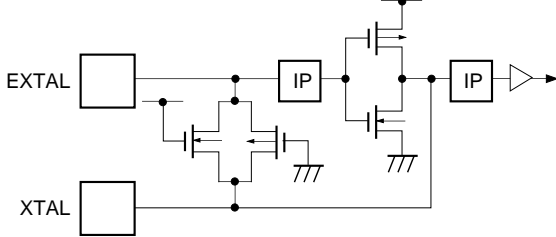
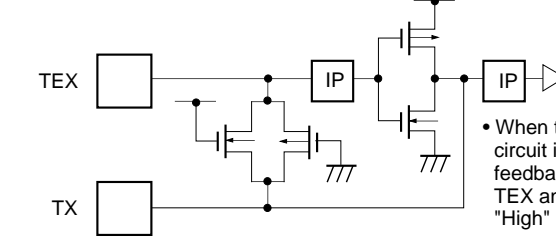
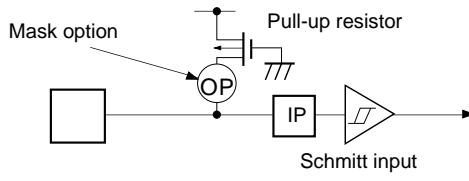
I/O Circuit Format for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>Pull-up resistor "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>A/D converter</p> <p>Input multiplexer</p> <p>IP Input protection circuit</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB0/$\overline{\text{CS1}}$ PB1/$\overline{\text{CS0}}$ PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p> <p>Pull-up resistor "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>$\overline{\text{CS1}}$ $\overline{\text{CS0}}$ SI0 SI1</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB2/$\overline{\text{SCK0}}$ PB5/$\overline{\text{SCK1}}$</p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistor "0" when reset</p> <p>$\overline{\text{SCK OUT}}$ Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>SCK in</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0 PB7/SO1</p> <p>2 pins</p>	<p>Port B</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PC0 to PC7</p> <p>8 pins</p>	<p>Port C</p>  <p>*1 Large current 12mA *2 Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PE0/INT0/\overline{EC} PE1/INT1 PE2/INT2 PE3/INT3/\overline{NMI} PE4/RMC</p> <p>5 pins</p>	<p>Port E</p>  <p>RD (Port E)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE5/PWM0</p> <p>1 pin</p>	<p>Port E</p> 	<p>High level</p>
<p>PE6/TO/ADJ</p> <p>1 pin</p>	<p>Port E</p>  <p>*1 Pull-up transistors approx. 150kΩ. *2 ADJ signals are frequency divider outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p>	<p>High level with approx. 150kΩ resistor when reset</p>
<p>PH0/PWM1</p> <p>1 pin</p>	<p>Port H</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format		When reset
<p>PD0 to PD7 PF0 to PF7</p> <p>24 pins</p>	<p>Port D Port F</p>		<p>Segment output (V_{DD} level)</p>
<p>SEG0 to SEG15</p> <p>16 pins</p>	<p>Segment</p>		<p>V_{DD} level</p>
<p>COM0 to COM3</p> <p>4 pins</p>	<p>Common</p>		<p>V_{DD} level</p>
<p>V_L</p> <p>1 pin</p>			<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop, and XTAL becomes "High" level. 	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed and TEX and TX become "Low" level and "High" level respectively. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Mask option</p> <p>Pull-up resistor</p> <p>Schmitt input</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS}=0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	V _{pp}	-0.3 to +13.0	V	Incorporated PROM
LCD bias voltage	V _{LC1} , V _{LC2} , V _{LC3}	-0.3 to +7.0*1	V	
Input voltage	V _{IN}	-0.3 to +7.0*1	V	
Output voltage	V _{OUT}	-0.3 to +7.0*1	V	
High level output current	I _{OH}	-5	mA	Output (value per pin)
High level total output current	∑I _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	All pins excluding large current output (value per pin)
	I _{OLC}	20	mA	Large current outputs (value per pin *2)
Low level total output current	∑I _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	-10 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP-80P-L01
		380	mW	LQFP-80P-L01
		380	mW	QFP-80P-L03

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The large current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS}=0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	High-speed mode guaranteed operation range* ¹
		3.5	5.5		Low-speed mode guaranteed operation range* ¹
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
	V _{PP}	V _{PP} = V _{DD}		V	* ⁶
LCD bias voltage	V _{LC1}	V _{SS}	V _{DD}	V	LCD power supply range* ⁵
	V _{LC2}				
	V _{LC3}				
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	* ²
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input* ³
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL * ⁴
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	* ²
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input* ³
	V _{ILEX}	-0.3	0.4	V	EXTAL * ⁴
Operating temperature	T _{opr}	-10	+75	°C	

*¹ High-speed mode is 1/2 frequency divider clock selection; low-speed mode is 1/16 frequency divider clock selection.

*² Value for each pin of normal input ports (PA, PB4, PB7, PC and PH0).

*³ Value of the following pins: \overline{RST} , $\overline{CS0}$, $\overline{CS1}$, SI0, SI1, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC}/INT0$, INT1, INT2, $\overline{NMI}/INT3$, and RMC.

*⁴ Specifies only during external clock input.

*⁵ Optimal values are determined by LCD used.

*⁶ V_{PP} and V_{DD} should be set to the same voltage.

Electrical Characteristics

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA, PB, PC, PD*1, PE5, PE6, PF, PH0, VL (VOL only)	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output voltage	VOL	PA, PB, PC, PD*1, PE5, PE6, PF, PH0, VL (VOL only)	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
		PC	VDD = 4.5V, IOL = 12.0mA			1.5	V
Input current	IiHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	V
	IiLE		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IiHT	TEX	VDD = 5.5V, VIH = 5.5V	0.1		10	μA
	IiLT			-0.1		-10	μA
	IiLR	RST*2	VDD = 5.5V, VIL = 0.4V		-1.5	-400	μA
	IiL	PA to PC*3, PH*3, PE0 to PE4, RST*2				-45	μA
	IiH		VDD = 4.5V, VIH = 4.0V	-2.78			μA
I/O leakage current	IIZ		VDD = 5.5V, VI = 0, 5.5V			±10	μA
Common output impedance	R _{COM}	COM0 to COM3	VDD = 5V, VLC1 = 3.75V		3	5	kΩ
Segment output impedance	R _{SEG}	SEG0 to SEG15, SEG16 to SEG31*1	VLC2 = 2.5V VLC3 = 1.25V		5	15	kΩ
Supply current*4	IDD1	VDD	High-speed mode operation (1/2 frequency divider clock)		18	40	mA
			VDD = 5.5V, 10MHz crystal oscillation (C1 = C2 = 15pF)				
	IDD2		VDD = 3V, 32kHz crystal oscillation (C1 = C2 = 47pF)		400	1000	μA
	IDDS1		SLEEP mode		1.1	8	mA
			VDD = 5.5V, 10MHz crystal oscillation (C1 = C2 = 15pF)				
	IDDS2		VDD = 3V, 32kHz crystal oscillation (C1 = C2 = 47pF)		9	30	μA
IDDS3	STOP mode				30	μA	
			VDD = 5.5V, termination of 10MHz and 32kHz crystal oscillation				

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C _{IN}	PA to PC, PE1 to PE4, EXTAL, TEX, RST	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 Common pins of PD0/SEG16 to PD7/SEG23, PF0/SEG24, PF7/SEG31, PD and PF are the case when the common pin is selected as port; SEG16 to SEG31 is when the common pin is selected as segment output.

*2 RST specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*3 PA to PC, and PH0 specify the input current when pull-up resistor has been selected; leakage current when no resistor has been selected. (PE0 to PE4 specify the leakage current.)

*4 When all output pins are left open.

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t _{XL} , t _{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise and fall time	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t _{EH} , t _{EL}	\overline{EC}	Fig. 3	t _{sys} +50*			ns
Event count input clock rise and fall time	t _{ER} , t _{EF}	\overline{EC}	Fig. 3			20	ms
System clock frequency	fc	TEX TX	V _{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10			μs
Event count input clock rise and fall time	t _{TR} , t _{TF}	TEX	Fig. 3			20	ms

* t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FE_H).

t_{sys} (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Fig. 1. Clock timing

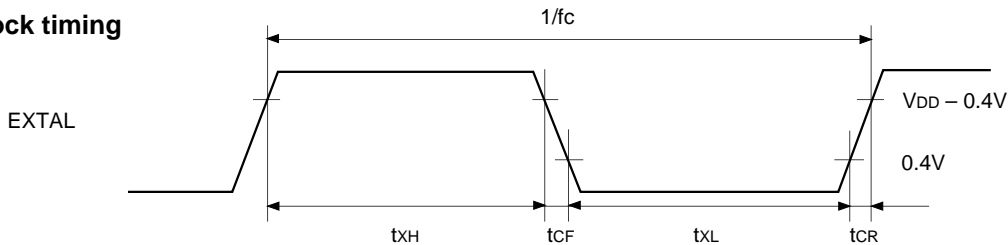


Fig. 2. Clock applied conditions

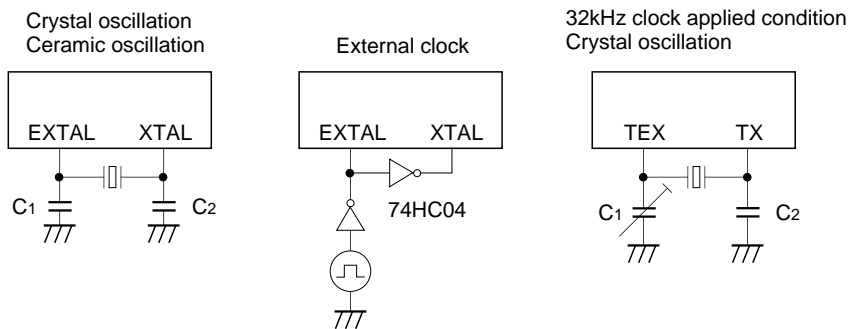
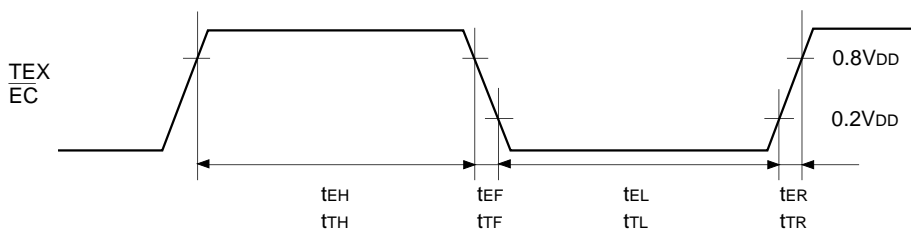


Fig. 3. Event count clock timing



(2) Serial transfer

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

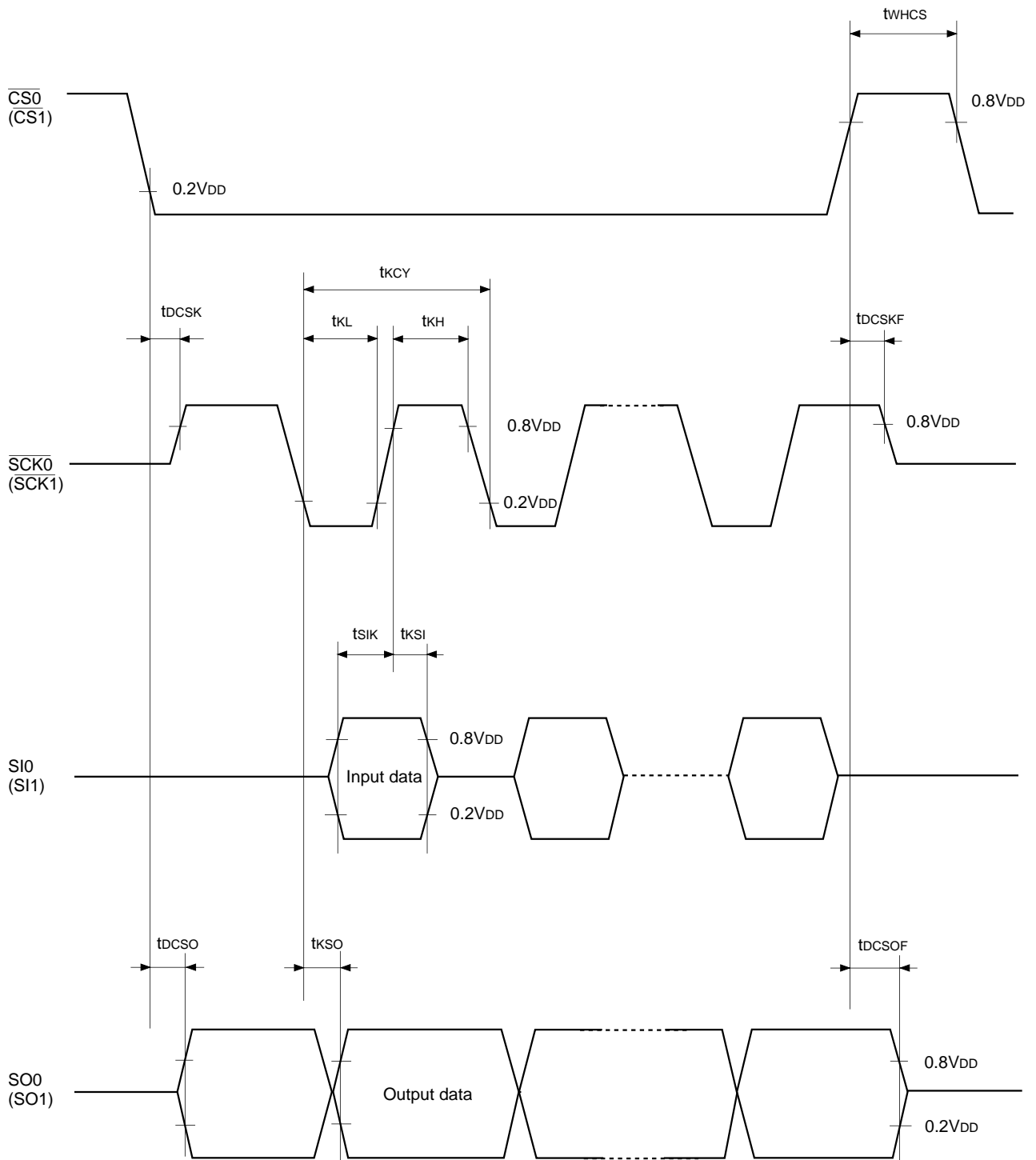
Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ ($\overline{CS1} \downarrow \rightarrow \overline{SCK1}$) delay time	t _{D_{CSK}}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ ($\overline{CS1} \uparrow \rightarrow \overline{SCK1}$) floating delay time	t _{D_{CSKF}}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		t _{sys} + 200	ns
$\overline{CS0} \downarrow \rightarrow \overline{SO0}$ ($\overline{CS1} \downarrow \rightarrow \overline{SO1}$) delay time	t _{D_{CSO}}	SO0 (SO1)	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SO0}$ ($\overline{CS1} \uparrow \rightarrow \overline{SO1}$) floating delay time	t _{D_{CSOF}}	SO0 (SO1)	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0}$ ($\overline{CS1}$) high level width	t _{WHCS}	$\overline{CS0}$ ($\overline{CS1}$)	Chip select transfer mode	t _{sys} + 200		ns
$\overline{SCK0}$ ($\overline{SCK1}$) cycle time	t _{KCY}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ ($\overline{SCK1}$) high and low level widths	t _{KH} t _{KL}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI0 (SI1) input setup time (for $\overline{SCK0} \uparrow$ ($\overline{SCK1} \uparrow$))	t _{SIK}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	100		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	200		ns
SI0 (SI1) input hold time (for $\overline{SCK0} \uparrow$ ($\overline{SCK1} \uparrow$))	t _{KSI}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	t _{sys} + 200		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow \overline{SO0}$ ($\overline{SCK1} \downarrow \rightarrow \overline{SO1}$) delay time	t _{KSO}	SO0 (SO1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode		t _{sys} + 200	ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEH).

t_{sys} (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ ($\overline{SCK1}$) output mode, SO0 (SO1) output delay time is 50pF + 1TTL.

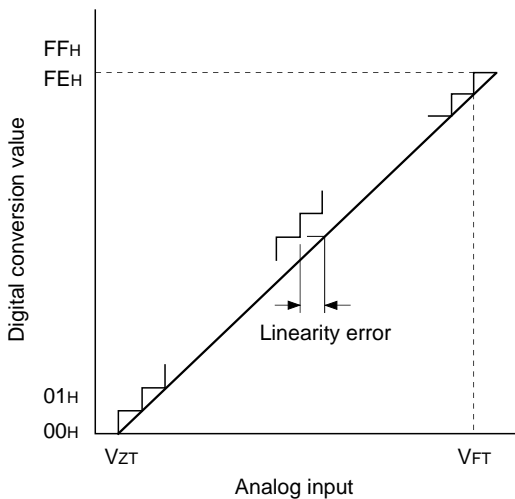
Fig. 4. Serial transfer CH0 timing



(3) A/D converter characteristics (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, AVREF = 4.0 to AVDD, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						±3	LSB
Zero transition voltage	VZT*1		Ta = 25°C VDD = 5.0V VSS = 0V	-10	10	70	mV
Full-scale transition voltage	VFT*2			4910	4970	5030	mV
Conversion time	tCONV			160/fADC*3			µs
Sampling time	tSAMP			12/fADC*3			µs
Analog input voltage	VIAN	AN0 to AN7		0		VDD + 0.3	V

Fig. 5. Definition of A/D converter terms



*1 VZT: Value at which the digital conversion value changes from 00H to 01H and vice versa.

*2 VFT: Value at which the digital conversion value changes from FEH to FFH and vice versa.

*3 fADC indicates the below values due to the contents of bit 6 (CK3) of the A/D control register (ADC: 00F9H) and bit 7 (PCK1) and bit 6 (PCK0) of the clock control register (CLC: 00FEH)

PCK1, PCK0 \ CKS	0 (φ/2 selection)	0 (φ selection)
	00 (φ = fEX/2)	fADC = fc/2
01 (φ = fEX/4)	fADC = fc/4	fADC = fc/2
11 (φ = fEX/16)	fADC = fc/16	fADC = fc/8

(4) Interruption, reset input (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t _{IH} t _{IL}	INT0 INT1 INT2 $\overline{\text{NMI/INT3}}$		1		μs
Reset input low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig 6. Interruption input timing

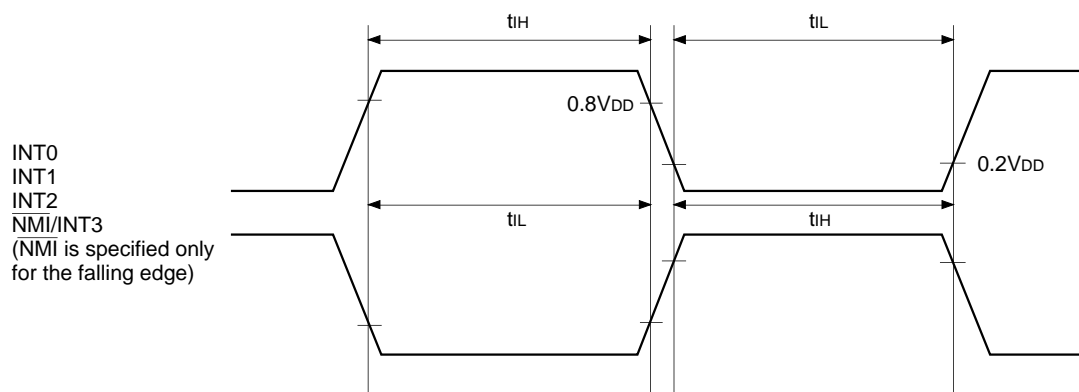
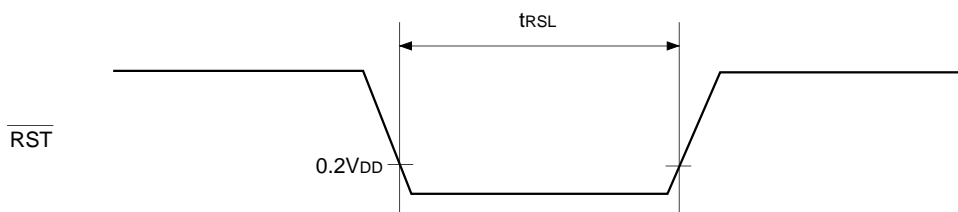
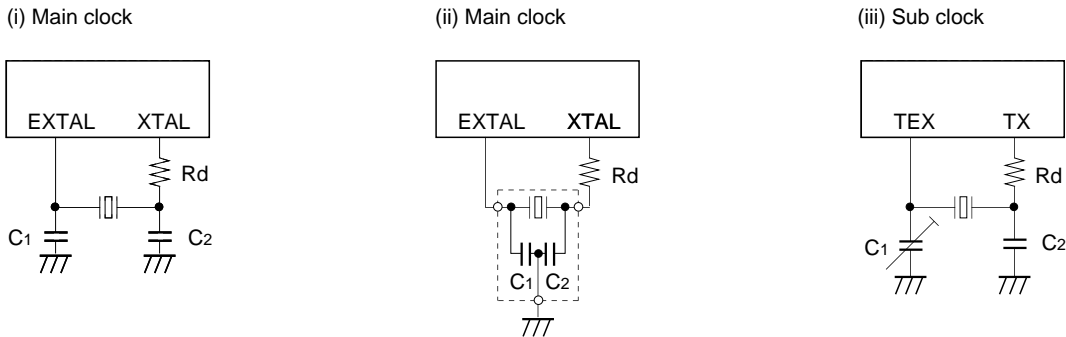


Fig. 7. $\overline{\text{RST}}$ input timing



Appendix

Fig. 8. SPC700 Series recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MG	8.00				
	CSA10.0MT	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.00MTW*	10.00				
RIVER ELETEC CO., LTD.	HC-49/U03	4.19	15	15	2.2k	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	22	22	560	
		8.00	18	18	0	
		10.00				

Models with an asterisk (*) have the built-in ground capacitance (C1, C2).

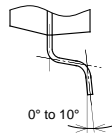
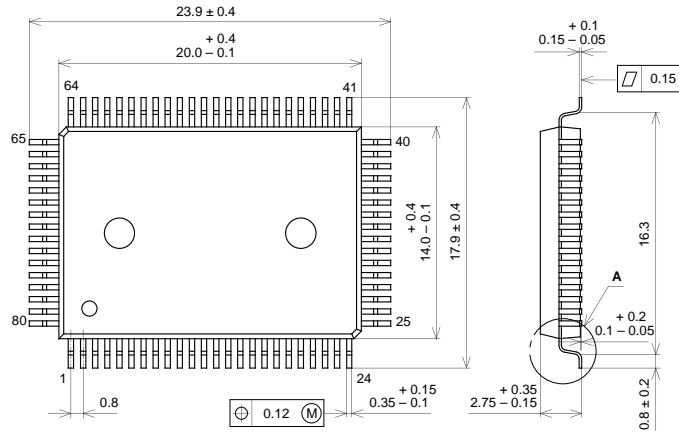
Product List

Optional	Mask				PROM		
	CXP83412	CXP83416	CXP83413	CXP83417	CXP834P16Q-1-□□□	CXP834P16R-1-□□□	CXP834P17Q-1-□□□
Package	80-pin plastic QFP/LQFP		80-pin plastic QFP (0.65mm pitch)		80-pin plastic QFP	80-pin plastic LQFP	80-pin plastic QFP (0.65mm pitch)
ROM capacity	12K bytes	16K bytes	12K bytes	16K bytes	PROM 16K bytes		
Reset pin pull-up resistance	Existent/Non-existent				Existent		

Package Outline Unit: mm

CXP834P16

80PIN QFP (PLASTIC)



DETAIL A

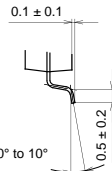
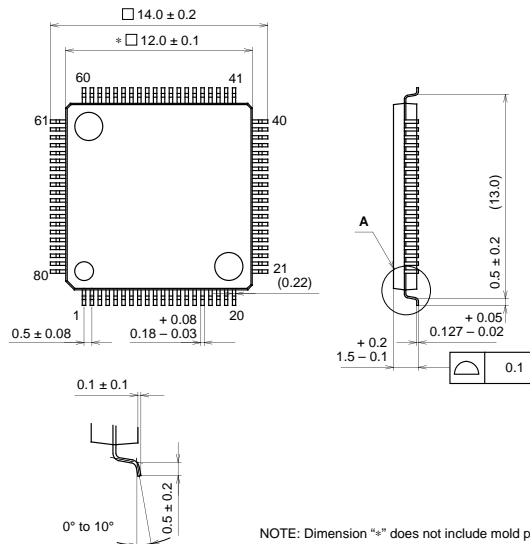
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g

SONY CODE	QFP-80P-L01
EIAJ CODE	+QFP080-P-1420-A
JEDEC CODE	—

CXP834P16

80PIN LQFP (PLASTIC)



DETAIL A

NOTE: Dimension "*" does not include mold protrusion.

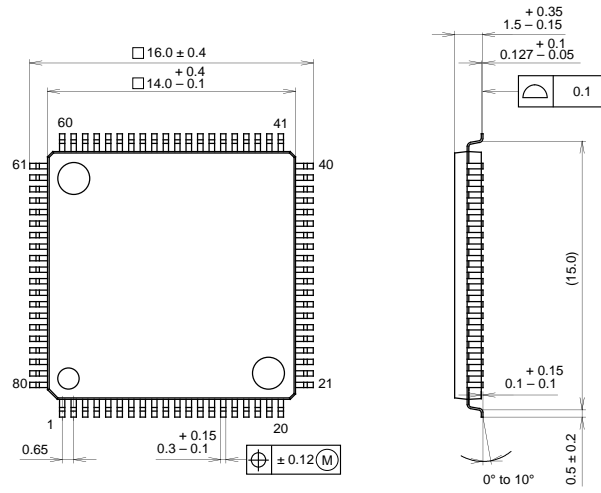
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g

SONY CODE	LQFP-80P-L01
EIAJ CODE	+QFP080-P-1212-A
JEDEC CODE	—

CXP834P17

80PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-80P-L03
EIAJ CODE	LQFP080-P-1414
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.6g