ANALOG DEVICES

T-51-07-01 **LC²MOS**

20-Bit Data Acquisition System

AD79024

FEATURES

20-Bit Sigma-Delta ADC
- **Dynamic Range of 105 dB (150 Hz Input)**
- **±0.0015% Integral Nonlinearity (150 Hz Input)**

On-Chip Low-Pass Digital Filter
- **Cut-Off Programmable from 300 Hz to 18.75 Hz**
- **Linear Phase Response**

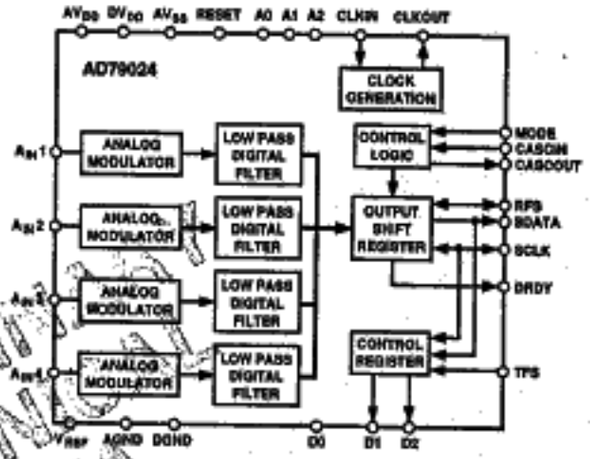
Five Line Serial I/O
Easy Interface to DSPs and Microcomputers
Software Control of Filter Cut-Off
±5 V Supply
Low Power Operation: 50 mW

APPLICATIONS

Biomedical Data Acquisition Systems
- **ECG Machines**
- **EEG Machines**

Process Control Systems
High Accuracy Measurement Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD79024 is a Signal Processing Block for Data Acquisition Systems. It is particularly suitable for biomedical applications like ECG and EEG machines. The device is capable of processing 4 channels with bandwidths of up to 300 Hz. Resolution is 20 bits, and the usable dynamic range varies from 115 dB with an input bandwidth of 18.75 Hz to 90 dB with an input bandwidth of 300 Hz.

The required system low-pass filtering is inherent in the sigma delta technique. This eliminates front-end filtering.

Three address pins program the device address. This allows a data acquisition system with up to 32 channels to be set up in a simple fashion. The output word from the device contains 32 bits of data. One bit is determined by the state of the D0 input and may be used with an external Pacemaker Detect Circuit to indicate that the output word is invalid because of the presence of a pacemaker pulse. There are 20 bits of data. Two bits contain the channel address, and 3 bits are the device address. Thus, each channel in a 32-channel system would have a discrete 5-bit address. The device also has a CASCOUT pin and a CASCIN pin which allow simple networking of multiple devices.

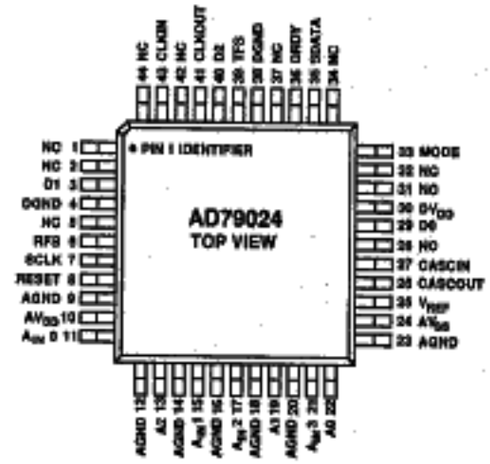
The on-chip Control Register is programmed using the SCLK, SDATA and TFS pins. Three bits of the Control Register set the Digital Filter Cut-Off Frequency for the device. Selectable frequencies are 300 Hz, 150 Hz, 75 Hz, 37.5 Hz and 18.75 Hz. A further 2 bits appear as outputs D1 and D2 and can be used for controlling calibration at the front end. The device is available in a 44-pin plastic QFP (Quad Flat Pack) package.

The AD79024 is fabricated in Analog Devices' Linear Compatible CMOS process (LC²MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

7

PIN CONFIGURATION

Plastic QFP



NOTE: PIN 16—AGND IS THE PRIMARY AGND TO THE PART. SECONDARY AGND PINS ARE USED TO ISOLATE THE ANALOG INPUT PINS. NO PINS MAY BE CONNECTED TO EITHER DIGITAL SUPPLY OR LEFT UNCONNECTED.

AD79024—SPECIFICATIONS[1, 2] (f_{CLKIN} = 4 MHz, AV_{DD} = +5 V ± 5%; AV_{SS} = −5 V ± 5%; AGND = DGND = 0 V; V_{REF} = 2.5 V; Filter Cut-Off = 150 Hz; A_{IN} = ±2.5 V, 30 Hz Sine Wave; A_{IN} Source Resistance = 750 Ω[2] with 1 nF to AGND at each A_{IN}. T_A = T_{MIN} to T_{MAX}, unless otherwise stated.)

Parameter	Limit @ T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution	20	Bits	
Integral Linearity Error	0.0015	% FSR typ	Guaranteed No Missed Codes to 20 Bits[3]
	0.003	% FSR max	
Gain Error	1	% FSR max	
Gain Match Between Channels	0.05	% FSR max	
Offset Error	1	% FSR max	
Offset Match Between Channels	0.5	% FSR max	
Noise	See Table I		
DYNAMIC PERFORMANCE			
Sampling Rate	300	kHz	
Output Update Rate	500	Hz	
Filter Cut-Off Frequency	See Table I		
Settling Time	See Table I		
Usable Dynamic Range[4]	See Table I		
Total Harmonic Distortion	−96	dB typ	
	−48	dB typ	A_{IN} = ±10 mV pk-pk
Intermodulation Distortion	100	dB typ	
	52	dB typ	A_{IN} = ±10 mV pk-pk
Absolute Group Delay[3]	10	ms max	
Differential Group Delay[3]	10	ns max	
ANALOG INPUT			
Input Range	±2.5	Volts	
Input Capacitance	10	pF typ	
Input Bias Current	1	nA typ	
LOGIC INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	2.4	V min	$\|I_{OUT}\| \leq 40$ μA
V_{OL}, Output Low Voltage	0.4	V max	$\|I_{OUT}\| \leq 1.6$ mA
POWER SUPPLIES			
Reference Input	2.4/3.1	V min/V max	
AV_{DD}	4.75/5.25	V min/V max	
DV_{DD}	4.75/5.25	V min/V max	
AV_{SS}	−4.75/−5.25	V min/V max	
I_{DD}	5	mA max	
I_{SS}	5	mA max	
Power Supply Rejection[5]	−70	dB typ	

NOTES
[1]Operating Temperature Range −40°C to +85°C.
[2]The A_{IN} pins present a very high impedance dynamic load which varies with clock frequency.
[3]Guaranteed by design and characterization.
[4]Usable Dynamic Range is guaranteed by measuring noise and relating this to the Full-Scale Input Range.
[5]100 mV pk-pk, 120 Hz sine wave applied to each supply.
Specifications subject to change without notice.

Table I. Usable Dynamic Range, RMS Noise and Filter Settling Time vs. Filter Bandwidth

Programmed Bandwidth (Hz)	Usable Dynamic Range (dB)	RMS Noise (μV)	Filter Settling Time to ±0.0007% FS (ms)
300	90	56	5
150	108	7	10
75	115	3	20
37.5	115	3	40
18.75	115	3	80

NOTE
Usable Dynamic Range is defined as the ratio of the rms full-scale reading (sine wave input) to the rms noise of the converter.

Timing Characteristics[1, 2] (AV_{DD} = DV_{DD} = +5 V ± 5%; AV_{SS} = −5 V ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 4 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD}; unless otherwise stated.)

Parameter	Limit @ T_{MIN}, T_{MAX}	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master Clock Frequency: Internal Gate Oscillator
	4	MHz max	
	400	kHz min	Master Clock Frequency: Externally Supplied
	4	MHz max	
t_R[5]	50	ns max	Digital Output Rise Time; Typically 20 ns
t_F[5]	50	ns max	Digital Output Fall Time; Typically 20 ns
Control Register Timing			
t_1	250	ns min	SCLK Period
t_2	77	ns min	SCLK Width
t_3	30	ns min	TFS Setup Time
t_4	20	ns min	SDATA Setup Time
t_5	10	ns min	SDATA Hold Time
t_6	20	ns min	TFS Hold Time
Master Mode Timing			
t_7	200	ns min	CASCIN Pulse Width
t_8[6]	25	ns max	CASCIN High to SCLK Valid Delay
t_9	500	ns min	SCLK Period
t_{10}	150	ns min	SCLK Width
t_{11}	25	ns max	SCLK High to RFS High Delay
t_{12}[7]	0	ns min	RFS Hold After SCLK High
t_{13}[7]	100	ns max	SCLK High to SDATA Valid
t_{14}[8]	250	ns max	SCLK Falling Edge to Hi-Z Delay
t_{15}	25	ns max	SCLK Hi-Z to CASCOUT High Delay
t_{16}	500	ns min	CASCOUT Pulse Width
Slave Mode Timing			
t_7	200	ns min	CASCIN Pulse Width
t_{16}	500	ns min	CASCOUT Pulse Width
t_{17}	100	ns min	CASCIN High to SCLK High Setup Time
t_{18}	250	ns min	SCLK Period
t_{19}	77	ns min	SCLK Width
t_{20}	50	ns min	RFS to SCLK High Setup Time
t_{21}	10	ns min	RFS Hold Time After SCLK Low
t_{22}[7]	100	ns max	SCLK High to SDATA Valid
t_{23}[8]	250	ns max	SCLK Falling Edge to Hi-Z Delay.
t_{24}	50	ns max	SCLK Low to CASCOUT High Delay

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 1 to 6.
[3]CLKIN Duty Cycle range is 20% to 80%.
[4]The AD79024 is production tested with f_{CLKIN} at 4 MHz. It is guaranteed by characterization to operate at 400 kHz.
[5]Specified using 10% and 90% points on waveform of interest.
[6]If DRDY is high when a rising edge occurs on CASCIN, the rising edge will not be recognized until DRDY goes low to indicate that the output register can be read.
[7]t_{13} and t_{22} are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[8]t_{14} and t_{23} are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

7

T-51-07-01

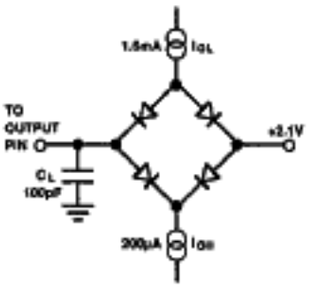


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

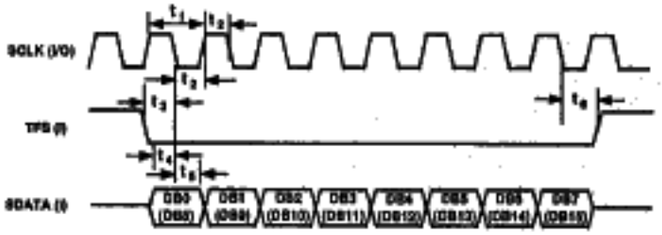


Figure 2. Control Register Timing Diagram

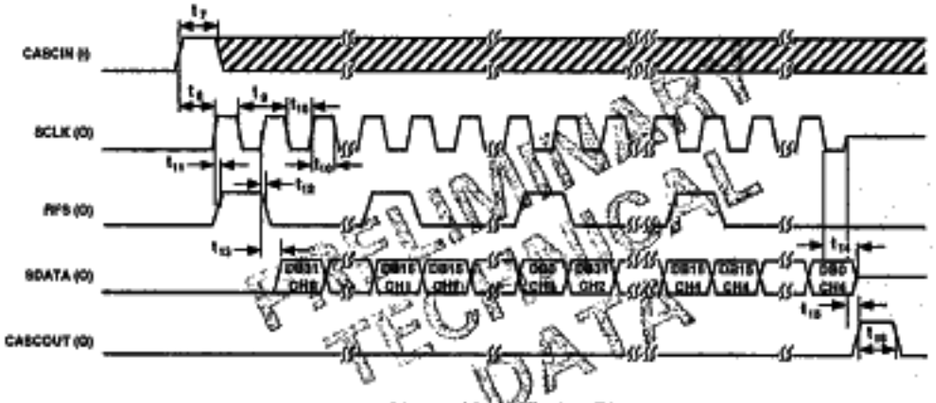


Figure 3. Master Mode Timing Diagram

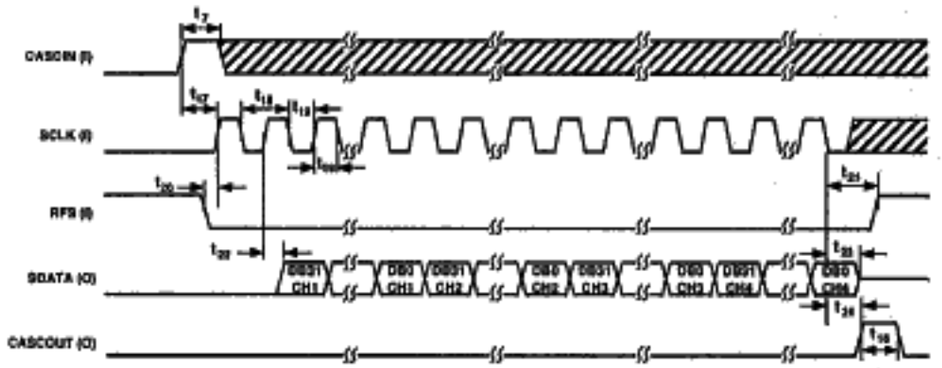


Figure 4. Slave Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

AV_{DD} to AGND . . . . . −0.3 V to +7 V
AV_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to +0.3 V
AV_{DD} to DV_{DD} . . . . . −0.3 V to +0.3 V
Analog Inputs to AGND . . . AV_{SS} − 0.3 V to AV_{DD} + 0.3 V
V_{REF} to AGND . . . . . V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V

Operating Temperature Range
Commercial Plastic (B Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 500 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN DESCRIPTION

Pin	Description
AV_{DD}	Analog Positive Supply, +5 V nominal.
DV_{DD}	Digital Positive Supply, +5 V nominal.
AV_{SS}	Analog Negative Supply, −5 V nominal.
RESET	A high pulse on this pin synchronizes the sampling point on the four input channels. It can be used in a multichannel system to ensure simultaneous sampling.
A0–A2	The three address pins, A0, A1 and A2 give the device a unique address. This information is contained in the output data stream from the device.
CLKIN	Clock Input for External Clock.
CLKOUT	Clock Output which is used to generate an internal master clock by connecting a crystal between CLKOUT and CLKIN. If an external clock is used, then CLKOUT is not connected.
MODE	This digital input determines the device interface mode. If it is hardwired low then the Master Mode interface is enabled; whereas if it is high, the Slave Mode interface is enabled.
CASCIN	Positive-edge triggered digital input which is used to enable the output data stream. This input is used to cascade several devices in a multichannel system.
CASCOUT	Digital output which goes high at the end of a complete 4-channel data transfer. This can be connected to the CASCIN of the next device in a multi-channel system to ensure proper control of the data transfer.
RFS	Receive Frame Synchronization signal for the serial output data stream. This can be an input or output depending on the interface mode.
SDATA	Serial Data Input/Output pin.
SCLK	Serial Clock Input/Output. The SCLK pin is configured as an input or output, depending on the state of the Mode pin.
DRDY	Data Ready Output. DRDY is low when valid data is available in the output register. It goes high for four clock cycles when a new word is being loaded into the output register, to indicate that valid data is not available.
TFS	Transmit Frame Sync input for programming the on-chip Control Register.
D0	Digital Data Input. This is contained in the digital data stream sent from the device.
D1, D2	Digital Outputs. These two digital outputs can be programmed from the on-chip Control Register. They can be used to switch in calibration signals at the front end.
V_{REF}	Reference Input, nominally 2.5 V.
AGND	Analog Ground. Ground reference for analog circuitry.
DGND	Digital Ground. Ground return for digital circuitry.
$A_{IN}1$–$A_{IN}4$	Analog Input pins. The analog input range is ±2.5 V.

7

DESCRIPTION OF OPERATION

Voltage Reference

Full scale analog input corresponds to reference voltage input.

The reference input presents exactly the same dynamic load as the analog input, but in the case of the reference input, source resistance and long settling time introduce gain errors rather than offset errors. Most precision references however have sufficiently low output impedance and wide enough bandwidth to settle to the required accuracy in the time allowed by the AD79024.

The reference should be chosen to have minimal noise in the programmed passband. Recommended references are the AD580, AD680 or the ADREF-43 from Analog Devices. These low noise references have a typical noise spectral density of 40 nV/$\sqrt{Hz}$ at 300 Hz.

Clock Generation

The device operates from a master clock which must be provided either from a crystal source or an external clock source. If a crystal is used, it must be connected across the CLKIN and CLKOUT pins. An external clock can be used by driving the CLKIN input directly with a CMOS compatible clock. In this case, CLKOUT is left unconnected. The nominal clock frequency for the device is 4.096 MHz.

Control Register Description

The 16-bit control register is programmed in two 8-bit bytes. Three control lines are used: TFS, SCLK and SDATA. SCLK can be an input or an output depending on the state of the MODE pin. When this is low, SCLK is an output (Master Mode); and when it is high, SCLK is an input (Slave Mode). When TFS goes low, data on the SDATA line is clocked into the control register on each succeeding falling edge of SCLK. When 8 bits have been clocked in, the transfer automatically stops. Only when another negative going edge is detected on TFS will new information be written into the control register. The control register programming model is shown in Table II. Bits DB8 and DB0 allow the control register to identify whether the MS Byte or the LS Byte has been programmed. Only when DB8 is a 1 and DB0 is a 0 will the register recognize that a complete valid word has been programmed.

Control Register bit, A3, acts as an extra address bit which must always be set to 1 to enable programming of the AD79024. If it is set to 0 then the programmed word is ignored. This allows the user to bypass the AD79024 control register and use the serial stream from the DSP or microcomputer to program other serial peripheral devices.

When a valid word has been received, the device interrogates the mode bit, M0. If this is 0, then the digital filter cut-off frequencies are programmed to the appropriate value if the device address pins correspond to the A2, A1, A0 bits in the control register. If the device address pins do not correspond to the A2, A1, A0 bits, then the FC2, FC1, FC0 bits are ignored. If M0 is 1, then the digital filter cut-off frequencies are programmed to the FC2, FC1, FC0 value irrespective of the address bits. In a multichannel system this allows the user to either program all AD79024s to have the same cut-off frequency or else to give each device a separate cut-off frequency.

Control Register bits FC2, FC1, FC0 program the digital filter cut-off frequency (see Table IV).

Control Register bits D2, D1 control the digital output Pins D2 and D1. These are programmed in the same way as FC2, FC1, FC0.

Table II. Control Register Programming Model

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
A3	A2	A1	A0	M0	FC2	FC1	1	FC0	D2	D1	X	X	X	X	0

Table III. M0 Truth Table

M0	Operating Mode
0	Initialization Mode 0. A2, A1, A0 determine which device is addressed and programmed with cut-off frequency and digital output.
1	Initialization Mode 1. A2, A1, A0 ignored. All devices are addressed and programmed with common cut-off frequency and digital output.

Table IV. Cut-Off Frequency Truth Table

FC2	FC1	FC0	Cut-Off Frequency (Hz)
0	0	0	300
0	0	1	150
0	1	0	75
0	1	1	37.5
1	0	0	18.75

Reset

The AD79024 has a hardware reset which can be used to synchronize many devices. When the RESET pin goes low after being high for at least 4 CLKIN cycles, the modulator sampling points and digital filter starting points are all synchronized. This synchronizes all devices which receive the RESET pulse and gives simultaneous sampling of all channels.

Data Output Interface Modes

When the control register has been programmed, the device begins conversion. There is an initial delay of 400,000 master clock cycles to allow the digital filters to settle. These filters are $Sinc^3$ and so the filter output update rate is directly related to the programmed cut-off frequency. The ratio between these is 3.81. So, for a filter cut-off frequency of 300 Hz, the output update is 1.145 kHz. The falling edge of the DRDY output indicates that the output shift register has been updated. There are two interface modes. One is the Master Mode where the AD79024 is the master in the system and the processor to which it is communicating is the slave. The other mode is the Slave Mode where the AD79024 is the slave and the processor is the system master. In both of these modes the data output stream contains 4 × 32 bits corresponding to the four input channels. The output data format is given in Table V, and the channel address format is given in Table VI.

Master Mode Interface

In this mode, data is clocked out of the AD79024 by an internally generated serial clock and frame synchronization pulse. Two signals initiate the transfer. These are the input CASCIN and the internally generated DRDY signal. When a rising edge is detected on CASCIN, the device checks the state of DRDY. Note, that on initial power-up or after a reset has been applied, the CASCIN input is not necessary on device 000 for the first data transfer but is required thereafter.

If DRDY is low, then the 3-state output, RFS, goes high on the next rising edge of CLKIN and stays high for two CLKIN cycles before going low again. The 3-state SCLK output is also activated on the same rising edge. As RFS goes low, DB31 is clocked out on the rising edge of SCLK. Data is transmitted in 16-bit words. For each A_{IN}, there are two 16-bit words and two RFS signals. When DB0 of $A_{IN}4$ has been clocked out, SCLK goes back into 3-state and the CASCOUT output goes high for two master clock cycles. DRDY also goes high at this point. Successive devices can be networked together by tying the CASCOUT of one device to the CASCIN on the next one.

The Master Mode interface is very suitable for loading data into a serial-to-parallel shift register or for DSPs like the ADSP-2101 which can accept a continuous stream of 16-bit words.

Slave Mode Interface

In this mode, the master processor controls the transfer of data from the signal processing block. It starts the transfer by sending a frame synchronization pulse and serial clock to the AD79024. This could be in response to an interrupt generated by the DRDY output on the AD79024. If the device has detected a rising edge on CASCIN or is device 000 on its first transfer, it starts to send out data on the next rising edge of SCLK. When all the data bits have been clocked out, the CASCOUT pin goes high for two CLKIN cycles and DRDY also goes high. If the device is still transmitting data when a new word becomes available, the old data will continue to be transmitted and the new data is lost.

The Slave Mode interface is suited to both microcomputers like the 8051 and 68HC11 and also DSPs like the TMS320C25, ADSP-2101 and 56000.

7

Table V. Output Data Word Format

DB31 . . . . . DB12	DB11 DB10	DB9 DB8 DB7	DB6	DB5 . . . . . DB0
DB19 . . . . . DB0	CA1 CA0	A0 A1 A2	D0	X X
Conversion Result	Channel Address	Device Address	Pace Detect	Don't Care

Table VI. Channel Address Format

Channel	CA1	CA0
A_{IN} 1	0	0
A_{IN} 2	0	1
A_{IN} 3	1	0
A_{IN} 4	1	1