

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

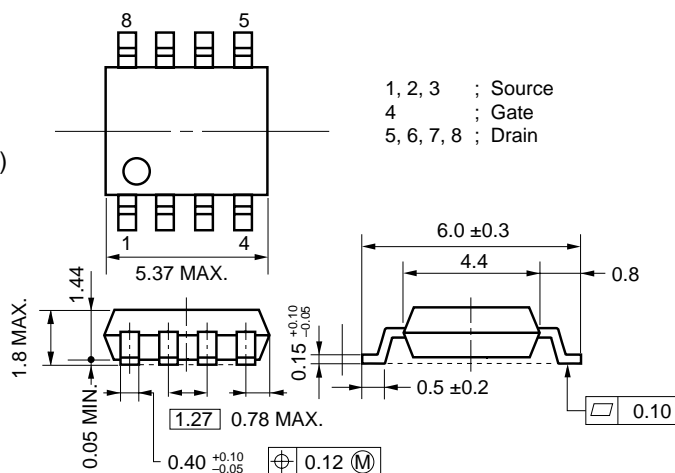
#### DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for power management applications of notebook computers.

#### FEATURES

- Super Low On-Resistance  
 $R_{DS(on)1} = 10.5 \text{ m}\Omega$  MAX. ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 5.0 \text{ A}$ )  
 $R_{DS(on)2} = 17 \text{ m}\Omega$  MAX. ( $V_{GS} = 4 \text{ V}$ ,  $I_D = 5.0 \text{ A}$ )
- Low  $C_{iss}$   $C_{iss} = 2180 \text{ pF TYP.}$
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

#### PACKAGE DIMENSIONS (in millimeter)

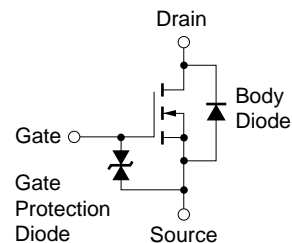


#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25 \text{ }^\circ\text{C}$ , all terminals are connected)

Drain to Source Voltage	$V_{DSS}$	30	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 10$	A
Drain Current (pulse) <sup>Notes1</sup>	$I_{D(pulse)}$	$\pm 40$	A
Total Power Dissipation ( $T_A = 25 \text{ }^\circ\text{C}$ ) <sup>Notes2</sup>	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

**Notes 1.**  $PW \leq 10 \text{ } \mu\text{s}$ , Duty Cycle  $\leq 1 \%$

**2.** Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 0.7 \text{ mm}$

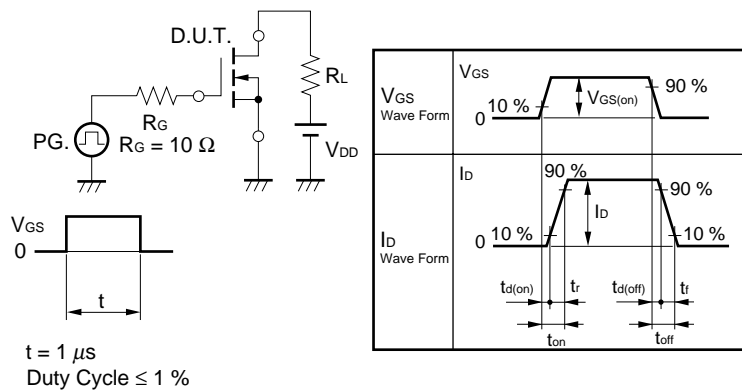


The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

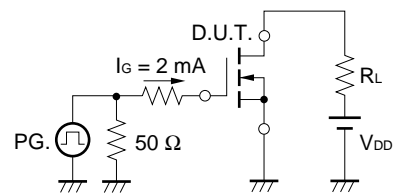
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, all terminals are connected)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.0 A		8.5	10.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 5.0 A		12	17	mΩ
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.0 A	8.0	18		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		2180		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0		890		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		370		pF
Turn-On Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 5.0 A		25		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		210		ns
Turn-Off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 15 V		120		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		75		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 10 A		40		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 24 V		5.6		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		9.6		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0		0.73		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0		46		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		45		nC

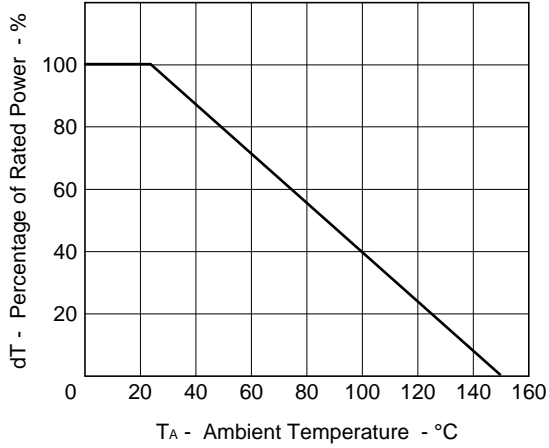
**Test Circuit 1 Switching Time**



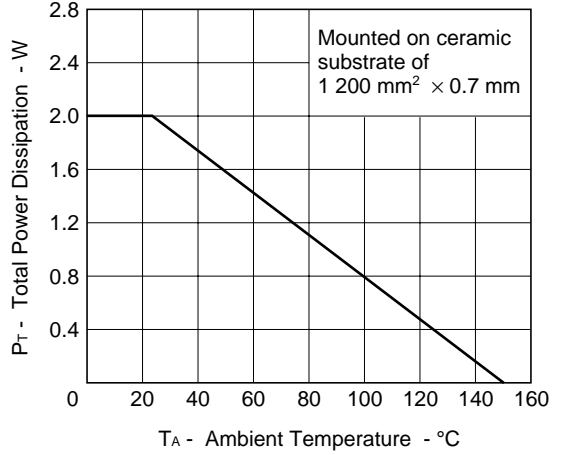
**Test Circuit 2 Gate Charge**



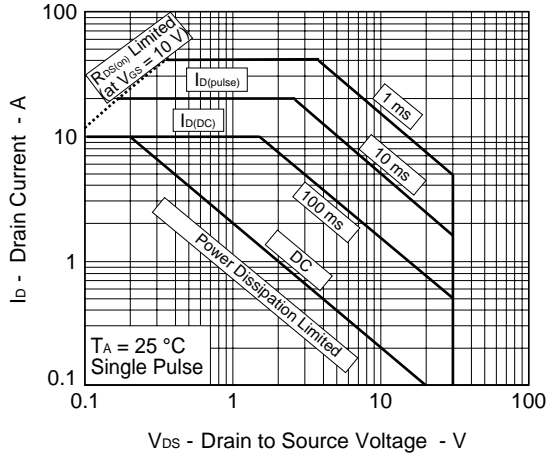
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

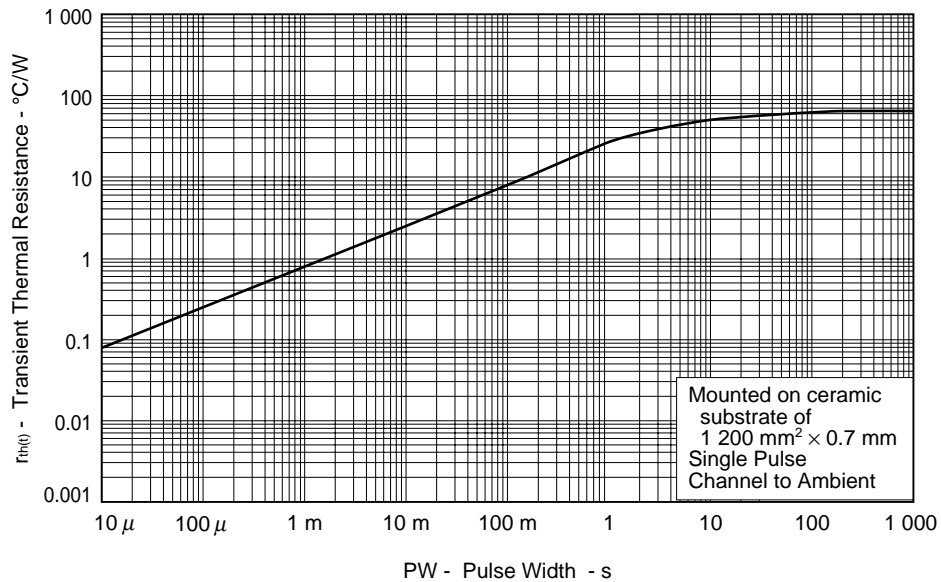


FORWARD BIAS SAFE OPERATING AREA

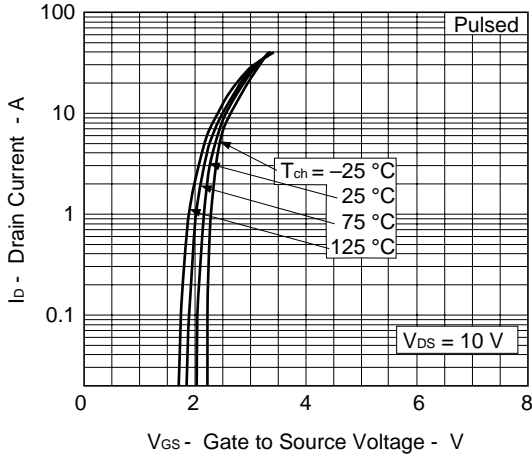


Note:  
Mounted on ceramic substrate of 1 200 mm<sup>2</sup> × 0.7 mm

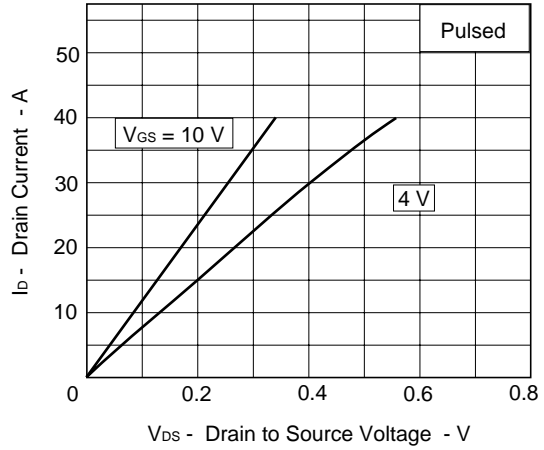
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



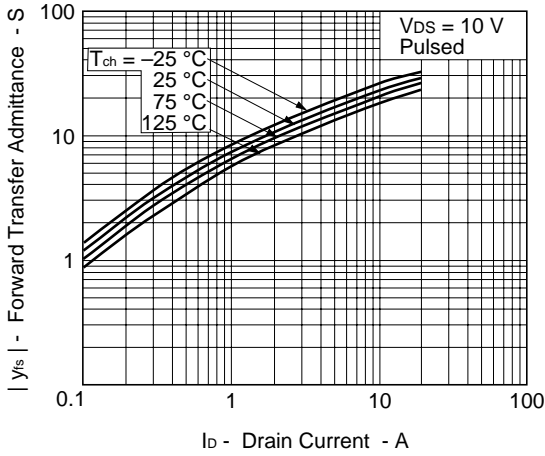
FORWARD TRANSFER CHARACTERISTICS



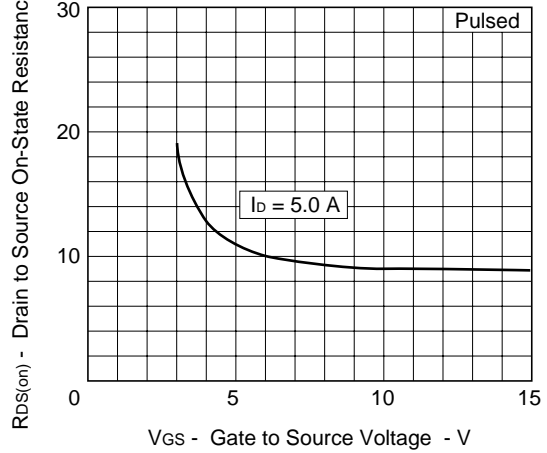
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



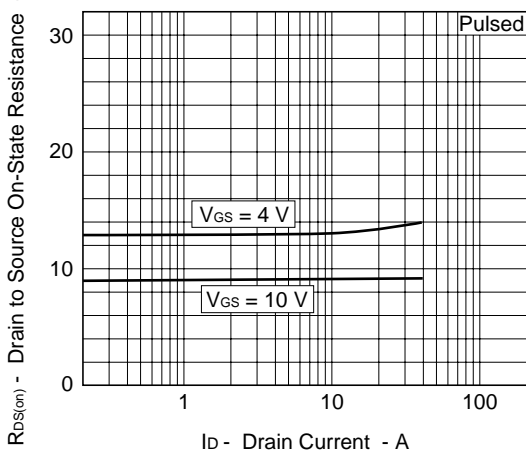
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



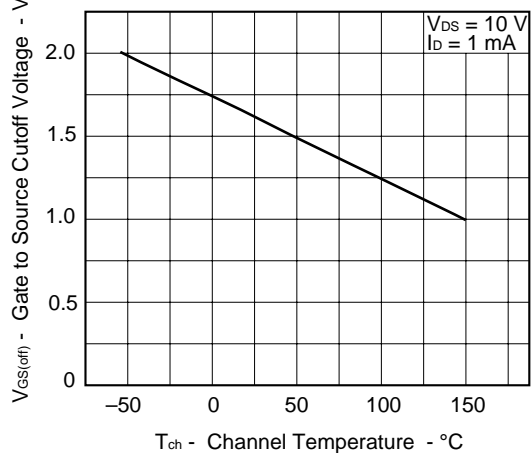
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

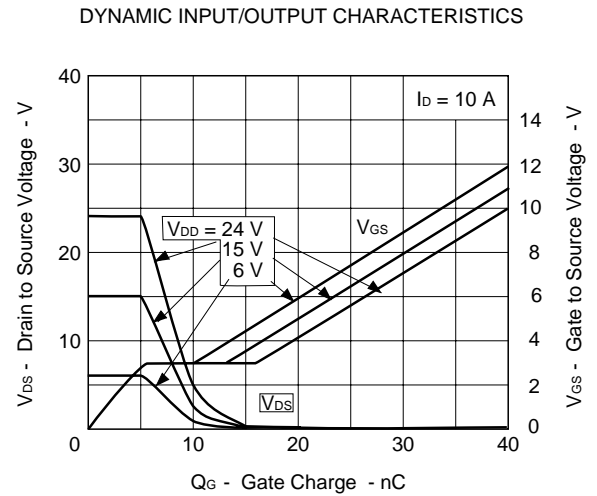
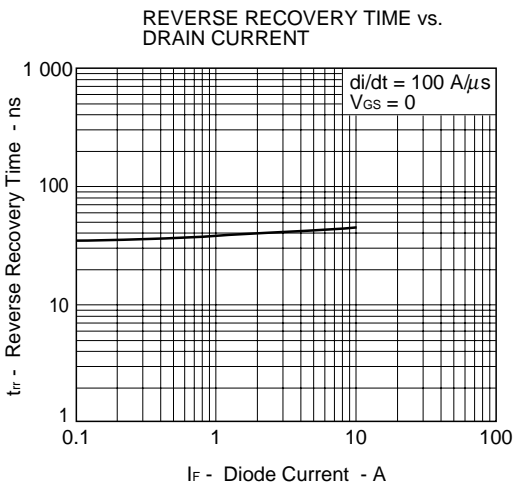
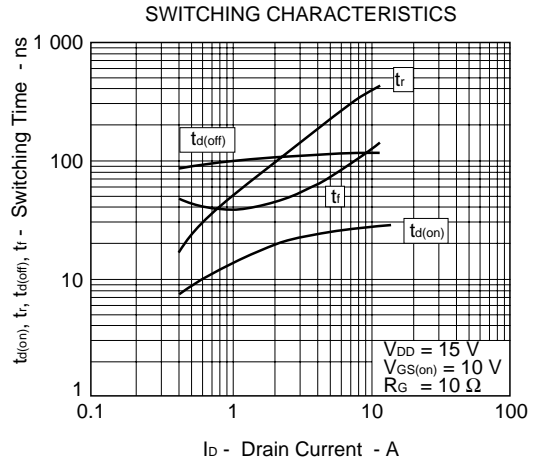
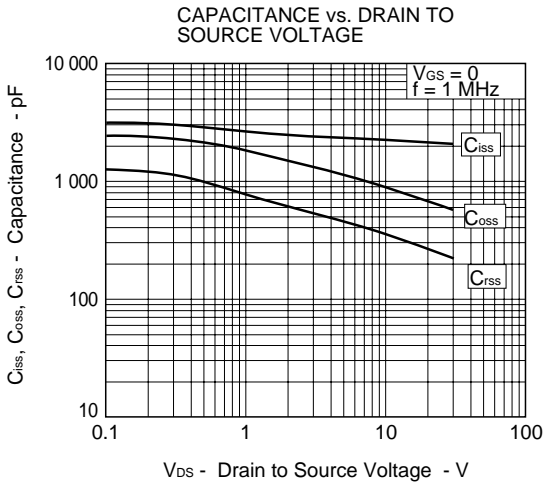
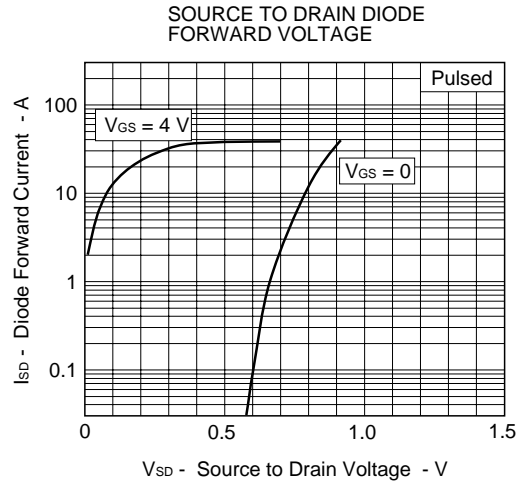
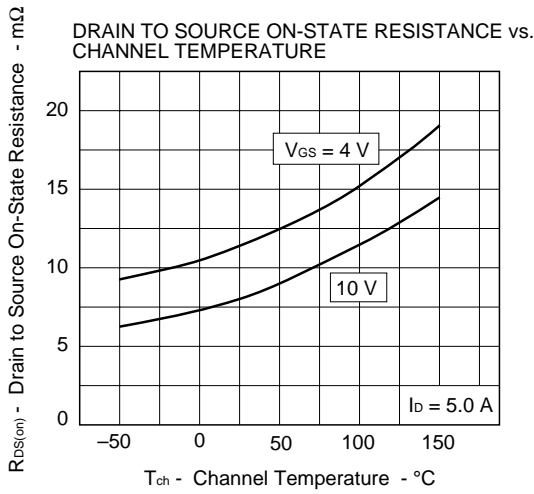


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





## REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	C11745E
Quality grade on NEC semiconductor devices	C11531E
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.