# HFA1110/883

## 750MHz, Low Distortion Unity Gain, Closed Loop Buffer

November 1998

### Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Fixed Gain of +1**
- **Wide -3dB Bandwidth . . . . . 750MHz (Typ)**
- **Very Fast Slew Rate . . . . . 1250V/μs (Typ)**
- **Low Differential Gain and Phase . . . 0.04%/0.025 Deg.**
- **Low Distortion (HD3, 30MHz) . . . . . -80dBc (Typ)**
- **Excellent Gain Flatness (to 100MHz) . . . ±0.03dB (Typ)**
- **Excellent Gain Accuracy . . . . . 0.99V/V (Typ)**
- **High Output Current . . . . . 60mA (Typ)**

### Applications

- **Video Switching and Routing**
- **Pulse and Video Amplifiers**
- **Wideband Amplifiers**
- **RF/IF Signal Processing**
- **Flash A/D Driver**
- **Medical Imaging Systems**

### Description

The HFA1110/883 is a unity gain, closed loop buffer which achieves a high degree of gain accuracy, wide bandwidth, and low distortion. Manufactured on Intersil's proprietary complementary bipolar UHF-1 process, the HFA1110/883 also offers very fast slew rates, and high output current.

Component and composite video systems will also benefit from this buffer's performance, as indicated by the excellent gain flatness, and 0.04%/0.025 Degree Differential Gain/Phase specifications ($R_L$ = 75Ω).

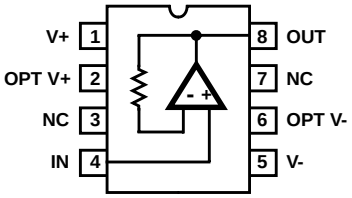
For buffer applications desiring a standard op amp pinout, or selectable gain (-1, +1, +2), please refer to the HFA1112/883 and HFA1113/883 (featuring programmable output clamps) datasheets.

### Ordering Information

| PART NUMBER | TEMP. RANGE ($^oC$) | PACKAGE | PKG. NO. |
|---|---|---|---|
| HFA1110MJ/883 | -55 to 125 | 8 Ld CERDIP | F8.3A |

### Pinout

**HFA1110/883**
**(CERDIP)**
TOP VIEW








Spec Number **511083-883**
File Number **3620.2**

## Absolute Maximum Ratings

Voltage Between V+ and V- . . . . . 12V
Voltage at Input Terminal . . . . . V+ to V-
Output Current (50% Duty Cycle) . . . . . ±55mA
ESD Rating. . . . . <2000V

## Operating Conditions

Supply Voltage ($\pm V_S$). . . . . ±5V
$R_L \geq 50\Omega$
Temperature Range . . . . . $-55^oC \leq T_A \leq 125^oC$

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$($^o$C/W) | $\theta_{JC}$($^o$C/W) |
|---|---|---|
| CERDIP Package . . . . . | 120 | 35 |

Maximum Package Power Dissipation at 75$^o$C
CERDIP Package . . . . . 0.83W
Package Power Dissipation Derating Factor above 75$^o$C
CERDIP Package . . . . . 8.3mW/$^o$C
Junction Temperature . . . . . 175$^o$C
Storage Temperature Range . . . . . $-65^oC \leq T_A \leq 150^oC$
Lead Temperature (Soldering 10s) . . . . . 300$^o$C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

**TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS**

Device Tested at: $V_{SUPPLY} = \pm 5V$, $R_{SOURCE} = 0\Omega$, $R_L = 100\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

| PARAMETER | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE ($^o$C) | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Offset Voltage | $V_{OS}$ | $V_{CM} = 0V$ | 1 | 25 | -25 | 25 | mV |
| | | | 2, 3 | 125, -55 | -40 | 40 | mV |
| Power Supply Rejection Ratio | PSRRP | $\Delta V_{SUP} = \pm 1.25V$ V+ = 6.25V, V- = -5V V+ = 3.75V, V- = -5V | 1 | 25 | 39 | - | dB |
| | | | 2, 3 | 125, -55 | 35 | - | dB |
| | PSRRN | $\Delta V_{SUP} = \pm 1.25V$ V+ = 5V, V- = -6.25V V+ = 5V, V- = -3.75V | 1 | 25 | 39 | - | dB |
| | | | 2, 3 | 125, -55 | 35 | - | dB |
| Input Current | $I_{BSP}$ | $V_{CM} = 0V$ | 1 | 25 | -40 | 40 | µA |
| | | | 2, 3 | 125, -55 | -65 | 65 | µA |
| Input Current Common Mode Rejection | $CMS_{IBP}$ | $\Delta V_{CM} = \pm 2V$ V+ = 3V, V- = -7V V+ = 7V, V- = -3V | 1 | 25 | - | 40 | µA/V |
| | | | 2, 3 | 125, -55 | - | 50 | µA/V |
| Input Resistance | $R_{IN}$ | Note 2 | 1 | 25 | 25 | - | kΩ |
| | | | 2, 3 | 125, -55 | 20 | - | kΩ |
| Gain ($V_{OUT} = 2V_{P-P}$) | $A_{VP1}$ | $V_{IN}$ = -1V to +1V | 1 | 25 | 0.980 | 1.020 | V/V |
| | | | 2, 3 | 125, -55 | 0.975 | 1.025 | V/V |
| Output Voltage Swing | $V_{OP100}$ | $R_L = 100\Omega$, $V_{IN}$ = +3.3V | 1 | 25 | 3 | - | V |
| | | | 2, 3 | 125, -55 | 2.5 | - | V |
| | $V_{ON100}$ | $R_L = 100\Omega$, $V_{IN}$ = -3.3V | 1 | 25 | - | -3 | V |
| | | | 2, 3 | 125, -55 | - | -2.5 | V |
| Output Voltage Swing | $V_{OP50}$ | $R_L = 50\Omega$, $V_{IN}$ = +2.7V | 1 | 25 | 2.5 | - | V |
| | | $R_L = 50\Omega$, $V_{IN}$ = +3.3V | 2 | 125 | 2.5 | - | V |
| | | | 3 | -55 | 1.5 | - | V |
| | $V_{ON50}$ | $R_L = 50\Omega$, $V_{IN}$ = -2.7V | 1 | 25 | - | -2.5 | V |
| | | $R_L = 50\Omega$, $V_{IN}$ = -3.3V | 2 | 125 | - | -2.5 | V |
| | | | 3 | -55 | - | -1.5 | V |

**TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)**

Device Tested at: $V_{SUPPLY}$ = ±5V, $R_{SOURCE}$ = 0Ω, $R_L$ = 100Ω, $V_{OUT}$ = 0V, Unless Otherwise Specified.

| PARAMETER | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE ($^oC$) | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Current | $+I_{OUT}$ | Note 3 | 1, 2 | 25, 125 | 50 | - | mA |
| | | | 3 | -55 | 30 | - | mA |
| | $-I_{OUT}$ | Note 3 | 1, 2 | 25, 125 | - | -50 | mA |
| | | | 3 | -55 | - | -30 | mA |
| Quiescent Power Supply Current | $I_{CC}$ | $R_L$ = 100Ω | 1 | 25 | 14 | 26 | mA |
| | | | 2, 3 | 125, -55 | - | 33 | mA |
| | $I_{EE}$ | $R_L$ = 100Ω | 1 | 25 | -26 | -14 | mA |
| | | | 2, 3 | 125, -55 | -33 | - | mA |

NOTES:

2. Guaranteed from Input Common Mode Rejection Test, by: $R_{IN} = 1/CMS_{IBP}$.
3. Guaranteed from $V_{OUT}$ Test with $R_L$ = 50Ω, by: $I_{OUT} = V_{OUT}/50Ω$.

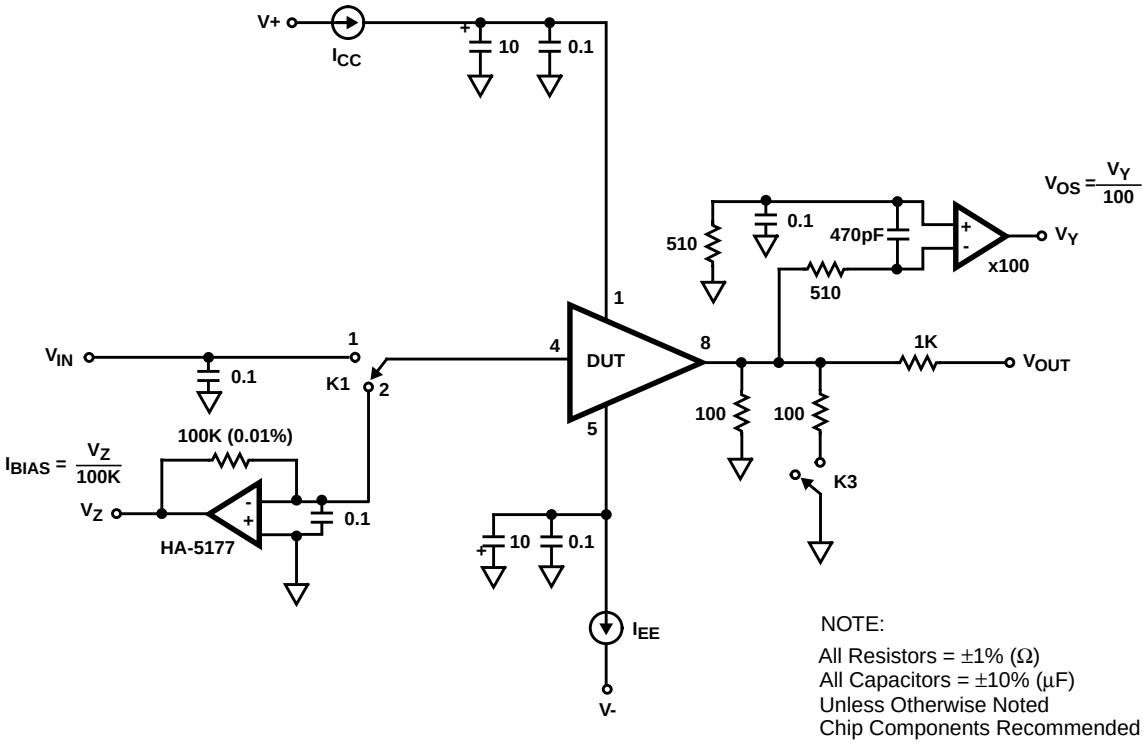
**TABLE 2. ELECTRICAL TEST REQUIREMENTS**

| MIL-STD-883 TEST REQUIREMENTS | SUBGROUPS (SEE TABLE 1) |
|---|---|
| Interim Electrical Parameters (Pre Burn-In) | 1 |
| Final Electrical Test Parameters | 1 (Note 7), 2, 3 |
| Group A Test Requirements | 1, 2, 3 |
| Groups C and D Endpoints | 1 |

NOTE:

4. PDA applies to Subgroup 1 only.

## *Test Circuit* (Applies to Table 1)



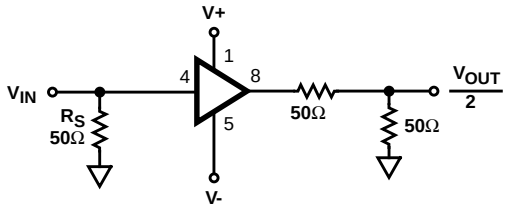

NOTE:

All Resistors = ±1% (Ω)
All Capacitors = ±10% (µF)
Unless Otherwise Noted
Chip Components Recommended

## Test Waveforms

**SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL PULSE RESPONSE** (Applies to Table 3)

**$A_V$ = +1 TEST CIRCUIT**




NOTE: $V_S = \pm 5V$
$R_S = 50\Omega$
$R_L = 100\Omega$ For Small and Large Signals

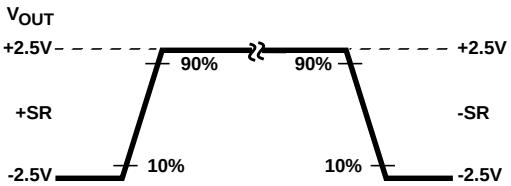



**FIGURE 1. LARGE SIGNAL WAVEFORM**

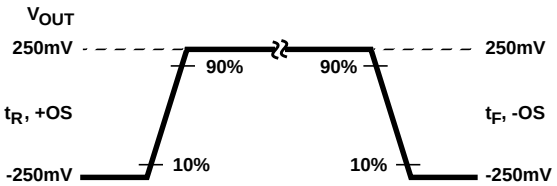
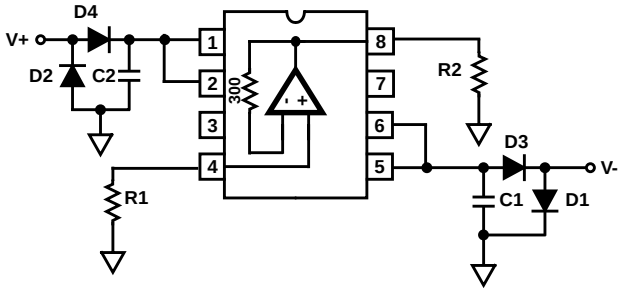



**FIGURE 2. SMALL SIGNAL WAVEFORM**

## Burn-In Circuit

**HFA1110MJ/883 CERAMIC DIP**




NOTES:

R1 = 1kΩ, ±5% (Per Socket)
R2 = 100Ω, ±5% (Per Socket)
C1 = C2 = 0.01µF (Per Socket) or 0.1µF (Per Row) Minimum

D1 = D2 = 1N4002 or Equivalent (Per Board)
D3 = D4 = 1N4002 or Equivalent (Per Socket)
V+ = +5.5V ± 0.5V
V- = -5.5V ± 0.5V

## Typical Design Information

*The information contained in this section has been developed through characterization by Intersil and is for use as application and design information only. No guarantee is implied.*

## Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$. Unless Otherwise Specified.

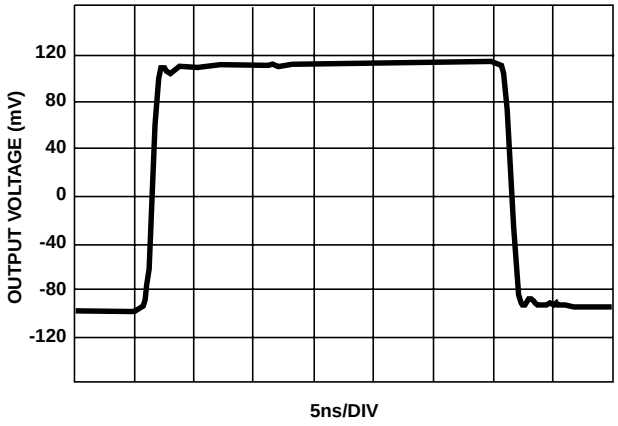



FIGURE 3. SMALL SIGNAL PULSE RESPONSE

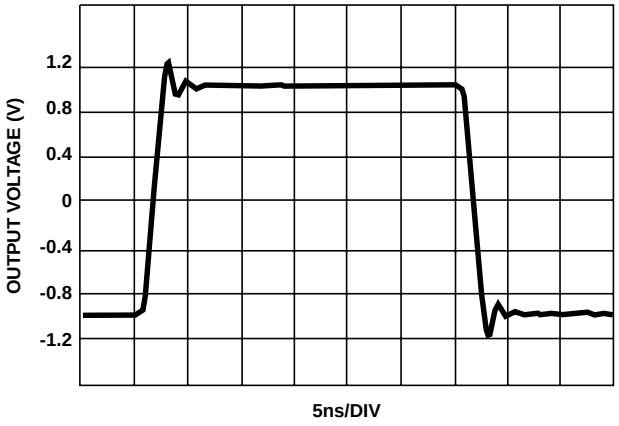



FIGURE 4. LARGE SIGNAL PULSE RESPONSE

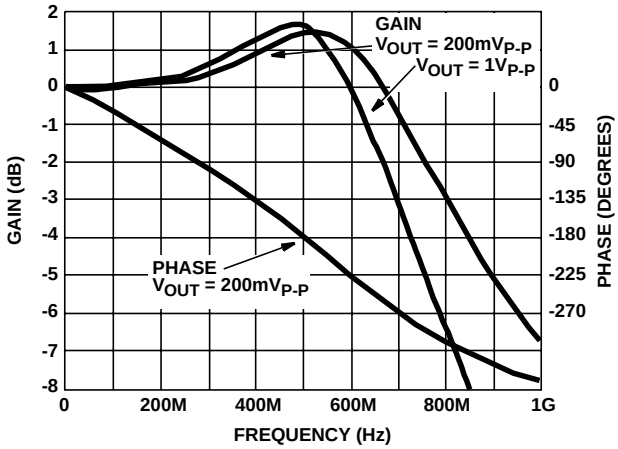



FIGURE 5. FORWARD GAIN AND PHASE

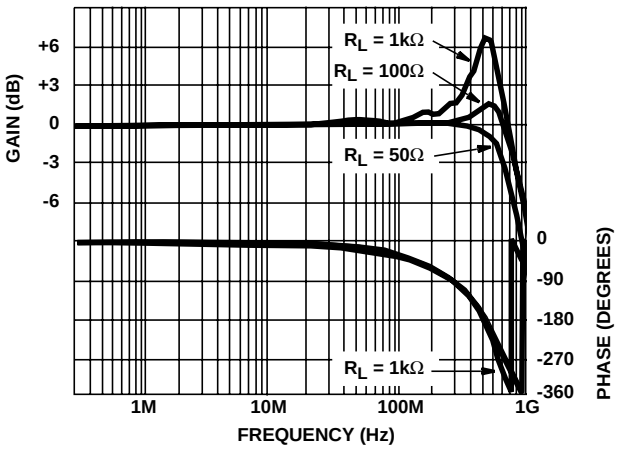



FIGURE 6. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

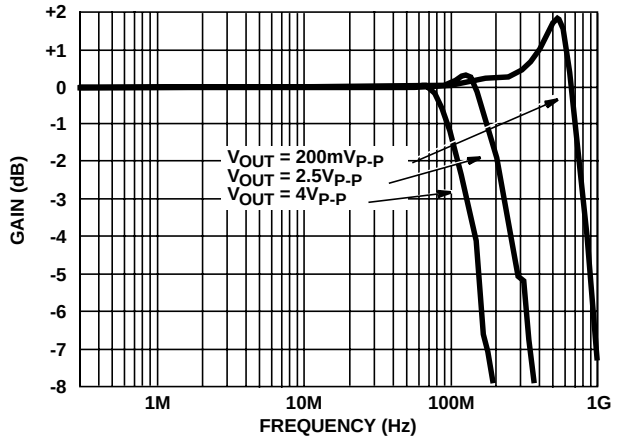



FIGURE 7. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

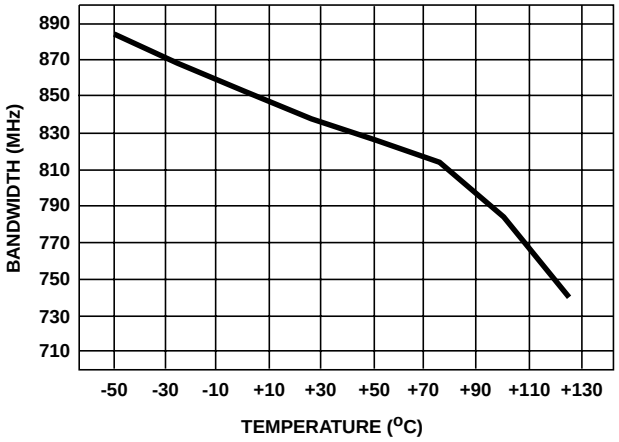



FIGURE 8. -3dB BANDWIDTH vs TEMPERATURE

## Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$. Unless Otherwise Specified. **(Continued)**

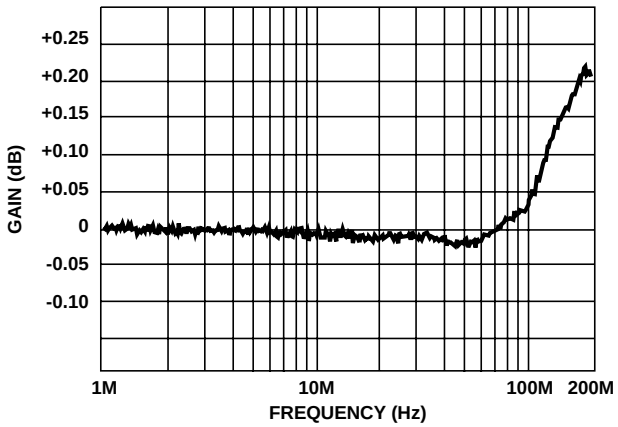



FIGURE 9. GAIN FLATNESS

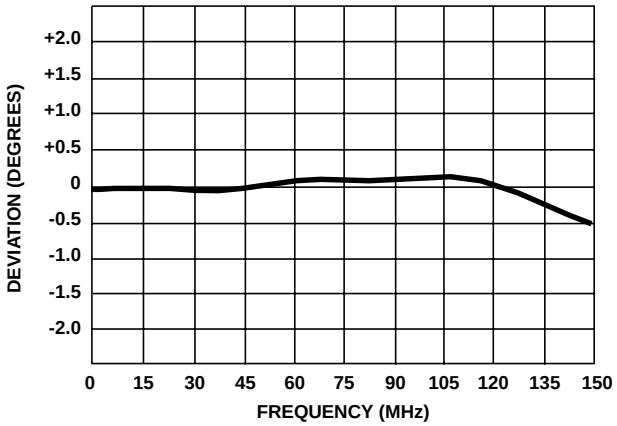



FIGURE 10. DEVIATION FROM LINEAR PHASE

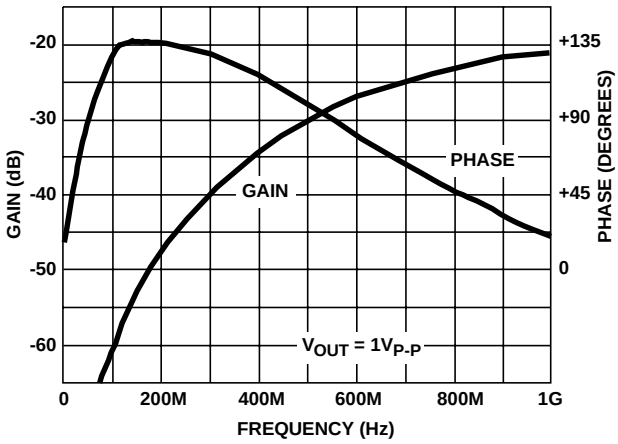



FIGURE 11. REVERSE GAIN AND PHASE

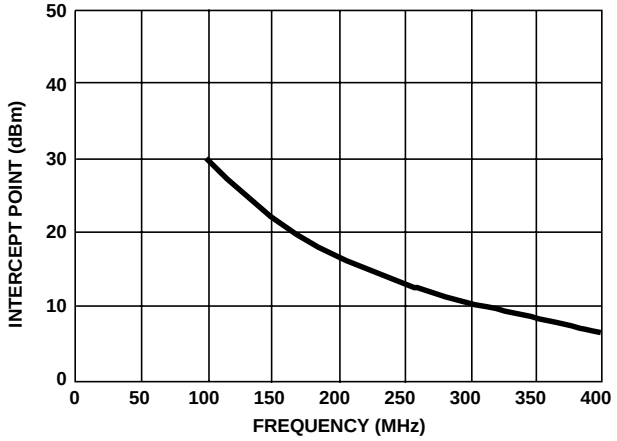



FIGURE 12. 2 TONE, 3RD ORDER INTERMODULATION INTERCEPT

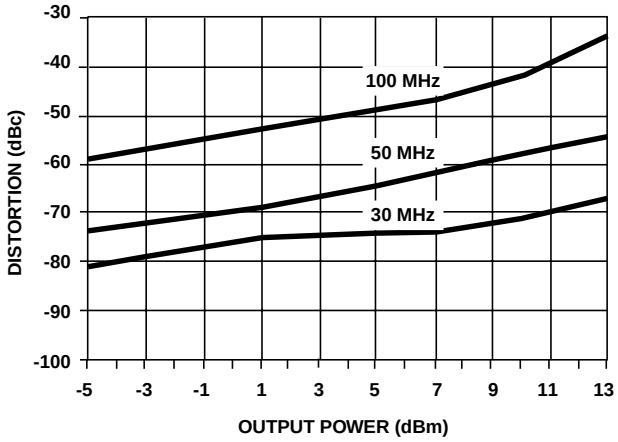



FIGURE 13. 2ND HARMONIC DISTORTION vs $P_{OUT}$

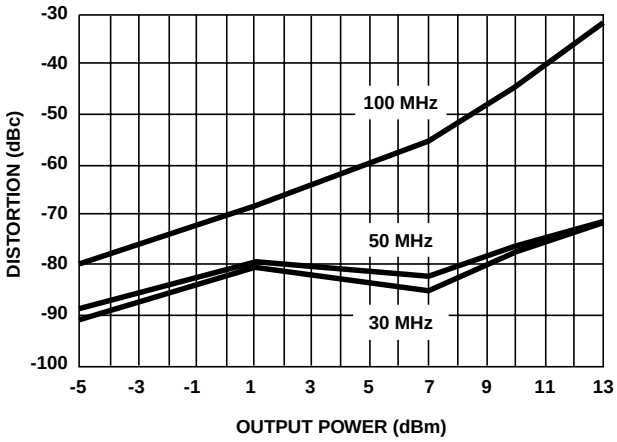



FIGURE 14. 3RD HARMONIC DISTORTION vs $P_{OUT}$

## Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$. Unless Otherwise Specified. **(Continued)**

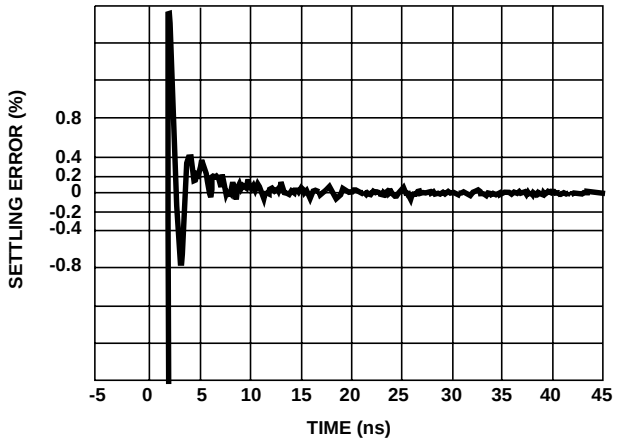



**FIGURE 15. SETTLING RESPONSE** ($V_{OUT}$ = 1V)

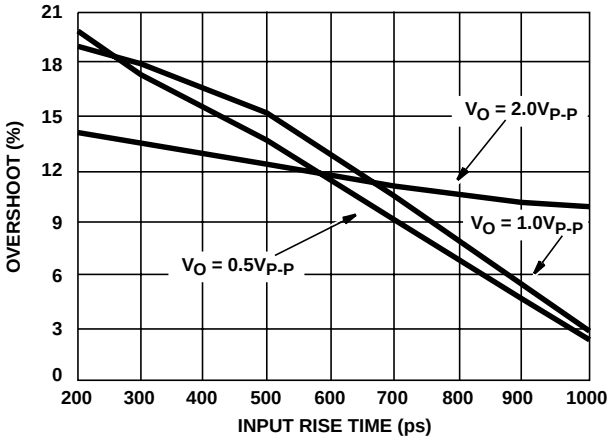



**FIGURE 16. OVERSHOOT vs INPUT RISETIME**

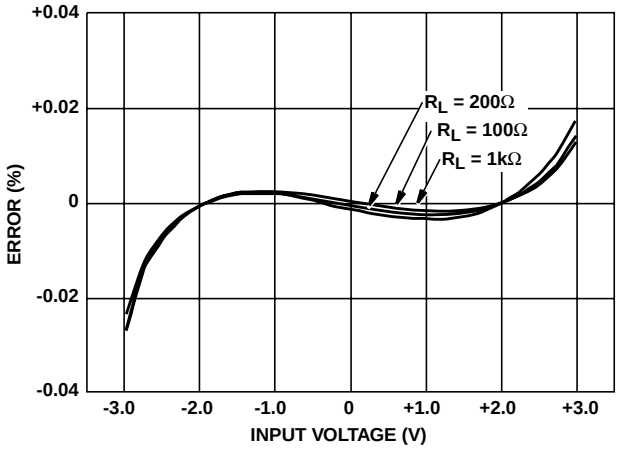



**FIGURE 17. INTEGRAL LINEARITY ERROR**

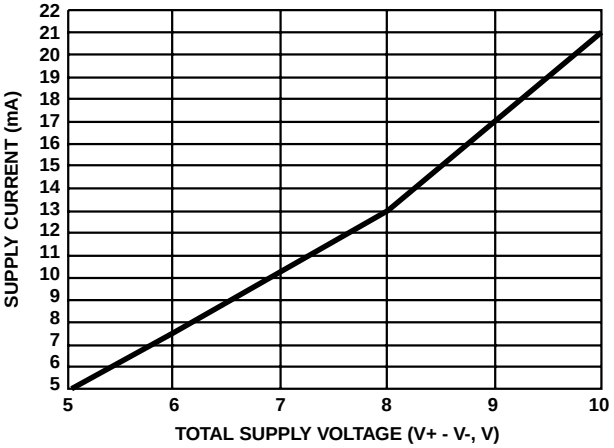



**FIGURE 18. SUPPLY CURRENT vs SUPPLY VOLTAGE**

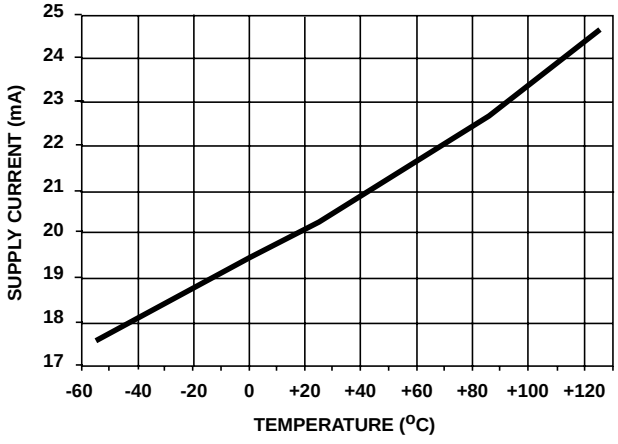



**FIGURE 19. SUPPLY CURRENT vs TEMPERATURE**

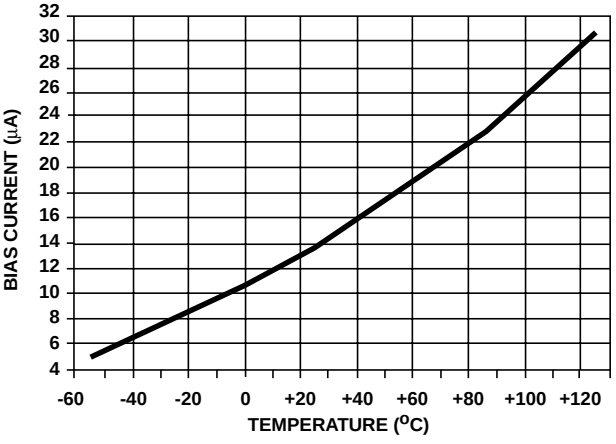



**FIGURE 20. BIAS CURRENT vs TEMPERATURE**

## Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$. Unless Otherwise Specified. **(Continued)**

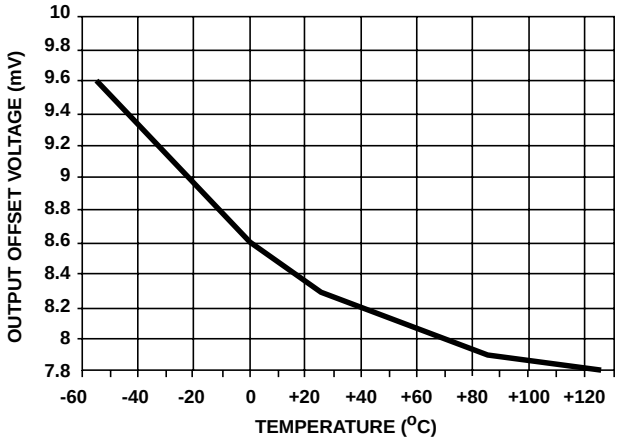



FIGURE 21. OFFSET VOLTAGE vs TEMPERATURE

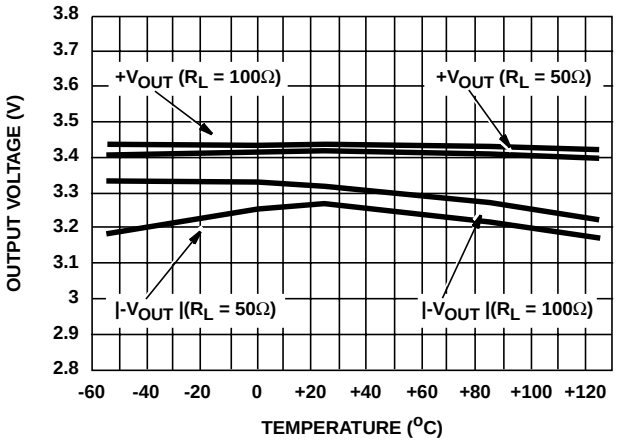



FIGURE 22. OUTPUT VOLTAGE vs TEMPERATURE

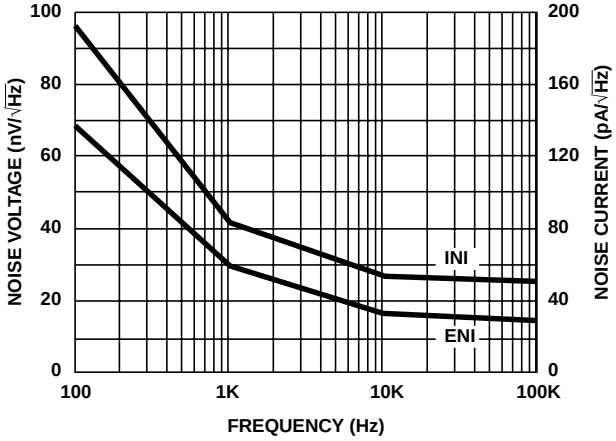



FIGURE 23. INPUT NOISE vs FREQUENCY

## PC Board Layout

The frequency response of this buffer depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section. Removing the GND plane under the output trace helps minimize this capacitance.

An example of a good high frequency layout is the Evaluation Board shown in Figure 25.

## Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the buffer's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor ($R_S$) in series with the output prior to the capacitance.

Figure 24 details starting points for the selection of this resistor. The points on the curve indicate the $R_S$ and $C_L$ combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

$R_S$ and $C_L$ form a low pass network at the output, thus limiting system bandwidth well below the buffer bandwidth of 750MHz. By decreasing $R_S$ as $C_L$ increases (as illustrated in Figure 24), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve.

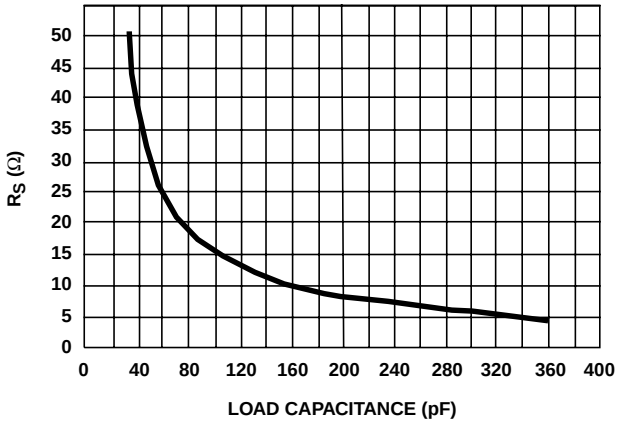


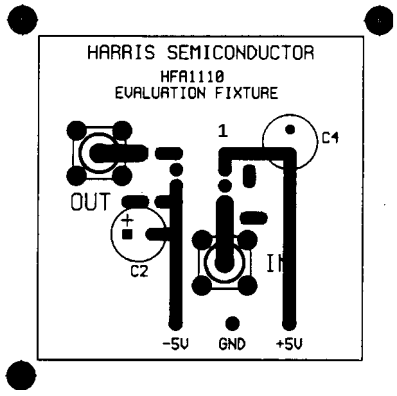

**FIGURE 24. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE**

## Evaluation Board

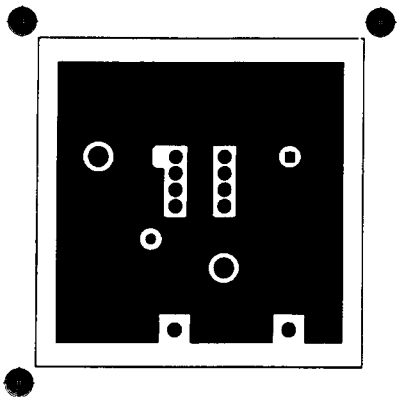
The performance of this buffer may be evaluated using the HFA1110 Evaluation Board. The layout and schematic of the board are shown in Figure 25.

To order evaluation boards, please contact your local sales office.

**TOP LAYOUT**




**BOTTOM LAYOUT**



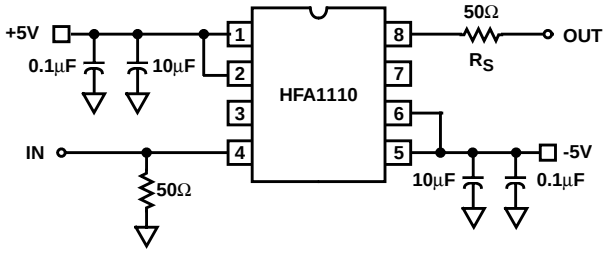



**FIGURE 25. EVALUATION BOARD SCHEMATIC AND LAYOUT**

**TABLE 3. TYPICAL PERFORMANCE SPECIFICATIONS**

Device Characterized at: $V_{SUPPLY}$ = ±5V, $R_L$ = 100Ω, Unless Otherwise Specified

| PARAMETER | CONDITIONS | TEMPERATURE ($^oC$) | TYPICAL | UNITS |
|---|---|---|---|---|
| Output Offset Voltage (See Note) | $V_{CM}$ = 0V | 25 | 8 | mV |
| Average Offset Voltage Drift | Versus Temperature | Full | 10 | µV/$^oC$ |
| Power Supply Rejection Ratio | $\Delta V_{SUP}$ = ±1.25V | 25 | 45 | dB |
| Input Current (See Note) | $V_{CM}$ = 0V | 25 | 10 | µA |
| Input Resistance | $\Delta V_{CM}$ = ±2V | 25 | 50 | kΩ |
| Input Capacitance | | 25 | 2.2 | pF |
| Input Noise Voltage (See Note) | f = 100kHz | 25 | 14 | nV/$\sqrt{Hz}$ |
| Input Noise Current (See Note) | f = 100kHz | 25 | 51 | pA/$\sqrt{Hz}$ |
| Input Common Mode Range | | Full | ±2.8 | V |
| Gain | $V_{OUT}$ = $2V_{P-P}$ | 25 | 0.99 | V/V |
| DC Non-Linearity (See Note) | ±2V Full Scale | 25 | 0.003 | % |
| Output Voltage (See Note) | $R_L$ = 100Ω | 25 | ±3.3 | V |
| | $R_L$ = 100Ω | Full | ±3.0 | V |
| Output Current (See Note) | $R_L$ = 50Ω | 25 to 125 | ±60 | mA |
| | $R_L$ = 50Ω | -55 to 0 | ±50 | mA |
| DC Closed Loop Output Resistance | | 25 | 0.3 | W |
| Quiescent Supply Current (See Note) | $R_L$ = Open | Full | 24 | mA |
| -3dB Bandwidth (See Note) | $V_{OUT}$ = $200mV_{P-P}$ | 25 | 750 | MHz |
| Slew Rate | $V_{OUT}$ = $5V_{P-P}$ | 25 | 1250 | V/µs |
| Full Power Bandwidth (See Note) | $V_{OUT}$ = $4V_{P-P}$ | 25 | 150 | MHz |
| Gain Flatness (See Note) | To 30MHz | 25 | ±0.01 | dB |
| | To 50MHz | 25 | ±0.02 | dB |
| | To 100MHz | 25 | ±0.03 | dB |
| Linear Phase Deviation (See Note) | To 100MHz | 25 | ±0.3 | Degrees |
| 2nd Harmonic Distortion (See Note) | 30MHz, $V_{OUT}$ = $2V_{P-P}$ | 25 | -72 | dBc |
| | 50MHz, $V_{OUT}$ = $2V_{P-P}$ | 25 | -57 | dBc |
| | 100MHz, $V_{OUT}$ = $2V_{P-P}$ | 25 | -42 | dBc |
| 3rd Harmonic Distortion (See Note) | 30MHz, $V_{OUT}$ = $2V_{P-P}$ | 25 | -80 | dBc |
| | 50MHz, $V_{OUT}$ = $2V_{P-P}$ | 25 | -74 | dBc |
| | 100MHz, $V_{OUT}$ = $2V_{P-P}$ | 25 | -51 | dBc |
| 3rd Order Intercept (See Note) | 100MHz | 25 | 30 | dBm |
| | 300MHz | 25 | 10 | dBm |
| 1dB Gain Compression | 100MHz | 25 | 14 | dBm |
| | 150MHz | 25 | 10 | dBm |
| | 200MHz | 25 | 7 | dBm |
| Reverse Isolation ($S_{12}$) (See Note) | 40MHz | 25 | -70 | dB |
| | 100MHz | 25 | -60 | dB |
| | 600MHz | 25 | -27 | dB |
| Rise and Fall Time | $V_{OUT}$ = $0.5V_{P-P}$ | 25 | 600 | ps |
| Overshoot (See Note) | $V_{OUT}$ = $0.5V_{P-P}$, Input $t_R$ /$t_F$ = 600ps | 25 | 9 | % |
| Differential Gain | $R_L$ = 75Ω, NTSC | 25 | 0.04 | % |
| Differential Phase | $R_L$ = 75Ω, NTSC | 25 | 0.025 | Degrees |

NOTE: See Typical Performance Curves for more information.

## Die Characteristics

**DIE DIMENSIONS:**

63 x 44 x 19 mils ± 1 mils
1600 x 1130 x 483µm ± 25.4µm

**METALLIZATION:**

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

**GLASSIVATION:**

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

**WORST CASE CURRENT DENSITY:**

$2.0 \times 10^5$ A/cm$^2$ at 47.5mA

**TRANSISTOR COUNT:**

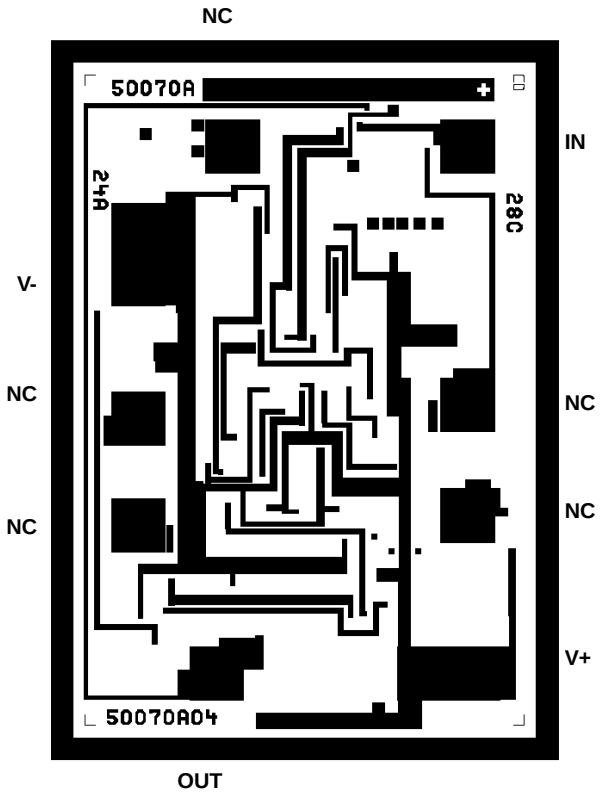
52

**SUBSTRATE POTENTIAL (Powered Up):**

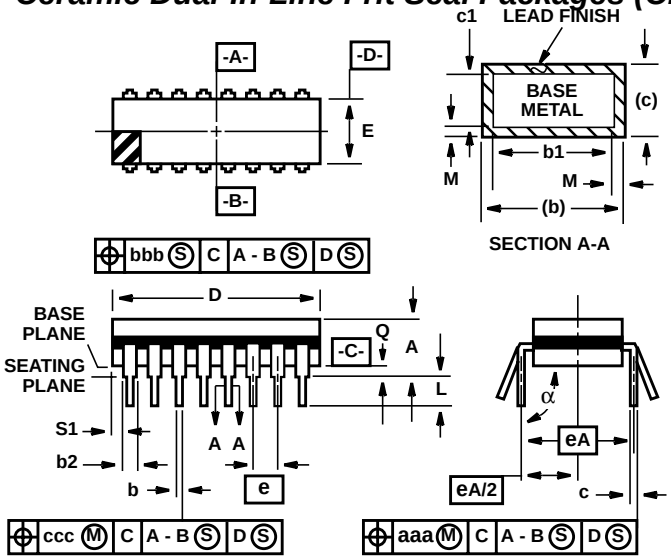
Floating (Recommend Connection to V-)

## Metallization Mask Layout

**HFA1110/883**



## Ceramic Dual-In-Line Frit Seal Packages (CERDIP)




**F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)**
**8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.405 | - | 10.29 | 5 |
| E | 0.220 | 0.310 | 5.59 | 7.87 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.300 BSC | | 7.62 BSC | | - |
| eA/2 | 0.150 BSC | | 3.81 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 6 |
| S1 | 0.005 | - | 0.13 | - | 7 |
| α | $90^o$ | $105^o$ | $90^o$ | $105^o$ | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2, 3 |
| N | 8 | | 8 | | 8 |

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.



## Sales Office Headquarters

**NORTH AMERICA**
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

**EUROPE**
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

**ASIA**
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029