



N-Channel 30-V (D-S) MOSFET

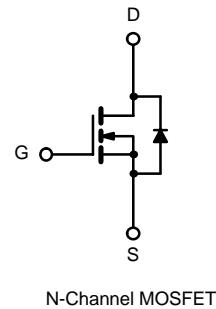
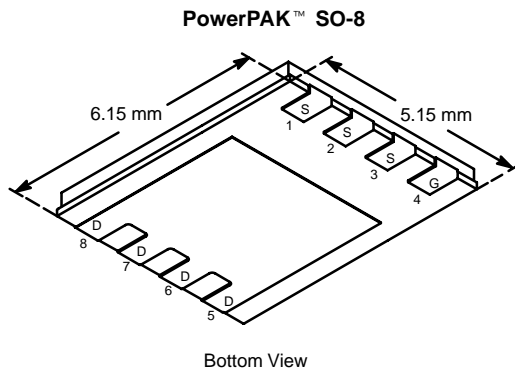
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0045 @ $V_{GS} = 10$ V	25
	0.0055 @ $V_{GS} = 4.5$ V	23

FEATURES

- TrenchFET® Power MOSFET
- Optimized for “Low Side” Synchronous Rectifier Operation
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile

APPLICATIONS

- DC/DC Converters
- Synchronous Rectifiers



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	30		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	25	14	A
		$T_A = 70^\circ\text{C}$	19	11	
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	60			
Continuous Source Current (Diode Conduction) ^a	I_S	4.5	1.6		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	5.4	1.9	W
		$T_A = 70^\circ\text{C}$	3.4	1.2	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	18	23	$^\circ\text{C/W}$
		Steady State	50	65	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.0	1.5		

Notes

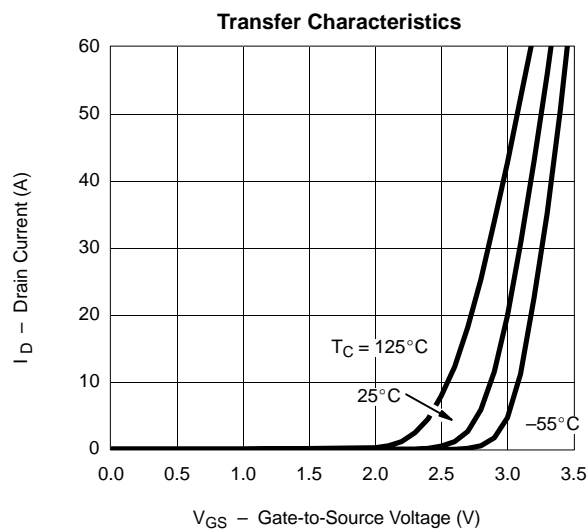
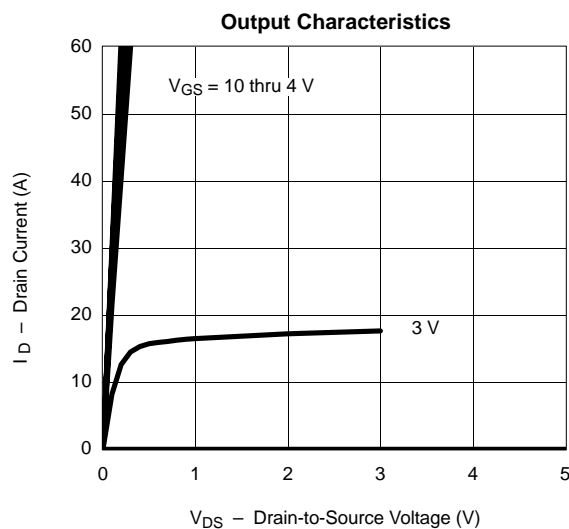
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0	1.95	3.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 25 A		0.0035	0.0045	Ω
		V _{GS} = 4.5 V, I _D = 19 A		0.0043	0.0055	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 25 A		95		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.9 A, V _{GS} = 0 V		0.72	1.1	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 25 A		34	50	nC
Gate-Source Charge	Q _{gs}			15		
Gate-Drain Charge	Q _{gd}			10		
Gate Resistance	R _G			1.3		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		21	35	ns
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			100	150	
Fall Time	t _f			30	45	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.9 A, di/dt = 100 A/μs		50	80	

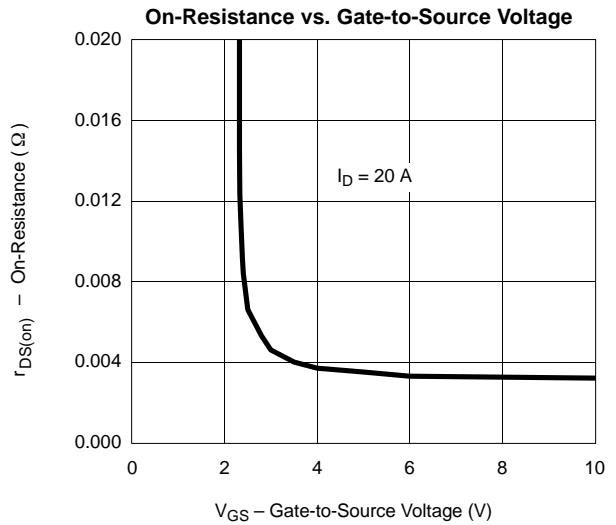
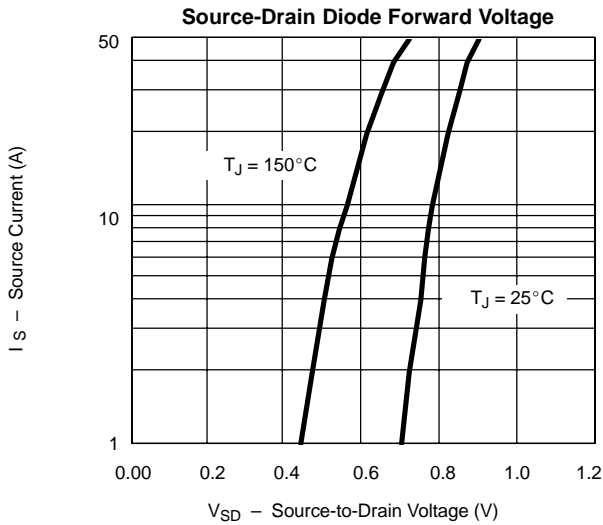
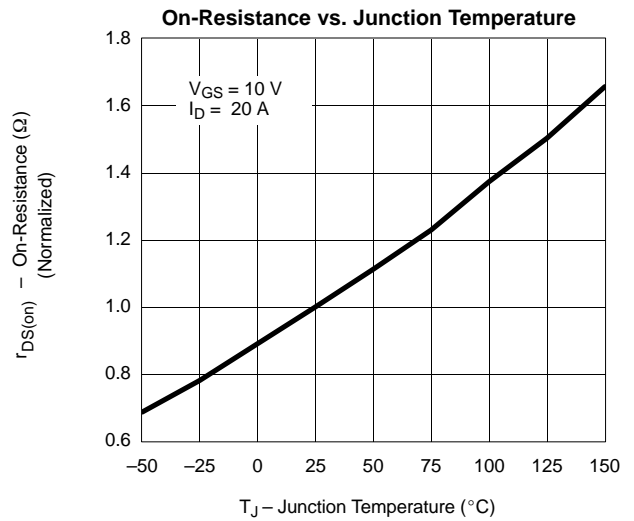
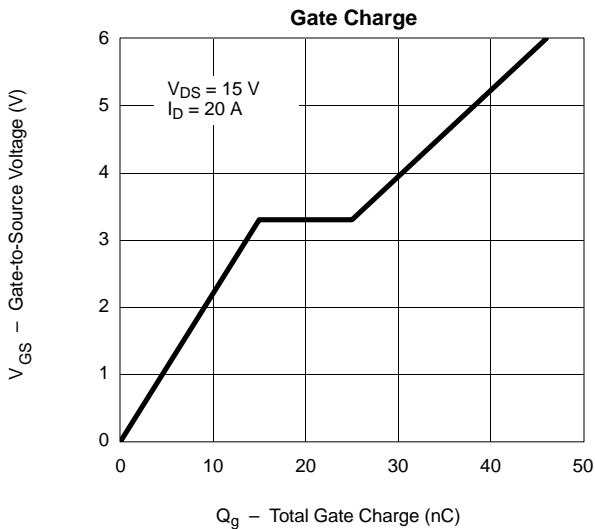
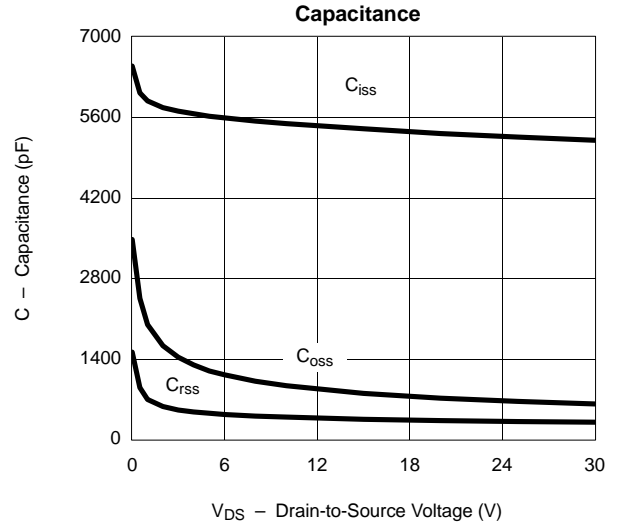
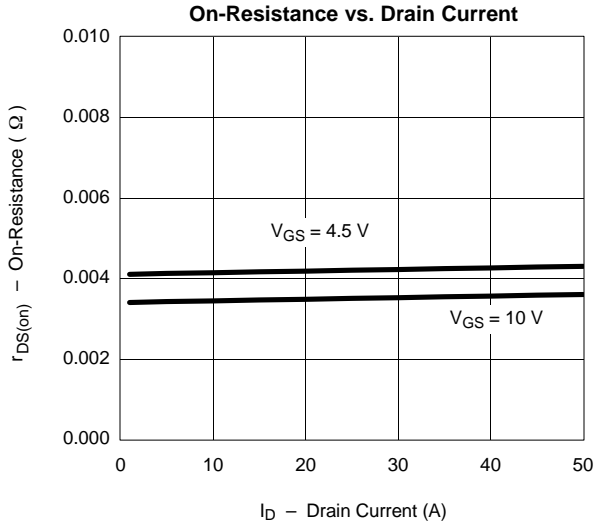
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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