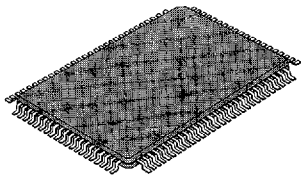
64 CHANNEL SEGMENT DRIVER FOR DOT MATRIX LCD

FUNCTION

The KS0108 is a LCD driver LSI with 64 channel output for dot matrix liquid crystal graphic display system. This device consists of the display RAM, 64 bit data latch 64 bit drivers and decoder logics. It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The KS0108 is composed of the liquid crystal display system in combination with the KS0107 (64 common driver)

100 QFP



FEATURES

- **Dot matrix LCD segment driver with 64 channel output.**
- **Input and output signal**
  - **— Input: 8 bit parallel display data**
    Control signal from MPU
    Splitted bias voltage (V_{1R}, V_{1L}, V_{2R}, V_{2L}, V_{3R}, V_{3L}, V_{4R}, V_{4L})
  - **— Output: 64 channel waveform for LCD driving.**
- **Display data is stored in display data RAM from MPU.**
- **Interface RAM**
  - **— Capacity: 512 bytes (4096 bits)**
  - **— RAM bit data: RAM bit data = 1:ON**
    RAM bit data = 0:OFF
- **Applicable LCD duty: 1/32 ~ 1/64**
- **LCD driving voltage: 8V ~ 17V**
- **Power supply voltage: +5V ± 10%**
- **High voltage CMOS process.**
- **100QFP and bare chip available.**

BLOCK DIAGRAM

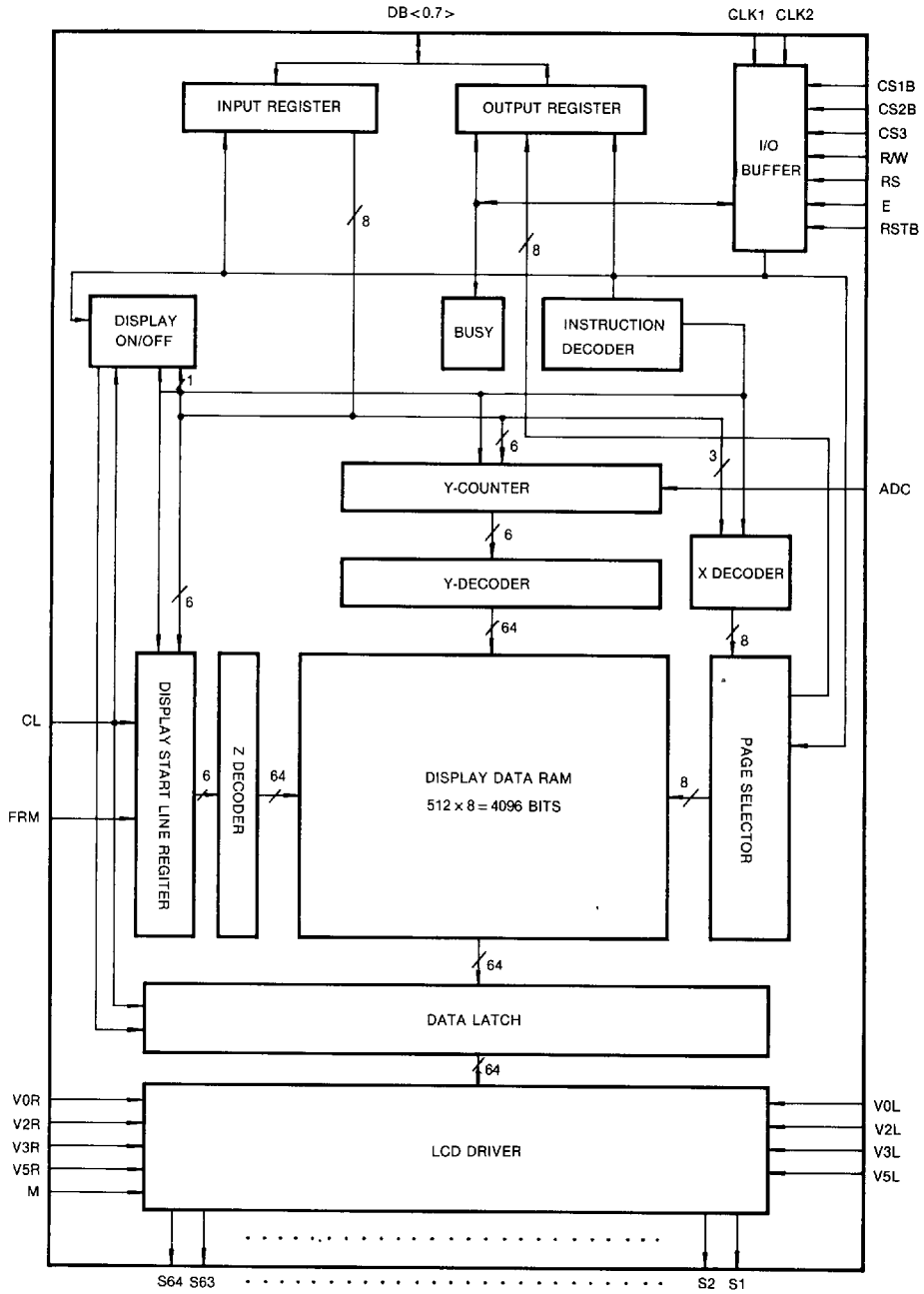


Fig. 1 KS0108 functional block diagram

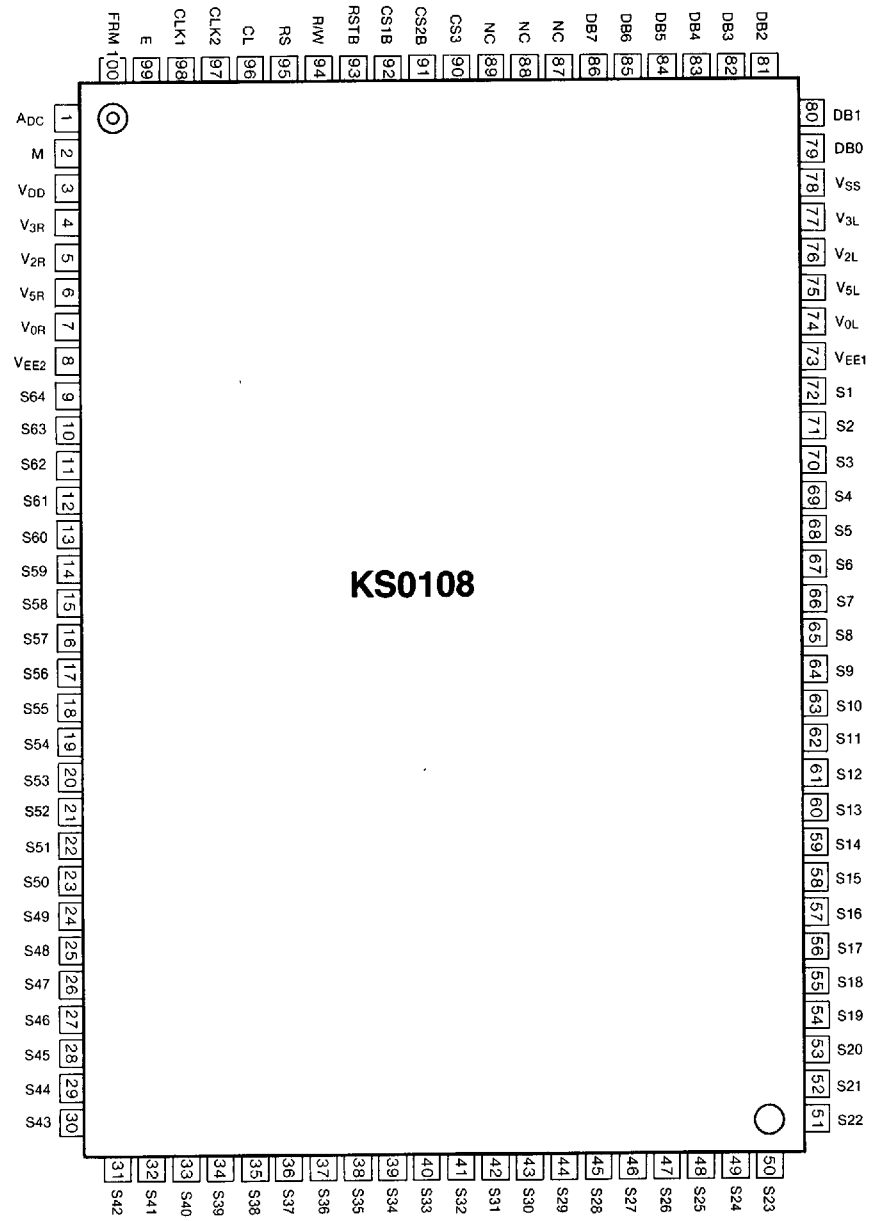


Fig. 2. 100QFP Top View

PIN DESCIPTION

Pin (No)	Symbol	Input/output	Function
3 78 73, 8	V_{DD} V_{SS} $V_{EE1,2}$	Power Power Power	Power supply for internal logic. Power supply for internal logic. Power supply for driving V_{SS} = 0V, V_{DD} = 5V ± 10% V_{DD}-V_{EE} = 8V ~ 17V V_{EE1} and V_{EE2} is connected by the same voltage.
74, 7 76, 5 77, 4 75, 6	V0L, V0R V2L, V2R V3L, V3R V5L, V5R	Power	Bias supply voltage terminals to drive the LCD. Select Level: V0L(R), V5L(R) Non-Select Level: V2L(R), V3L(R)
92 91 90	CS1B CS2B CS3	I	Chip selection In order to interface data for input or output The terminals have to be CS1B = L, CS2B = L and CS3 = H.
2	M	I	Alternating signal input for LCD driving.
1	ADC	I	Address control signal of Y address counter. ADC = H → DB<0:7> = 0 → Y0 → S1 DB<0:7> = 63→Y63→S64 ADC = L→DB<0:7> = 0→Y63→S64 DB<0:7> = 63→Y0→S1
100	FRM	I	Synchronous frame sinal. Presets the 6-bit Z counter and syncronizes the common signal with the frame signal when the frame signal becomes high.
99	E	I	Enable signal. write mode (R/W = L) → data of DB<0:7> is latched at the falling edge of E. read mode (R/W = H) → DB<0:7> appears the reading data while E is at high level.
98 97	CLK1 CLK2	I	2 phase clock signal for internal operation. Used to execute operations for input/output of display RAM data and others.
96	CL	I	Display synchronous signal. Display data is latched at rising time of the CL signal and increments the Z-address counter at the CL falling time.
95	RS	I	Data or Instruction. RS = H → DB<0:7> : Display RAM Data RS = L → DB<0:7> : Instruction Data
94	R/W	I	Read or Write. R/W = H → Data appears at DB<0:7> and can be read by the CPU while E = H, CS1B = L, CS2B = L and CS3 = H. R/W = L → Display data (DB<0:7>) can be written at falling of E when CS1B = L, CS2B = L and CS3 = H.
79 ~ 86	DB0 ~ DB7	I/O	Data bus. Three state I/O common terminal.

PIN DESCRIPTION (continued)

Pin (No)	Symbol	Input/output	Function
72~9	S1~S64	O	LCD Segment driver output. display RAM data 1:ON display RAM data 0:OFF (Relation of display RAM data & M) M / DATA / Output Level: 0 / 0 / V_2; 0 / 1 / V_0; 1 / 0 / V_3; 1 / 1 / V_5
93	RSTB	I	Reset signal. When RSTB = L, ① ON/OFF register becomes set by 0. (display off) ② Display start line register line becomes set by 0 (Z-address 0 set, display from line 0) After releasing reset, this condition can be changed only by instruction.
87~89	NC		No connection. (open)

MAXIMUM ABSOLUTE LIMIT (Ta=25° C)

Characteristic	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	$-0.3 \sim +7.0$	V	*1
	V_{EE}	$V_{DD}-19.0 \sim V_{DD}+0.3$	V	*4
Terminal voltage	V_I	$-0.3 \sim V_{DD}+0.3$	V	*1,3
	V_{LCD}	$V_{EE}-0.3 \sim V_{DD}+0.3$	V	*2
Operating temperature	T_{opr}	$-20 \sim +75$	°C	
Storage temperature	T_{stg}	$-55 \sim +125$	°C	

*1. Based on $V_{SS}=0V$.
*2. Applies the same supply voltage to V_{EE1} and V_{EE2}. $V_{LCD}=V_{DD}-V_{EE}$.
*3. Applies to M, FRM, CL, RSTB, ADC, CLK1, CLK2, CS1B, CS2B, CS3, E, R/W, RS and DB0~DB7.
*4. Applies $V_{OL(R)}$, $V_{2L(R)}$, $V_{3L(R)}$ and $V_{5L(R)}$.
Voltage level: $V_{DD} \geq V_{OL}=V_{OR} \geq V_{2L}=V_{2R} \geq V_{3L}=V_{3R} \geq V_{5L}=V_{5R} \geq V_{EE}$.

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD} = 4.5 ~ 5.5V, V_{SS} = 0V, V_{DD}-V_{EE} = 8 ~ 17V, Ta = −20 ~ +75°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit	Note
High input voltage	V_{IH1}		0.7V_{DD}		V_{DD}	V	1
	V_{IH2}		2.0		V_{DD}	V	2
Low input voltage	V_{IL1}		0		0.3V_{DD}	V	1
	V_{IL2}		0		0.8	V	2
High output voltage	V_{OH}	I_{OH} = −200[μA]	2.4			V	3
Low Output Voltage	V_{OL}	IOL=1.6[mA]			0.4	V	3
Input leakage current	I_{IL}	V_{IN} = V_{SS} ~ V_{DD}	−1.0		1.0	μA	4
Three-state(OFF) Input current	I_{TSL}	V_{IN} = V_{SS} ~ V_{DD}	−5.0		5.0	μA	5
Driver input leak. current	I_{IL1}	V_{IN} = V_{EE} ~ V_{DD}	−2.0		2.0	μA	6
Dissipation current	I_{DD1}	During Display			100	μA	7
	I_{DD2}	During Access Access Cycle = 1[MHZ]			500	μA	7
Driver ON resistance	RON	V_{DD}-V_{EE} = 15[V] ± ILOAD=0.1[mA]			7.5	KΩ	8

*1. CL, FRM, M, RSTB, CLK1, CLK2
2. CS1B, CS2B, CS3, E, R/W, RS, DB0 ~ DB7
3. DB0 ~ DB7
4. Excepted DB0 ~ DB7
5. DB0 ~ DB7 at High Impedance
6. $V_{OL(R)}$, $V_{2L(R)}$, $V_{3L(R)}$, $V_{5L(R)}$
7. 1/64 DUTY, FCLK = 250[KHZ], Frame Frequency = 70[HZ], Output: No Load
8. V_{DD} ~ V_{EE} = 15.5[V]
   $V_{OL(R)} > V_{2L(R)} = V_{DD} - 2/7\ (V_{DD} - V_{EE}) > V_{3L(R)} = V_{EE} + 2/7\ (V_{DD} - V_{EE}) > V_{5L(R)}$

AC CHARACTERISTICS (V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = −20°C ~ +75°C)

(1) Clock Timing

Characteristic	Symbol	Min	Typ	Max	Unit
CLK1, CLK2 cycle time	tcyc	2.5	—	20	us
CLK1 'LOW' level width	twl_{CLK1}	625	—	—	ns
CLK2 'LOW' level width	tw_{lCLK2}	625	—	—	ns
CLK1 'HIGH' level width	twh_{CLK1}	1875	—	—	ns
CLK2 'HIGH' level width	twh_{CLK2}	1875	—	—	ns
CLK1-CLK2 phase difference	td12	625	—	—	ns
CLK2-CLK1 phase difference	td21	625	—	—	ns
CLK1, CLK2 rise time	t_r	—	—	150	ns
CLK1, CLK2 fall time	t_f	—	—	150	ns

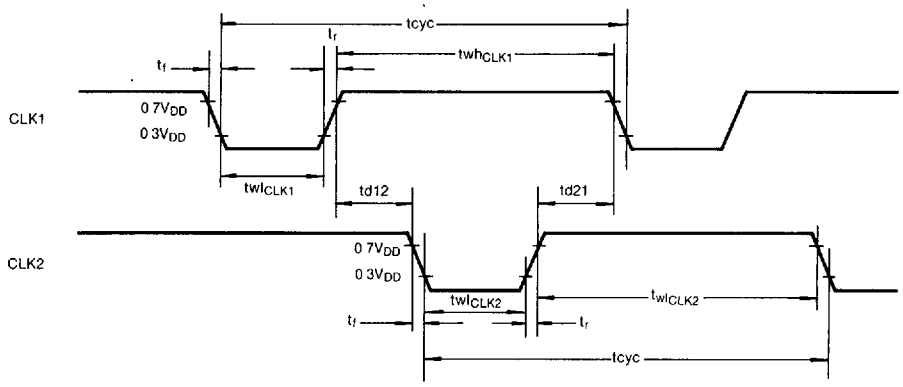


Fig 1. External clock waveform

(2) Display Control Timing

Characteristic	Symbol	Min	Typ	Max	Unit
FRM delay time	td_{FRM}	−2	—	+2	us
M delay time	td_{M}	−2	—	+2	us
CL 'LOW' level width	twl_{CL}	35	—	—	us
CL 'HIGH' level width	twh_{CL}	35	—	—	us

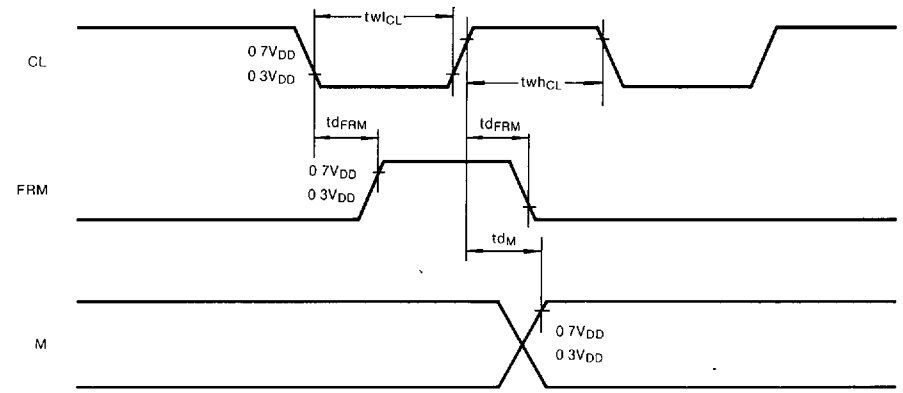


Fig 2. Display control signal waveform

(3) MPU Interface

Characteristic	Symbol	Min	Typ	Max	Unit
E cycle	tcyc	1000	—	—	ns
E high level width	twh_E	450	—	—	ns
E low level width	twl_E	450	—	—	ns
E rise time	t_r	—	—	25	ns
E fall time	t_f	—	—	25	ns
Address set-up time	t_{as}	140	—	—	ns
Address hold time	t_{ah}	10	—	—	ns
Data set-up time	tdsw	200	—	—	ns
Data delay time	tddr	—	—	320	ns
Data hold time (write)	tdhw	10	—	—	ns
Data hold time (read)	tdhr	20	—	—	ns

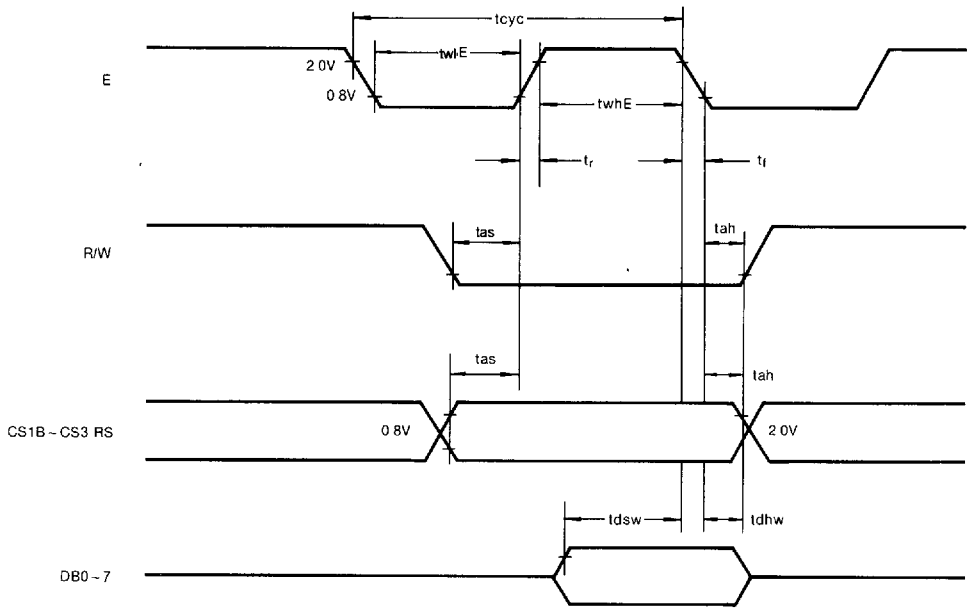


Fig 3. MPU write timing

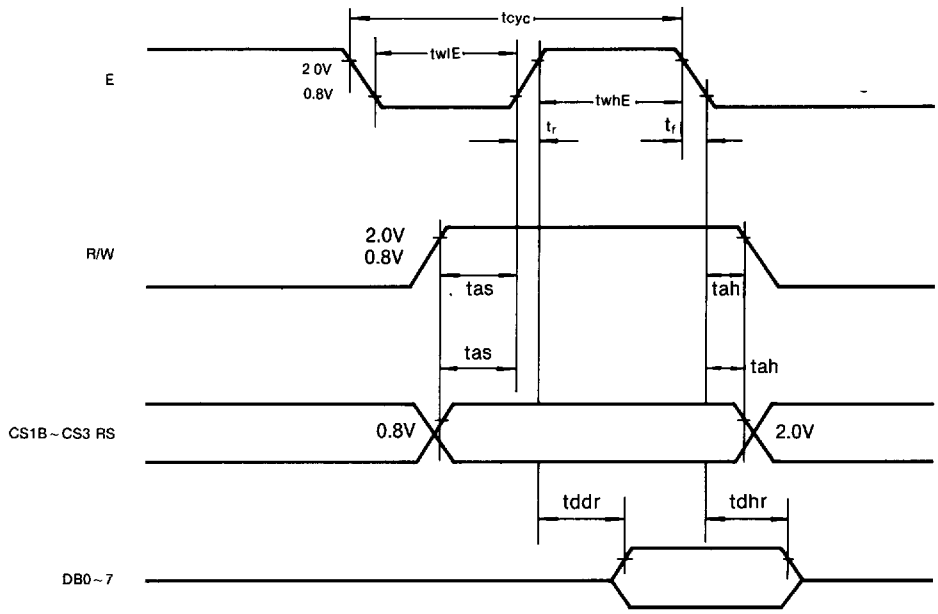


Fig 4. MPU read timing

OPERATING PRINCIPLES & METHODS

1. I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B ~ CS3.

2. Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.

When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then Writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

3. Output register

Output register stores the data temporarily from dispaly data RAM when CS1B, CS2B, CS3 is in active mode and R/W and RS = H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W = H, RS = L, status data (busy check) can read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
0	0	Instruction
	1	Status read (busy check)
1	0	Data write (from input register to display data RAM)
	1	Data read (from display data RAM to output register)

4. Reset

Reset can be initialized system by setting RSTB terminal at low level when turning power on, receiving instruction form MPU.

When RSTB becomes low, following procedure is occured.

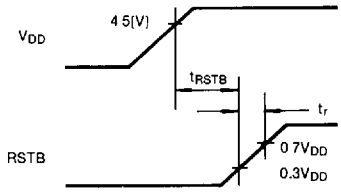
1. Display off
2. Display start line register become set by 0.(Z-address 0)

While RSTB is low level, no instruction except status read can be accepted. Reset status appears at DB4. After DB4 is low, any instruction can be accepted.

The Conditions of power supply at initial power up are shown in table 1.

Table 1. Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RSTB}	1.0	—	—	us
Rise time	t_r	—	—	200	ns



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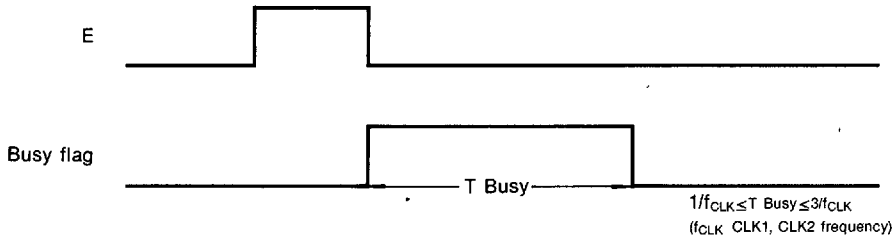
5. Busy flag

Busy flag indicates that KS0108 is operating or no operating. When busy flag is high, KS0108 is in internal operating. When busy flag is low, KS0108 can accept the data or instruction.

DB7 indicates busy flag of the KS0108.



6. Display On/Off Flip-Flop

The display on/off flip-flop makes on/off of the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logical high), non selective voltage appears on segment output terminals regardless of display RAM data.

The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low.

The status of the flip-flop is output to DB5 by status read instruction.

The display on/off flip-flop synchronizes by CL signal.

7. X Page Register

X page register designates page of the internal display data RAM.

It has not count function. An address is set by instruction.

8. Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

9. Display Data RAM

Display data RAM stores a display data for liquid crystal dispaly. To express on state of dot matrix of liquid crystal display, write data 1. The other way, off state writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

ADC = H ⇒(DB<0:7>=0 – Y-address 0 – A0 – S1
DB<0:7>=63 – Y-address 63 – A63 – S64
ADC = L ⇒(DB<0:7>=0 ~ Y-address 63 – A63 – S64
DB<0:7>=63 ~ A0 – S1

ADC terminal connect the V_{DD} or V_{SS}.

10. Display Start Line Register

The display start line register indicates address of display data RAM to display top line of liquid crystal dispaly.

Bit data (DB<0:5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.

It is used for scrolling of the liquid crystal display screen.

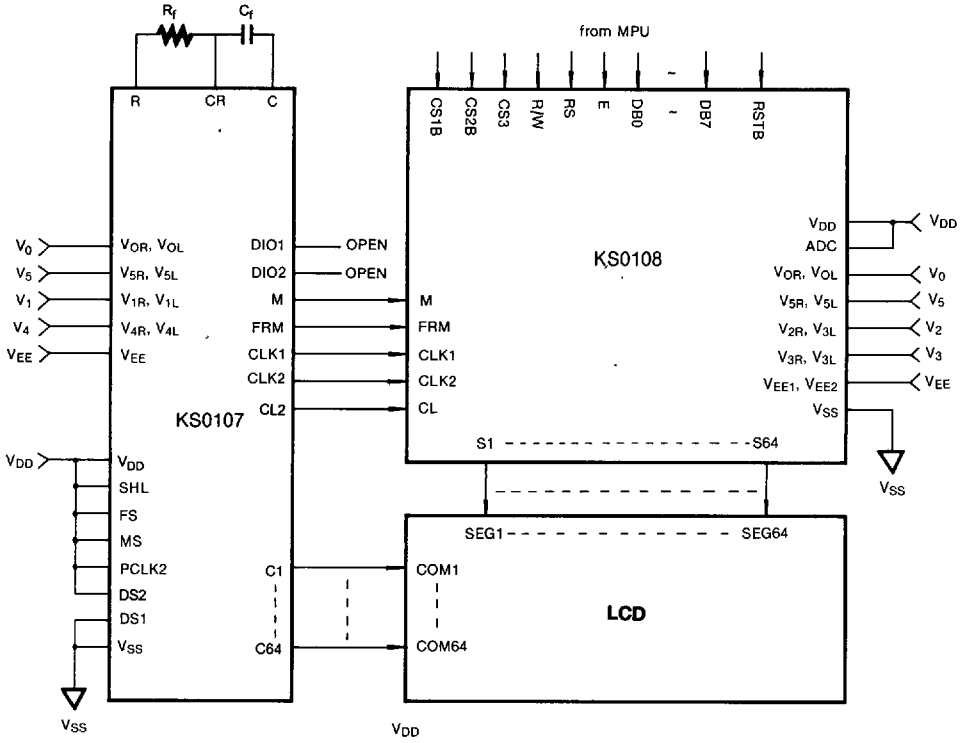
DISPLAY CONTROL INSTRUCTION

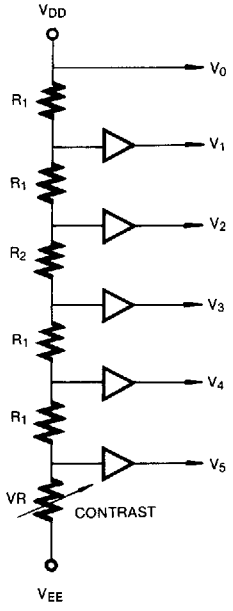
The display control instructions control the internal state of the KS0108. Instruction is received form MPU to KS0108 for the display control. The following table shows various instructions.

Instruction	R S	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display ON/OFF	0	0	0	0	1	1	1	1	1	0/1	Controls the display on or off. Internal status and display RAM data is not affected. 0:OFF, 1:ON
Set Address	0	0	0	1	Y address (0~63)						Sets the Y address in the Y address counter.
Set Page (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the display data RAM displayed at the top of the screen.
Status Read	0	1	BUSY	0	ON/OFF	RESET.	0	0	0	0	Read status. BUSY 0: Ready 1: In operation ON/OFF 0: Display ON 1: Display OFF RESET 0: Normal 1: Reset
Write Display Data	1	0	Write Data								Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read Display Data	1	1	Read Data								Reads data (DB0:7) from display data RAM to the data bus.

APPLICATION CIRCUIT

1. 1/64 duty common driver (KS0107) interface circuit





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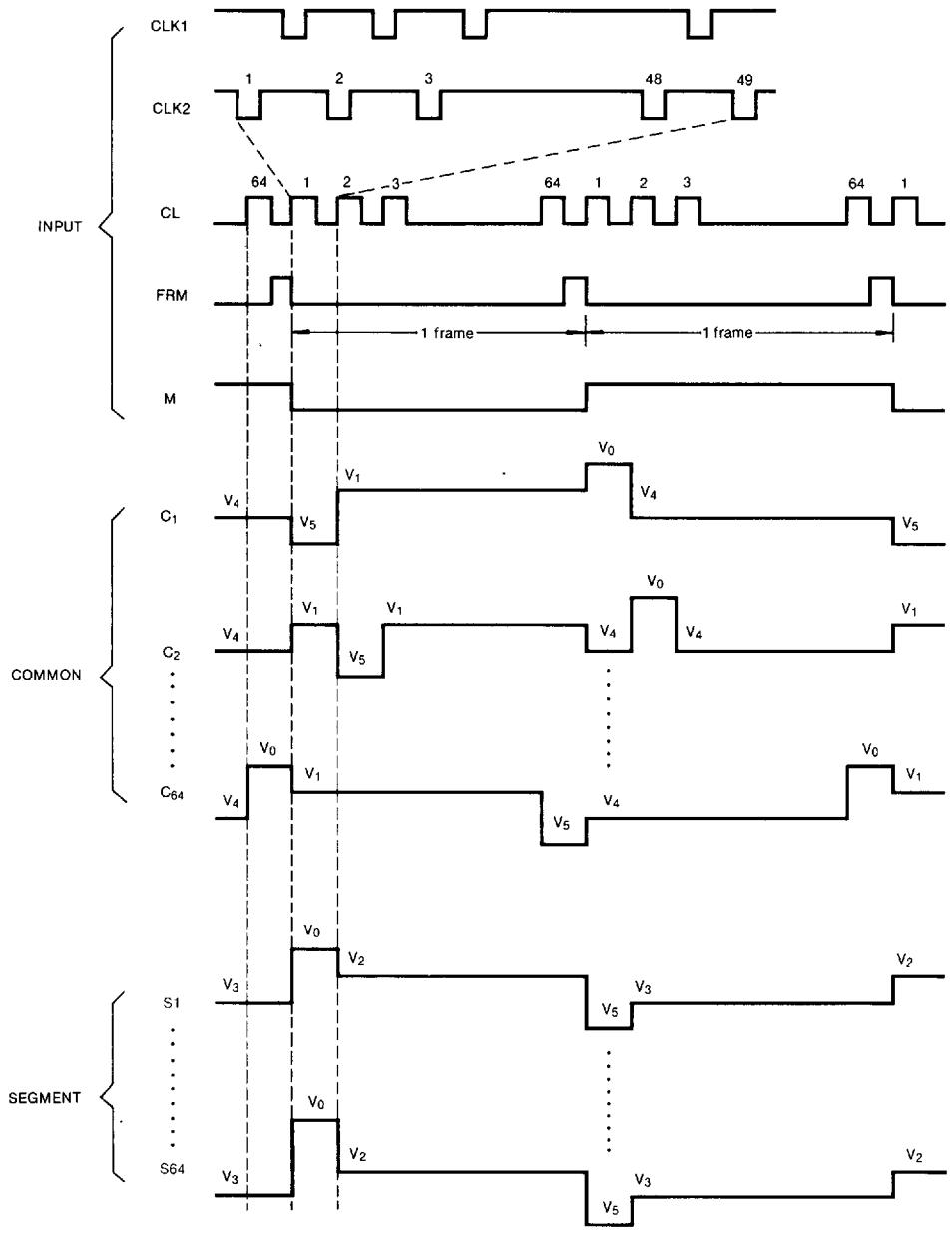
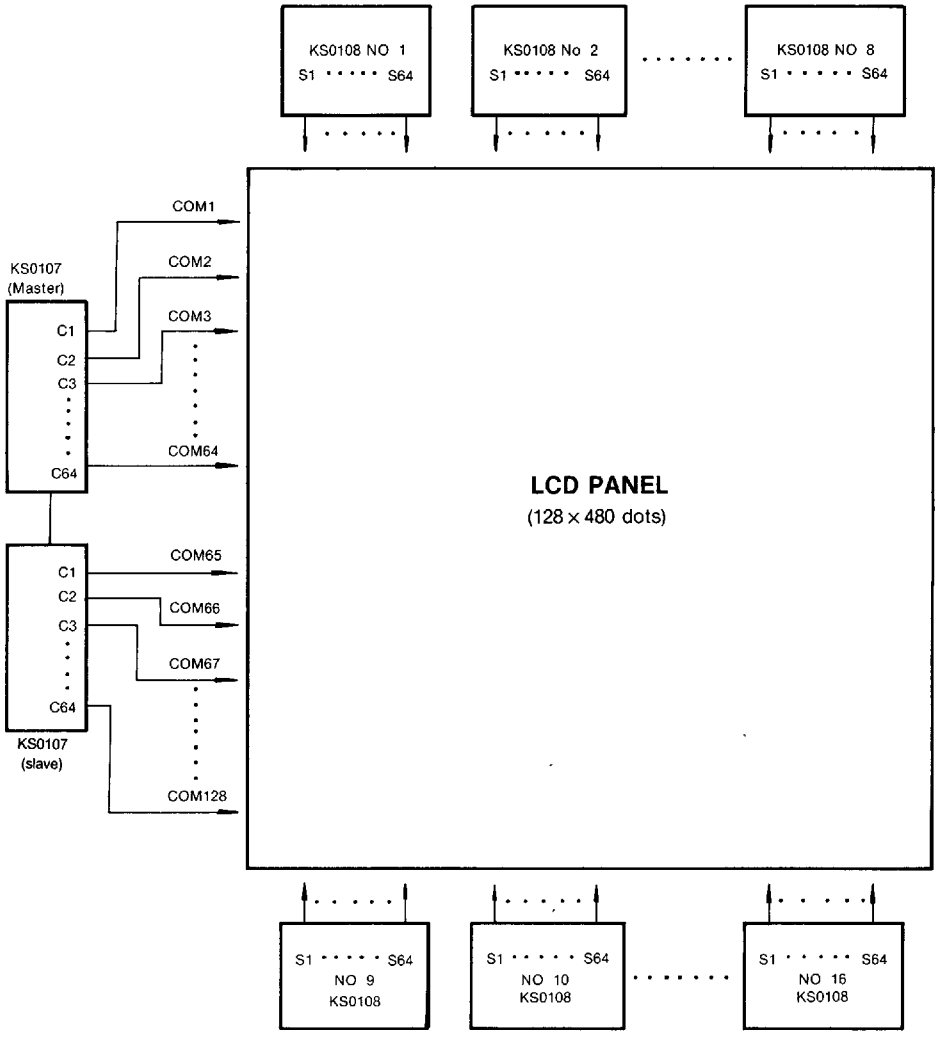
2. Timing diagram (1/64 duty)



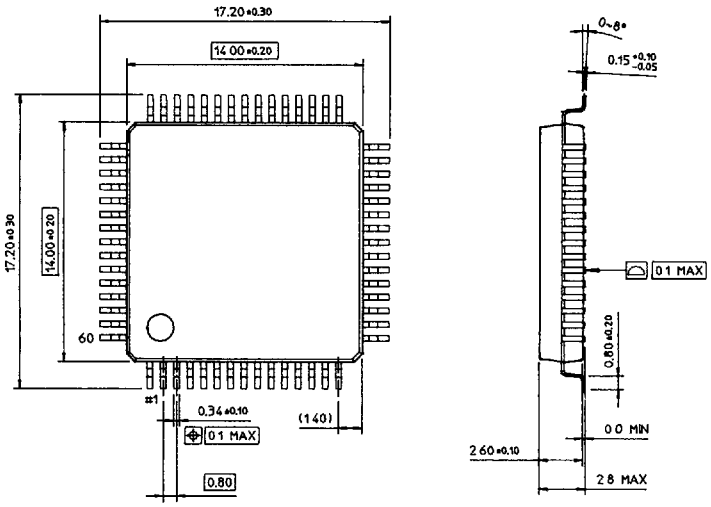
3. LCD Panel interface application circuit



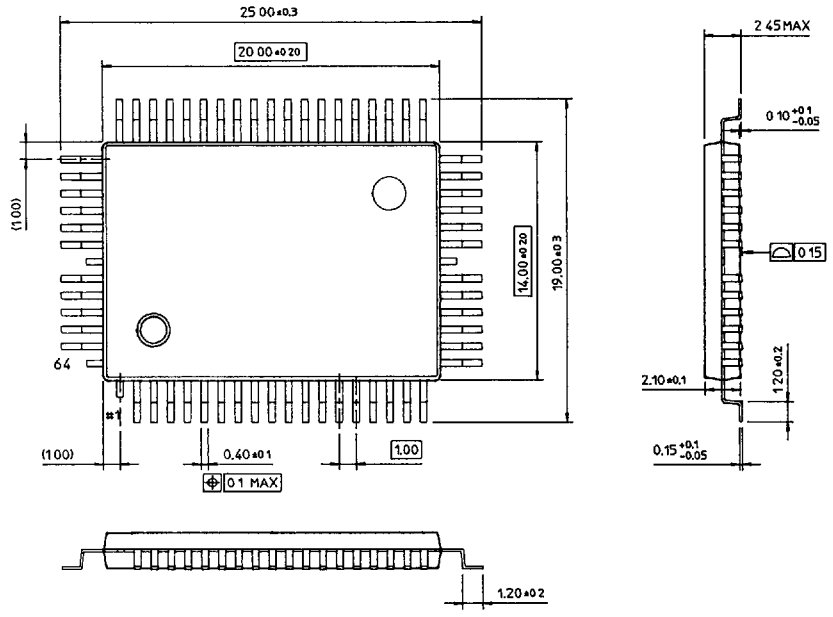
PACKAGE DIMENSIONS

Dimensions in Milimeters

60-QFP-1414A



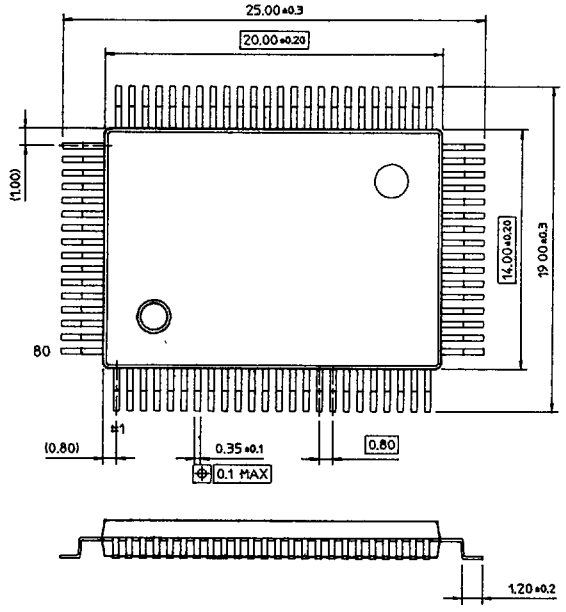
64-QFP-1420D



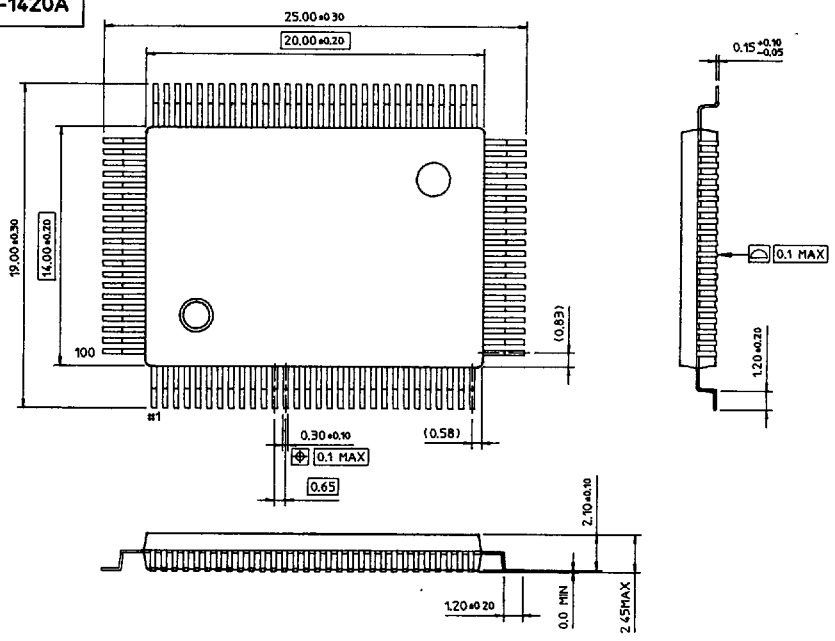
PACKAGE DIMENSIONS

Dimensions in Milimeters

80-QFP-1420A



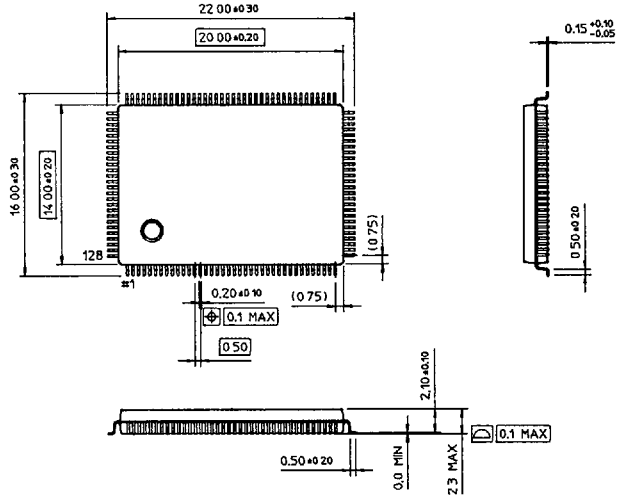
100-QFP-1420A



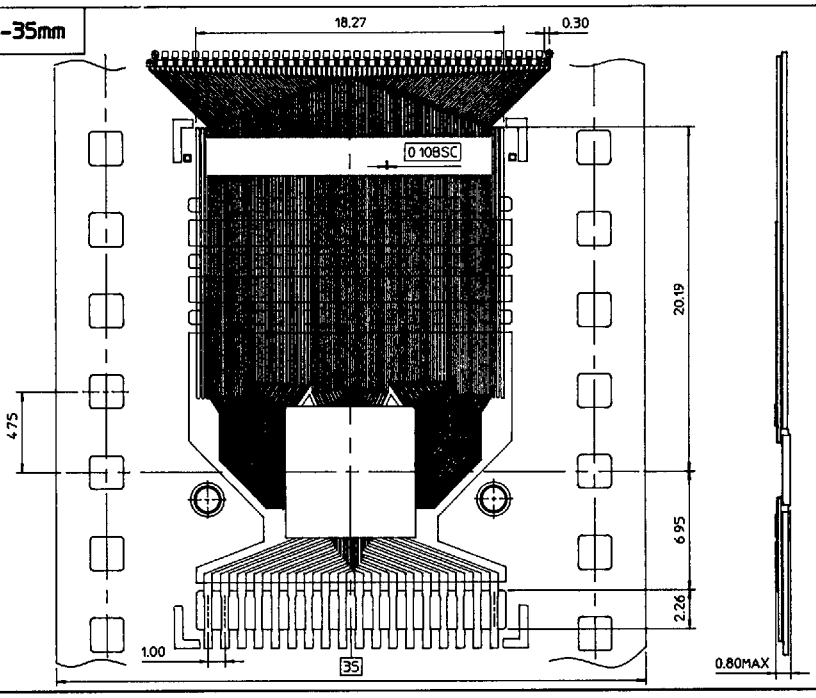
PACKAGE DIMENSIONS

Dimensions in Milimeters

128-QFP-1420



98-TAB-35mm



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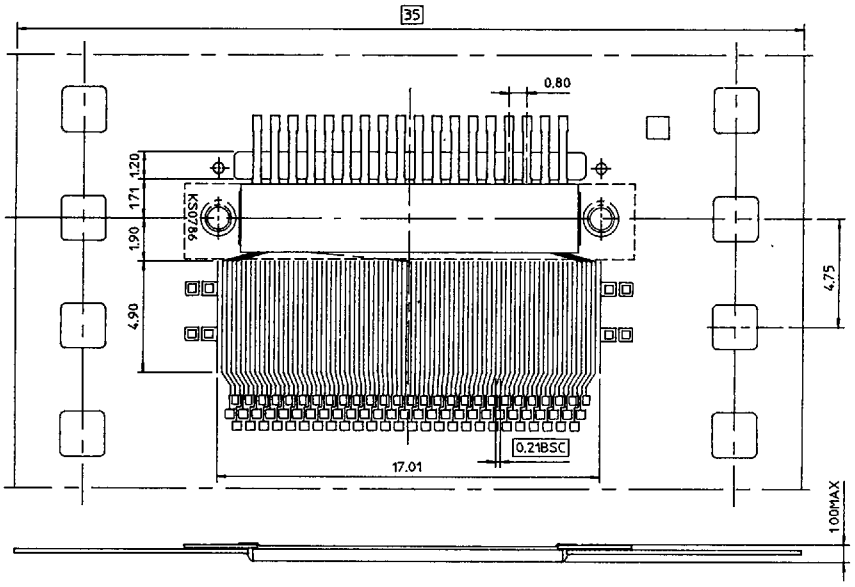
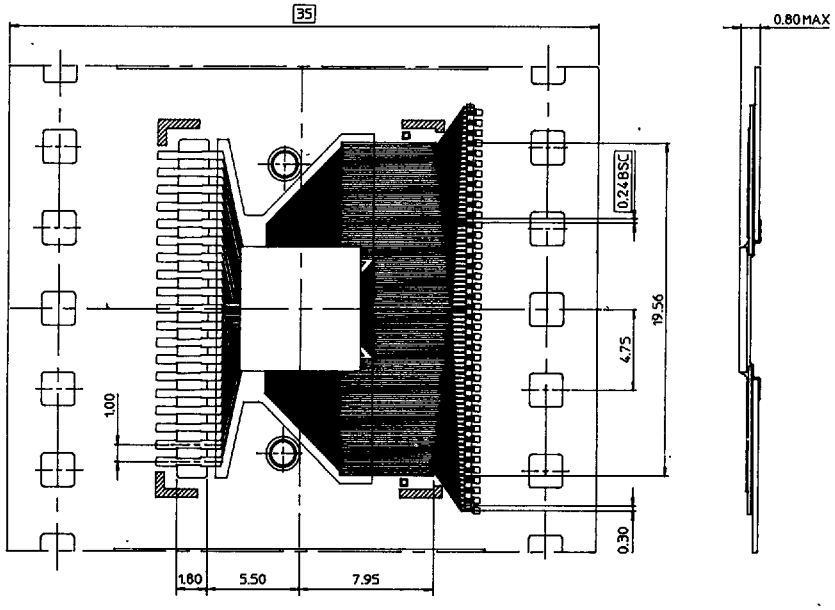
PACKAGE DIMENSIONS

Dimensions in Milimeters

98-STAB-35mm



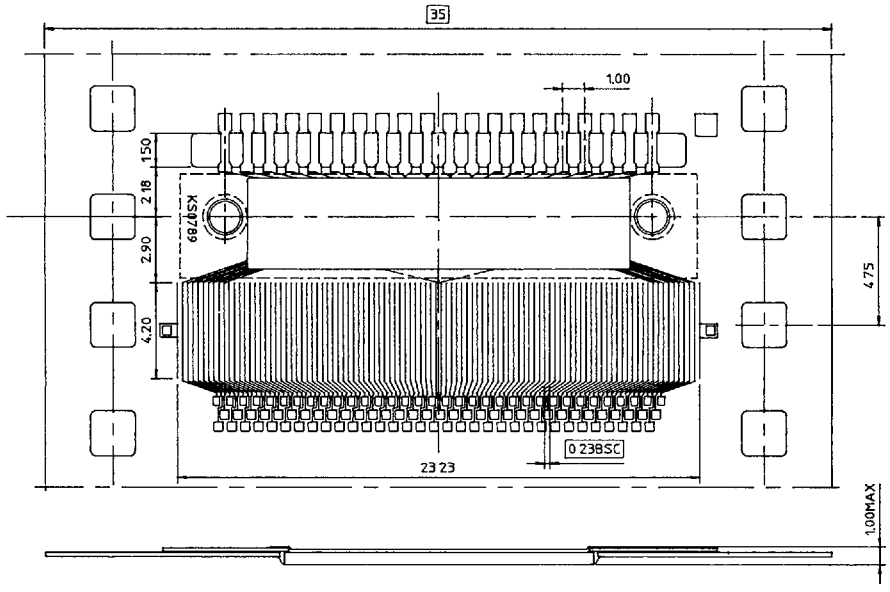
99-TAB-35mm



PACKAGE DIMENSIONS

Dimensions in Milimeters

120-STAB-35mm



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