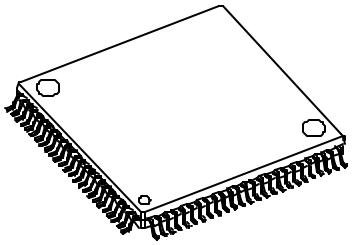
USBvision™ II

ZR36504

Video & Audio Interface solution via USB

Data Sheet



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to support or sustain life, or for any other application in which the failure of the Zoran product could create a situation where personal injury or death may occur.

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ZR36504 - Full Video and Audio Interface solution for Video via USB

The ZR36504 is an ideal solution for digital camera manufacturers who want to utilize the Universal Serial Bus as an interface between the camera and the computer. Using a proprietary video compression algorithm, the ZR36504 enables a throughput of up to 30f/s for CIF size images and up to 15f/s for VGA size images, utilizing only half of total available bandwidth of the USB port. An appropriate software driver in the host computer de-compresses the incoming USB data, consuming only 25% of CPU time (@ CIF 30f/s). The resulting digital image quality is almost identical to the source coming from the camera. This monolithic feature of the ZR36504 makes it ideal to be used as a one chip solution for a very low cost USB portable Video Camera.

The ZR36504 can also be used to transfer video sequence from a Composite-Video source to the computer for editing (this requires an additional video decoder chip). Due to the fact that the USB bandwidth used by the ZR36504 can be adjusted (0.5-7.5 Mbit/sec), the video software application always has enough time to record the incoming compressed video data on disk and display full frame-rate on screen simultaneously.

The ZR36504 is compatible with the NT1003-1, but has a smaller package. It supports simultaneous Serial Digital Audio input and simultaneous external Bulk-Data input as well, and eliminates the need for an external EEPROM to set a specific manufacturer USB ID code. The ZR36504 also supports 16 Mbit DRAMs for a better quality VGA video and still capture.

Features

- Up to 30 frames/sec @ CIF size (352x288 pixels)
- Up to 15 frames/sec @ VGA size (640x480 pixels)
- Connects to various YUV sources (4:4:4, 4:2:2, 16 or 8-bit bus)
- Selectable Raw/Compressed video out
- Variable Compression ratio
- Selectable USB bandwidth (0.5Mbps - 7.5Mbps in 0.5Mbps steps):
- Built-in programmable true scaler (Down Scale - horizontal and vertical)
- Built in Zoom and Pan capabilities
- Supports high resolution still image capture (640x480 pixels)
- Supports serial Digital Audio input (8K/16K samp/sec, 8-bit µ-Law / 16-bit linear)
- Auxiliary simultaneous external serial Bulk-data input (0 to 2Mbit/sec).
- Selectable Data/Clock serial protocols - ideal for camera control
- Low power consumption (190mW @ 3.3V) - can use USB power source
- Direct connection to USB port
- Handles device Power Management (complies with USB standard spec.)
- Fits Intel's MMX® concept
- Supports most popular software applications that require digital video.
- Available in 100-pin PQFP and TQFP packages

Product Description

Refer to Fig.1 for an internal Block Diagram of the ZR36504.

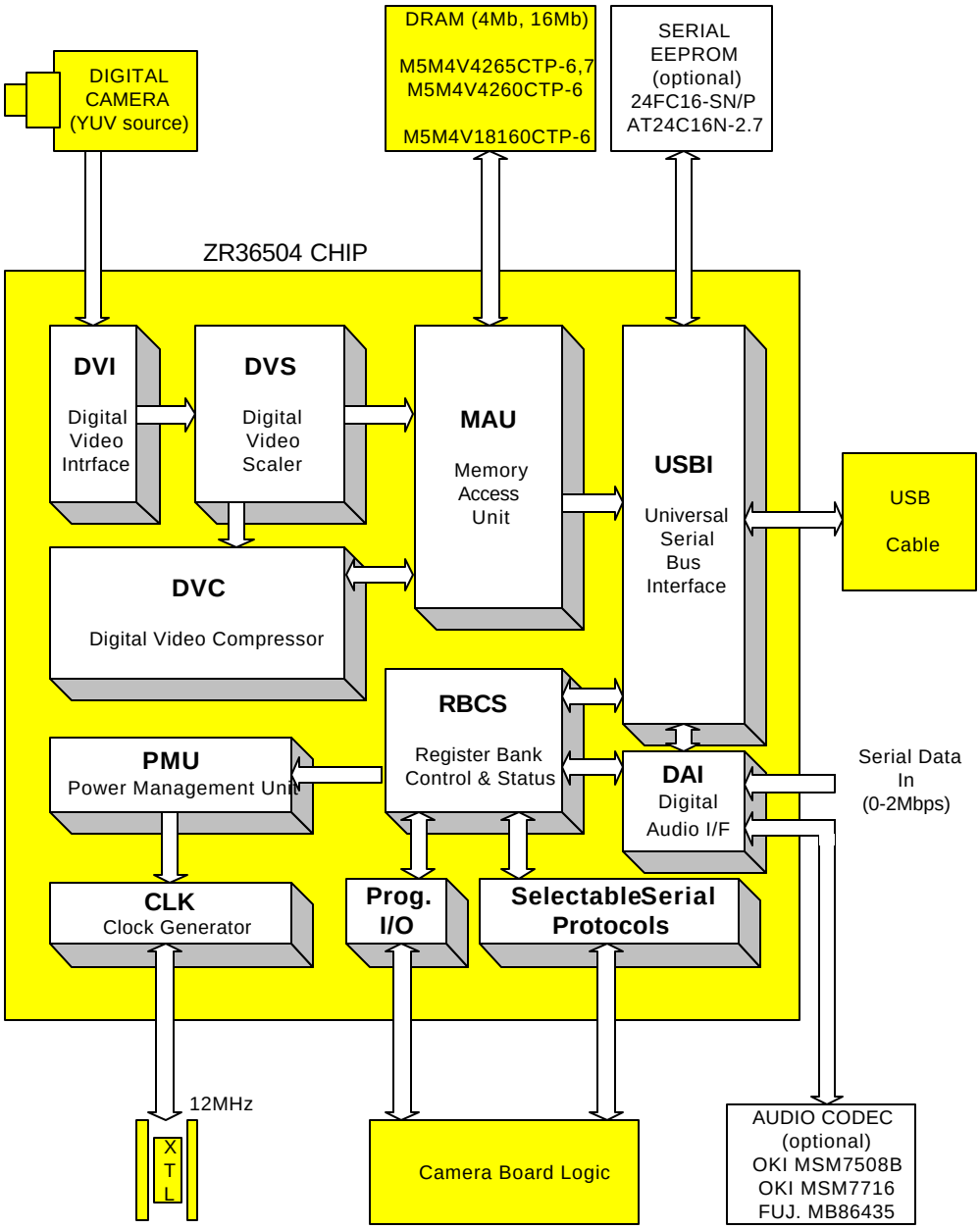


Fig.1 ZR36504 Block Diagram

The ZR36504 utilizes a single USB port to enable the host computer to access 4 different data channels simultaneously. These 4 channels are the Digital Video input (7.5Mbit/sec), Digital Audio input, Serial Bulk data input, and I/O control (internal registers, programmable I/O pins, and selectable Data/Clock serial protocols).

Due to the sophisticated architecture and protocol of the USB, the software application is not required to take care of the time-sharing management of several tasks using a single serial bus; This is handled by the lower-level drivers, so that the application program can access each function of the ZR36504 independently.

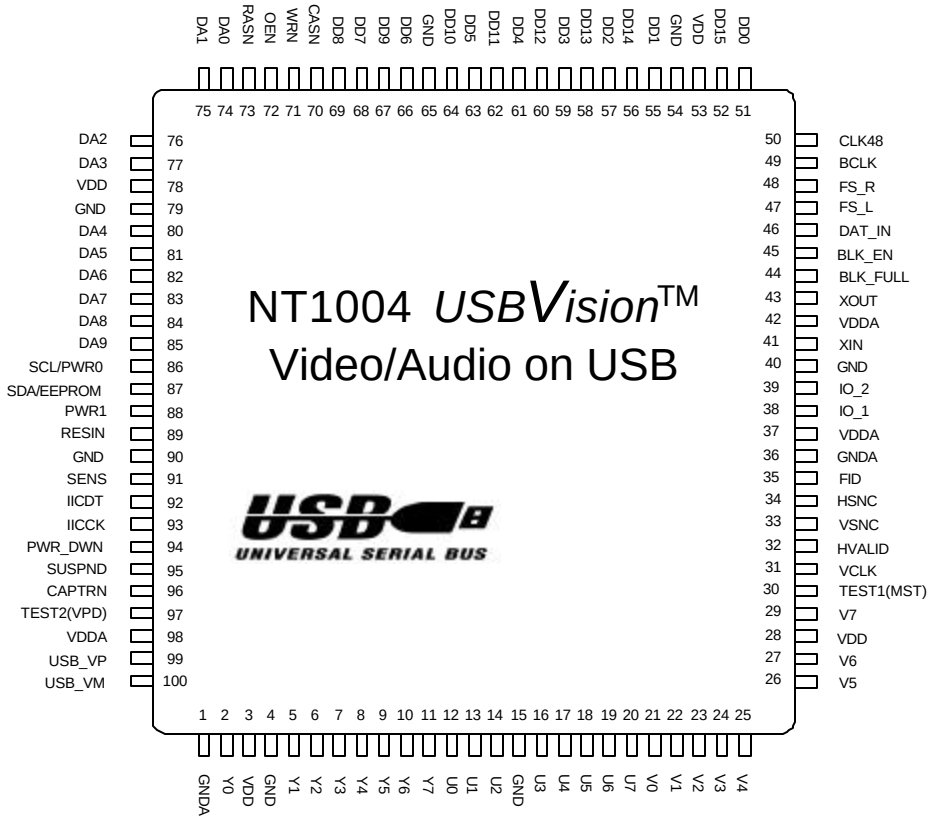
In normal operation, the ZR36504 will provide the system with the following services:

- **Compressed Video Channel:** The ZR36504 connects to a Y/U/V video digital source, scales the image on the fly horizontally and vertically, compresses the data down to 0.5-7.5Mbit/sec, and sends it to the host computer via the USB port. The ZR36504 scaler supports zoom-in like effects, by applying combinations of zooming and cropping built-in functions. The unique method of compression is a special design of Zoran, to allow easy and fast de-compression in software only means. The de-compression software driver supplied with the ZR36504, will accept the compressed data and convert it back to standard video formats in less time than it takes to read raw video from any external port. Still images can be captured and sent via the USB in the best quality and resolution that the camera can provide.

- **Sound System: Some** camera applications require that a microphone sound system will be implemented inside the camera. Also, a Composite-Video to USB adapter applications requires audio recording support as well. The ZR36504 provides solution for these applications, by multiplexing a serial digital audio input with the video data that is sent via USB port. In such a system, the microphone can be located inside the camera, up to 5 meters away from the host computer. The ZR36504 does not include the audio A/D, and is designed to use an external low-cost telephony audio codec.

- **Camera Control:** Camera (or any video source) control and status monitoring can be carried out by a built-in serial interface, or direct I/O pins. The serial interface supports some commonly used serial protocols. These ports can be used by the application software to control and monitor some other remote devices as well. In a Video Conference application, this allows the local or remote user to set the focus, zoom, and other parameters of the camera, or even to switch the camera to the power-down mode. The ZR36504 also supports usage of an external capture button that is mounted on the camera board and used for capturing video frames on the host computer disk (this is application dependent; the ZR36504 only delivers the capture command signaling from button to host computer via USB).

Pin Assignments (Top View)



PIN DESCRIPTIONS

PIN NUMBER	SIGNAL	I/O	DESCRIPTION
3, 28, 53, 78	VDD		Digital 3.3V power supply
37, 42, 98	VDDA		Analog 3.3V supply. 37:PLL, 42:OSC, 98:USB
4, 15, 40, 54, 65, 79, 90	GND		Digital ground connection
1, 36	GNDA		Analog ground connection. 1:USB, 36:PLL
2, 5-11	Y0-Y7	I	Video Luminance input from camera. The ZR36504 uses the VCLK input to sample this bus. These input pins are 5-volt tolerant with P.D
12-14,16-20	U0-U7	I	Video Chroma U or U/V-components input from camera. The ZR36504 uses the VCLK input to sample this bus. These input pins are 5-volt tolerant with P.D.
21-27, 29	V0-V7	I	Video Chroma V-component input from camera. The ZR36504 uses the VCLK input to sample this bus in the 24-bit format mode. V2-V0 inputs are also used to set the *idProduct* code. V7-V3 inputs are also used to set the *idVendor* code. These input pins are 5-volt tolerant. Should be connected to GND if not used.
30	TEST1(MST)	I	This pin must be connected to GND.

31	VCLK	I	Video Pixel-Clock input from camera. This input pin is 5-volt tolerant.
32	HVALID	I	Video Clock Enable input qualifier. This input pin is 5-volt tolerant. Should be connected to GND if not used.

PIN DESCRIPTIONS (continued)

PIN NUMBER	SIGNAL	I/O	DESCRIPTION
33	VSNC	I	Video Vertical-Sync input signal from camera. This input pin is 5-volt tolerant. Should be connected to GND if not used.
34	HSNC	I	Video Horizontal-Sync input signal from camera. This input pin is 5-volt tolerant. Should be connected to GND if not used.
35	FID	I	Video Field-ID input signal from camera. This input pin is 5-volt tolerant. Should be connected to GND if not used.
38-39	IO-1 - IO-2	I/O	General Programmable I/O pins. Each of these 2 pins has an Open Drain 5v tolerant output, and it is supposed to be connected to an external pull-up resistor. The host uses these pins as programmable output ports by writing '0' or '1'. By writing '1' and read back, the host can use these pins as input ports - as this allows any external source to force the pull-up resistor. These outputs are temporarily set to high-z while in the Suspend position.
41	XIN	I	Crystal Oscillator input pin (12 MHz). Crystal frequency must have not worse than 100 PPM accuracy.
43	XOUT	O	Crystal Oscillator output pin (12 MHz).
44	BLK_FULL	O	"Bulk-Fifo full" indication output signal. This output signal is normally '0', and is set to '1' when the ZR36504 Bulk-Fifo is full. This output is temporarily set to '0' while in the Suspend or Power-Down position.
45	BLK_EN	I	Bulk Data Enable input. When set to '1', Bulk input data from DAT_IN pin is sampled-in by falling edge of BCLK into the ZR36504 Bulk-Fifo. This input pin is 5-volt tolerant.
46	DAT_IN	I	Data Input pin for both Audio CODEC Tx chan and Bulk Data in. This input pin is 5-volt tolerant, and requires an external pull-up resistor.
47	FS_L	O	Audio Codec Frame-Sync pulse for Left channel. This signal triggers the beginning of a new audio sample (left chan.) . This output is temporarily set to '0' while in the Suspend or Power-Down position.
48	FS_R	O	Audio Codec Frame-Sync pulse for Right channel. This signal triggers the beginning of a new audio sample (right chan.) . This output is temporarily set to '0' while in the Suspend or Power-Down position.
49	BCLK	O	Main Clock for both Audio CODEC and Bulk Data in. This output is temporarily set to '0' while in the Suspend or Power-Down position.
50	CLK48	O	48MHz Clock output for user application. This output is temporarily set to '0' while in the Suspend or Power-Down position.
51-52,55-64,66-69	DD0-DD15	I/O	DRAM Data bus input/output pins. These pins have internal Pull-Down resistors, and are temporarily set to High-Z while in the Suspend or Power-Down position..
70	CASN	O	DRAM Column-Select control signal. This output is designed to drive 2 input pins of the external DRAM that are tied together (LCAS+UCAS). This output is temporarily set to High-Z while in the Suspend or Power-Down position.
71	WRN	O	DRAM Write control signal. This output is temporarily set to High-Z while in the Suspend or Power-Down position.

72	OEN	O	DRAM Read control signal. This output is temporarily set to High-Z while in the Suspend or Power-Down position.
73	RASN	O	DRAM Row-Select control signal. This output is temporarily set to High-Z while in the Suspend or Power-Down position.
74-77, 80-84	DA0-DA8	O	DRAM Row/Column Address-bus. These outputs are temporarily set to '0' while in the Suspend or Power-Down position.
85	DA9	O	DRAM Row/Column MSbit of Address-bus. This outputs is used for 16M DRAMs, and temporarily set to '0' while in the Suspend or Power-Down position.

PIN DESCRIPTIONS (continued)

PIN NUMBER	SIGNAL	I/O	DESCRIPTION
86	SCL/PWR0	I/O	Serial EEPROM clock signal, and LSbit of Device Power Code. If an EEPROM was detected, then this pin is used as the EEPROM clock output signal; otherwise its voltage (Vdd or GND) is used by the ZR36504 as the LSbit of the Device Power Code for the USB Device Descriptor. If EEPROM is detected, this pin is temporarily set to '1' while in the Suspend position.
87	SDA/EEPROM	I/O	Serial EEPROM data signal, and EEPROM Detect pin. If EEPROM is used, a 10KΩ pull-up resistor to Vdd should be connected to this pin; otherwise it should be tied to GND. During a Reset operation the ZR36504 samples the voltage level on this pin, to determine if an external EEPROM exists. This pin has an Open Drain output, and is temporarily set to high-z while in the Suspend position.
88	PWR1	I	MSbit of Device Power Code. The voltage level in this input (Vdd or GND) is used by the ZR36504 as the MSbit of the Device Power Code for the USB Device Descriptor. If an external EEPROM exists, this input is ignored.
89	RESIN	I	Power-On Reset input. This input is Schmitt-Trigger type, and it is active low.
91	SENS	O	Serial control Enable Signaling. This pin has an Open Drain output, and is 5v tolerant. It should be connected to an external 3.3-10KΩ pull-up resistor. This output is temporarily set to high-z while in the Suspend or Power-Down position.
92	IICDT	I/O	Camera-Control Data I/O (supports some commonly used serial protocols). This pin has an Open Drain output, and is 5v tolerant. It should be connected to an external 3.3-10KΩ pull-up resistor. This output is temporarily set to high-z while in the Suspend or Power-Down position.
93	IICCK	O	Camera-Control Clock output (supports some commonly used serial protocols). This pin has an Open Drain output, and is 5v tolerant. It should be connected to an external 3.3-10KΩ pull-up resistor. This output is temporarily set to high-z while in the Suspend or Power-Down position.
94	PWR_DWN	O	Camera Power-Down control. This is an Open Drain 5v tolerant output. The ZR36504 uses this output to switch On/Off the camera and/or external circuit. Upon Reset operation to the ZR36504, this output is set to high-z (=Off). It is also set to high-z in the Suspend position, and remains high-z after Suspend position is over.
95	SUSPND	O	USB Suspend mode control output. This pin is an Open Drain 5v tolerant output. A Power-On Reset or a USB-Reset clear this output to 0 volt; it is set to high-z when the ZR36504 enters the Suspend mode, and cleared back to '0' upon detection of Resume condition.
96	CAPTRN	I	Capture Command input. This input has an internal pull-up to Vdd. When forced to '0', host computer is automatically informed that a video frame capture was requested by user. This input is Schmitt-Trigger type.
97	TEST2(VPD)	I	This pin must be connected to GND.
99	USB_VP	I/O	Universal-Serial-Bus Positive data line; This line should be connected to an external pull-up resistor of 1.5KΩ. Refer to Electrical Characteristics table for pin spec. This pin is kept high-z while in the Suspend position.
100	USB_VM	I/O	Universal-Serial-Bus Negative data line. Refer to Electrical Characteristics table for pin spec. This pin is kept high-z while in the Suspend position.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{dd} - GND	-0.5 to 4.0	V
Voltage, any pin to GND	V	-0.5 to V_{dd}+0.5*	V
DC Current Drain per Pin (Excluding V_{dd}, GND)	I	±14	mA
Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

* 5.5V for 5-volt Tolerant inputs, and 6.0V for 5-volt Tolerant Open-Drain outputs

ELECTRICAL CHARACTERISTICS (V_{dd}=3.3V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Supply Voltage (V_{dd} to GND)	V_{dd}	3.0	3.3	3.6	V
DC Supply Current (@ V_{dd}=3.3V)	I_{CC}	-	58	73	mA
Suspend mode Current (@ V_{dd}=3.3V)	$I^{Suspend}$	-	-	200	µA
High Level Input Voltage (other than XIN, CAPTRN, and RESIN)	V_{IH}	2.0	-	V_{dd}+0.3*	V
Low Level Input Voltage (other than XIN, CAPTRN, and RESIN)	V_{IL}	-0.3	-	0.8	V
High Level Input Voltage (XIN, CAPTRN, and RESIN)	$V_{IH-s.t}$	0.8 V_{dd}	-	V_{dd}+0.3	V
Low Level Input Voltage (XIN, CAPTRN, and RESIN)	$V_{IL-s.t}$	-0.5	-	0.2V_{dd}	V
Input Current $V_I = V_{dd}$+0.3 or GND	I_{in}	-5	+1	+5	µA
Input Capacitance	C_{in}	-	5	16	pF
3-State Output Leakage Current $V_O = V_{dd}$+0.3 or GND	I_{OZ}	-10	+1	+10	µA
Output Capacitance	C_{out}	-	5	16	pF
High Level Output Voltage (@ Iout = -2mA)	V_{OH}	V_{dd}-0.5	-	V_{dd}	V
Low Level Output Voltage (@ Iout = 2mA)	V_{OL}	0	-	0.4	V
Output Short Circuit Current	I_{OS}	-	-	±30	mA
Pull-Up / Pull-Down Resistance	R_{PU}	25	50	200	KΩ

* Vdd+0.3 is for regular inputs. 5-volt Tolerant inputs allow maximum input voltage of 5.25 volt.

USB_VP/VM pins ELECTRICAL CHARACTERISTICS (V_{dd}=3.3V, T_A = 0 to 70° C)

Characteristic	Symbol	Min	Typ	Max	Unit
Hi-Z State Data Line Leakage (@ 0<Vin<3.3v)	I_{LO}	-10	-	+10	µA
Differential Input Sensitivity	V_{DI}	0.2	-	-	V
Differential Common Mode Range	V_{CM}	0.8	-	2.5	V
Single Ended Receiver Threshold	V_{SE}	0.8	-	2.0	V
Static Output Low (@ 1.5KΩ pull-up resistor to 3.6v)	V_{OL}	-	-	0.3	V
Static Output High (@ 15KΩ pull-down resistor to GND)	V_{OH}	2.8	-	3.6	V
Capacitance	C_{IN}	-	-	20	pF
Rise Time (@ C_L =50 pF)	T_R	4	-	20	nS
Fall Time (@ C_L =50 pF)	T_F	4	-	20	nS

Driver Output Resistance (@ external serial 24Ω resistor)	Z_{DRV}	28	-	43	Ω

VIDEO PARAMETERS SPECIFICATION

Parameter	Symbol	Value	Unit
Digital Video Input Format (1)	Y/U/V	-	-
Down Scaling (V/H independent and arbitrary)	-	up to 16:1 vertical and horizontal	-
Horizontal Anti Aliasing Filter (2)	-	2-5 taps	-
Vertical Anti Aliasing Filter (2)	-	2-3 taps	-
Interpolation Phase Resolution	-	360°/4	-
Image Cropping (V/H independent and arbitrary)	-	any window of length 1 to full image	-
Video Compression Ratio	Cr	1-8	-
Video Compressor Clock Frequency	-	48.000	MHz
Compressed Video Bit Rate	-	0.5 to 7.5 Mbit/sec	-

Notes:

1. Refer to *Video Channel* chapter for specification of digital video input modes and waveforms.
2. Filter uses interpolation process.

USB INTERFACE PARAMETERS SPECIFICATION

Parameter	Value	Unit	USB Pipe mode
USB Maximum Data Rate	12	Mbit/sec	-
Compressed Video Maximum Data Rate	7.5	Mbit/sec	Isochronous
I/O channel Rate Capacity(1)	0-16	Kbit/sec	Control & Bulk

Notes:

1. I/O channel uses transactions of up to 8-bytes per package.

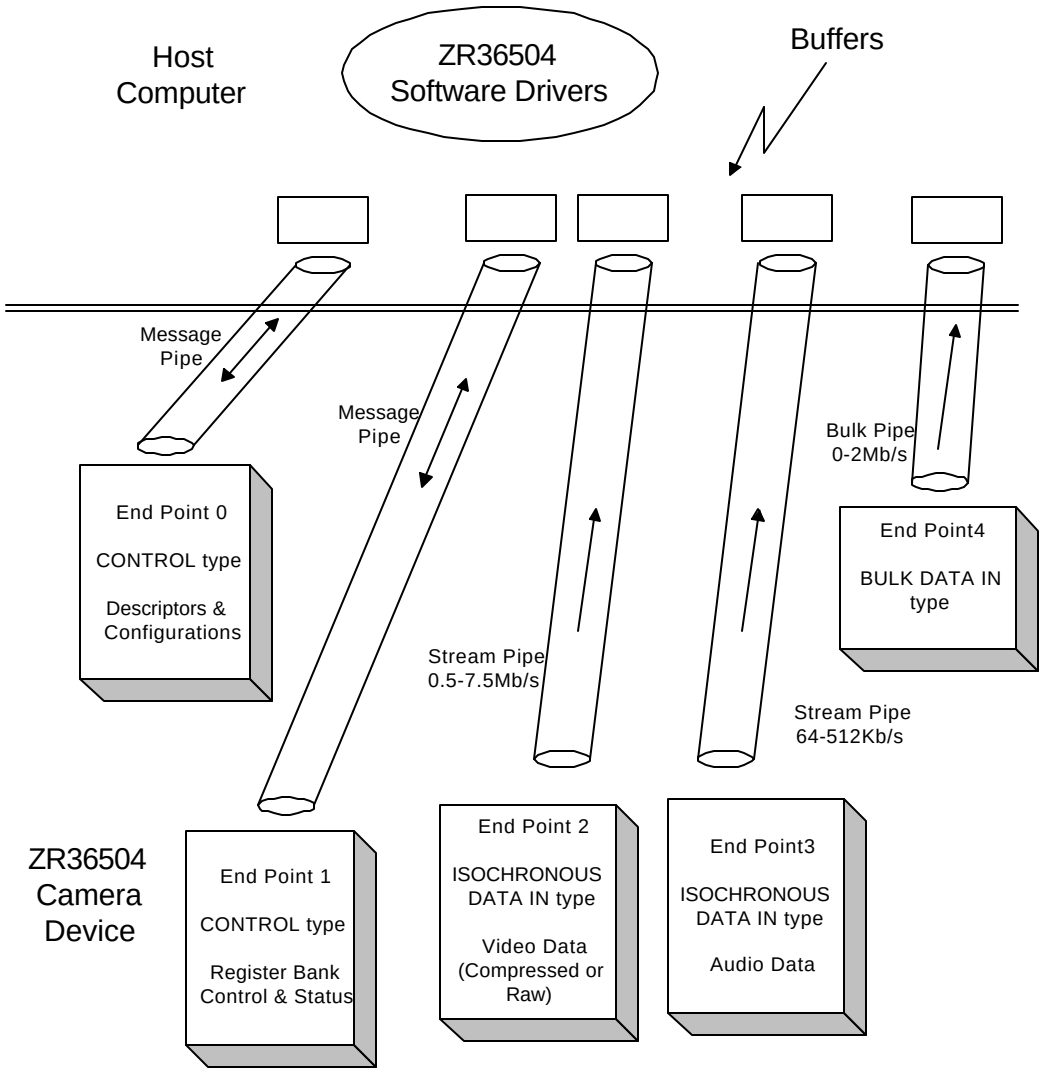
AUDIO PARAMETERS SPECIFICATION

Parameter	Symbol	Value	Unit
Digital Audio Sampling Rate	Fs	8.0/16.0 ± 0.25%	KHz
Audio channel Bit Rate	-	64-512 Kb/sec μ-Law or A-Law	-
Audio CODEC clock frequency		1.536, 2.048 (1)	MHz

Note:
1. Programmable to either 1.536 or 2.048 MHz.

1. General Architecture

The following diagram describes the general architecture of the ZR36504, regarding it as a standard USB device:



The ZR36504 has 5 USB End-Points located on chip:

* End-Point #0: This is the Descriptors and Configuration End-Point, which is mandatory by the USB standard.

* End-Point #1: This is the ZR36504 Register Bank; the host computer uses these registers to control the ZR36504 and Camera.

* End-Point #2: This End-Point produces and sends the digital Video Data to the host computer. It uses 0.5 to 7.5Mb/s of the USB bandwidth, depending on how much bandwidth is available for the camera.

* End-Point #3: This End-Point sends the input digital Audio Data to the host computer. It uses 64 to 512Kb/s of the USB bandwidth, depending on the audio quantization and sampling rate.

* End-Point #4: This End-Point sends the external Bulk Data input to the host computer. It uses 0 to 2Mb/s of the USB bandwidth, depending on the external source of data.

The ZR36504 has a default set of USB Descriptors on-chip, which are automatically used in absence of an external serial EEPROM (otherwise, all descriptors are read from the EEPROM). The default descriptors allow the host computer to select one of 4 different configurations to operate the camera. Most camera vendors can now use the ZR36504 without an external EEPROM. Also Vendor USB ID and Product ID are now pin-programmable, and do not require to add an extra EEPROM.

Camera vendors need not use an external EEPROM for a low-cost solution. The ZR36504 and a 4Mb DRAM are sufficient for a fully USB standard compatible camera (this includes the specific given Vendor ID, which identifies the camera with the specific manufacturer).
If an external 8-pin serial EEPROM is added, the camera manufacturer can define new configurations (which combine only the available End-Points). Also, String-Descriptors can be added (in multiple languages) to define the camera vendor's name, product name, serial-number, and others; the USB standard regards these features as optional.

The ZR36504 supports USB Power-Management-Protocol. The Camera and external circuits can be power-controlled by their vendor-specific software drivers, via serial Data/Clock, and I/O ports; also, the PWR_DWN output pin can be used to turn off the local power supply to these external circuits (refer to ZR36504 application notes). The ZR36504 uses a single 12MHz crystal to derive all its internal clock sources. Power

Management also involves switching of internal clock sources which are not in use in certain modes of operation; this further reduces the power consumption of the device.

The ZR36504 has two sources of Reset control: The Power-On Reset that comes from a dedicated input pin RESIN, and the USB-Reset command received from the host computer. Both reset sources produce a single reset signal inside the ZR36504, which initializes the ZR36504. It is assumed that a power-on-reset should be applied to the RESIN pin before any USB transaction is sent to the ZR36504 by host; this is required so that the Serial-Interface-Engine inside the ZR36504 will be able to receive any valid host command that will follow (including a USB-Reset command).

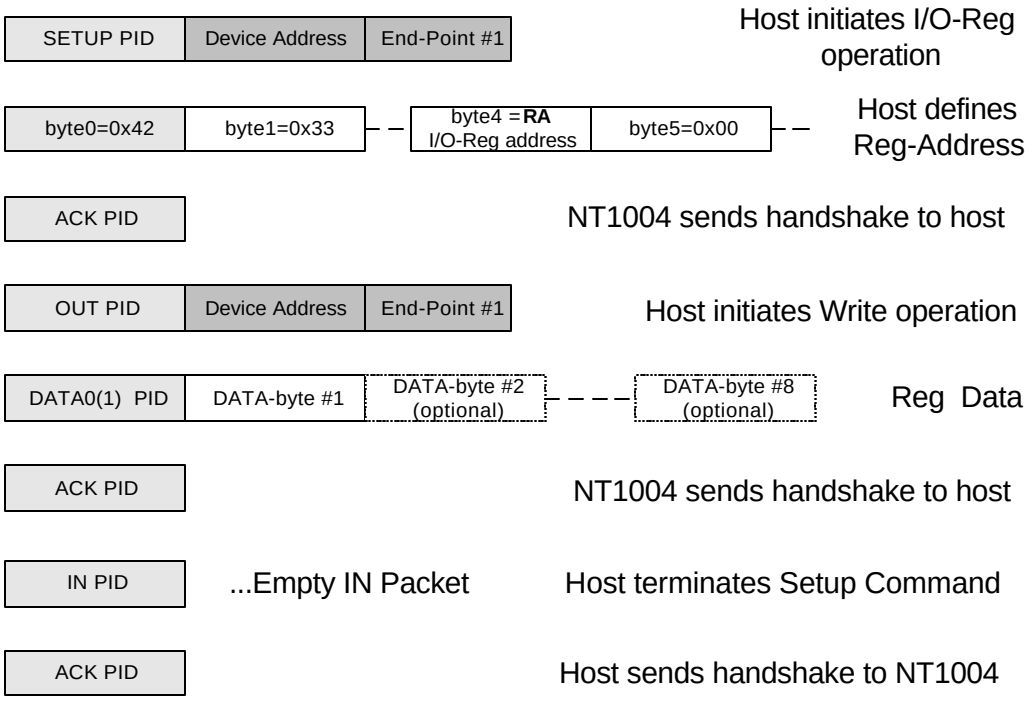
The total USB bandwidth that is occupied by the ZR36504 is mainly affected by the bandwidth of the Video Data Stream (End-Point #2). In order for a host computer, which initially has a small available bandwidth, not to reject the camera device, the ZR36504 uses the Alternate-Interface mechanism to enable variable bandwidth. This allows the host computer to select the highest bit-rate that it can reserve for the Video Stream, starting from 7.5Mb/s down to 0.5Mb/s in 0.5MHz down steps (the selected bit-rate affects the video quality).

2. Registers Bank (Control and Status)

The ZR36504 uses the End-Point #1 message pipe for ZR36504 and camera control. As a bi-directional pipe, this channel allows the host computer to write contents to control registers, as well as to read status registers. Also, the control registers can be read by host computer to check their contents. All registers are byte-oriented.

The following section defines a USB vendor-specific protocol for Read and Write operations applied to the ZR36504 register bank. This protocol uses a standard USB Request of a vendor-specific type (defined in chapter 9.3 of USB standard rev.1.0) to perform a data transfer of up to 8 bytes long to/from End-Point #1. A single Write operation will write 1-8 concurrent bytes to the register bank, and a single Read operation will read 1-8 concurrent bytes from the register bank. The USB Request Command always defines the address of the first I/O-register to be read or write; this address is automatically incremented by the ZR36504 for the following data bytes. The first byte of the USB Request Command defines the direction of the data transfer (0x42 for Write, and 0xC2 for Read); the second byte is a ZR36504 specific code - 0x33. The address of the first I/O-register in list is defined in the **wIndex** parameter of the standard USB Request Command (these are bytes 4 & 5 of the command). All the other bytes in the Request Command are not important to the ZR36504.

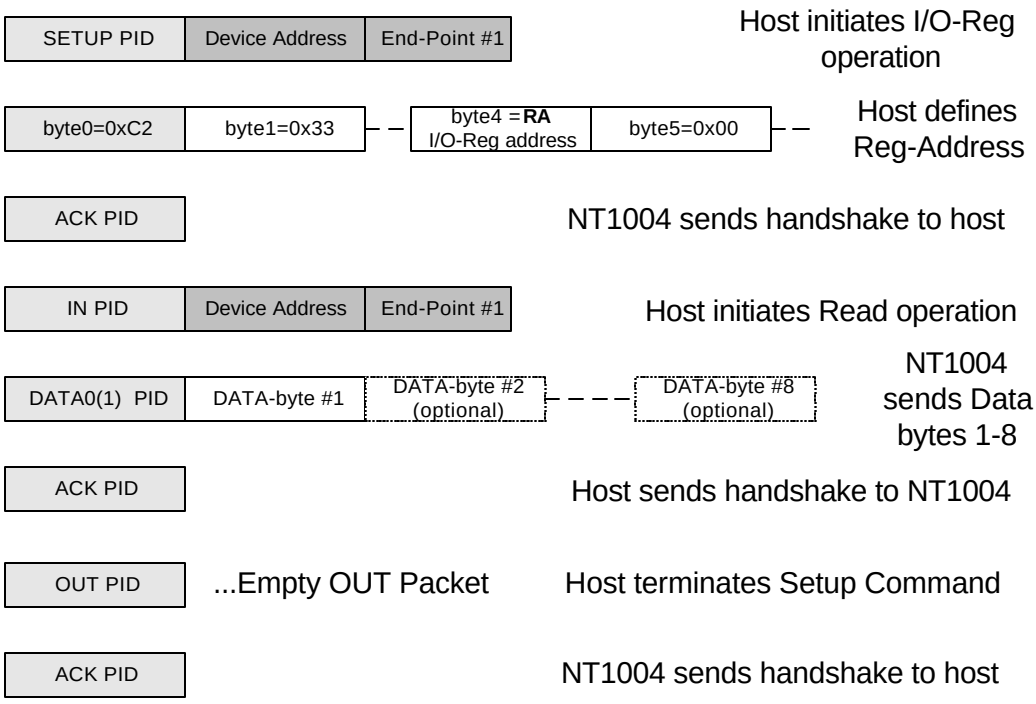
Write transaction protocol:



The following table specifies the addresses where the ZR36504 stores each of the bytes that appear in the data-section of the USB OUT transaction. These addresses relate to the contents of the **wIndex** parameter (bytes 4&5 of the SETUP command), which is denoted here by **RA**.

DATA byte #	Contents	Description
1	Out Data	Will be stored in register at address RA.
2	Out Data	Optional. Will be stored in register at address RA+1.
3	Out Data	Optional. Will be stored in register at address RA+2.
4	Out Data	Optional. Will be stored in register at address RA+3.
5	Out Data	Optional. Will be stored in register at address RA+4.
6	Out Data	Optional. Will be stored in register at address RA+5.
7	Out Data	Optional. Will be stored in register at address RA+6.
8	Out Data	Optional. Will be stored in register at address RA+7.

Read transaction protocol:



DATA byte #	Contents	Description
1	Register Data	Byte read from register at address RA.
2	Register Data	Optional. Byte read from register at address RA+1.
3	Register Data	Optional. Byte read from register at address RA+2.
4	Register Data	Optional. Byte read from register at address RA+3.
5	Register Data	Optional. Byte read from register at address RA+4.
6	Register Data	Optional. Byte read from register at address RA+5.
7	Register Data	Optional. Byte read from register at address RA+6.
8	Register Data	Optional. Byte read from register at address RA+7.

Note: Reading from an address that does not exist is legal, but will return unpredicted data.

The tables in the following pages specify all the Control and Status registers in the ZR36504. A brief description is given for every specific bit in these registers, and the default values (after Reset operation) are defined. For more details about a specific register, consult the appropriate session in this data sheet.

General Control Registers (Power, Restart EP, USB, IO-pins, Camera Control):

Reg. Address	Reg. Name	Function	Default Value
0	PWR_REG	d0: WD_EN: '1' Enables USB Watch-Dog timer d1: SSPND_EN: '0' Enables Suspend-Resume logic d2: RES2: '0' Restarts End-Point #2 logic, '1' Releases d3: CLK48_EN: '1' Enables 48MHz at CLK48 output pin. d4: reserved d5: PWR_VID: '1' Video-logic Power-On d6: reserved d7: E2_EN: '1' Enables EEPROM R/W	00H
1	CONFIG_REG	d7-d0: Configuration (set via USB). Read-Only reg.	00H
2	ADRS_REG	d6-d0: Device Address (set via USB). Read-Only reg. d7: '0'. reserved.	00H
3	ALTER_REG	d3-d0: Video Bandwidth (set via USB). Read-Only reg. d7-d4: '0000'. reserved.	00H
4	FORCE_ ALTER_REG	d3-d0: NEW_ALT Forced Video Bandwidth. R/W reg. d7: FORCE_ALT ('1'=force, '0'=ignore) d6-d4: '000'. reserved.	00H
5	STATUS_REG	d0: VFRM_BLNK Vertic. Blank (if '1'). Read-Only reg. d7-d1: '0000000'. reserved.	00H
6	IOPIN_REG	d0: IO_1 Read/Write level of ZR36504 pin IO-1 d1: IO_2 Read/Write level of ZR36504 pin IO-2 d7-d4: TEST[3..0], must be '0000' for proper operation. d3-d2: '00'. reserved	00H
7	SER_MODE	d7-d4: MODE (Soft, IICC, Cam1,Cam2,,,) **normally (when not in Soft mode):** d0: CLK_RATE ('0' = 93.75KHz, '1' =1.5MHz) d1: CLK_POL ('0' = Normal, '1' = Inverted) d2: TEST(auto bulk). Must be '0' for proper operation. d3: VSYNC ('1' = wait to new input video field) **Soft mode:** d0: CLK_OUT (functional in Soft mode only) d1: DAT_IO (functional in Soft mode only) d2: SENS_OUT (functional in Soft mode only)	00H
8	SER_ADRS	d7-d0: Address of serial device/camera-param.	00H
9	SER_CONT	d2-d0: SER_LEN Number of bytes to Wr/Rd d3: SER_DIR ('0' = Wr, '1' = Rd) d4: SER_GO/SER_BUSY d5: NACK_RCV (Read-Only. '1' means Not Ack.) d6: CONTINUE (Do not send START signal next time) d7: NO_STOP (Do not send STOP signal this time)	00H
10	SER_DAT1	d7-d0: 1st serial byte to be sent/received	00H
11	SER_DAT2	d7-d0: 2nd serial byte to be sent/received	00H
12	SER_DAT3	d7-d0: 3rd serial byte to be sent/received	00H
13	SER_DAT4	d7-d0: 4th serial byte to be sent/received	00H

EEPROM Read/Write Registers:

Reg. Address	Reg. Name	Function	Default Value
14	EE_DATA	d7-d0: EEPROM byte to be Written/Read	00H
15	EE_LSBAD	d7-d0: 8-LSbits of byte address in EEPROM	00H
16	EE_CONT	d2-d0: 3-MSbits of byte address in EEPROM d3: EE_DIR ('0' = Write, '1' = Read) d4: EE_GO/EE_BUSY d7-d5: EE_CLK_FORCE (This field is Read-Only)	00H or xxx0000 (when no EPROM)

DRAM and Memory Buffers Setup Registers:

Reg. Address	Reg. Name	Function	Default Value
18	DRM_CONT	d0: REF ('0' = 8.2ms, '1' = 128ms refresh rate) d1: DRAM_SIZE. '0' selects 4M, '1' selects 16M d2: RES_UR Restart video out buff. read logic d3: RES_FDL Restart video-frame-delay logic d4: RES_VDW Restart vid.out buff. write logic d5: Bit 9 of UR_1ST_ROW parameter (16M only) also Bit 9 of VDW_1ST_ROW parameter (16M only) d6: Bit 9 of UR_LST_ROW parameter (16M only) also Bit 9 of VDW_LST_ROW parameter (16M only) d7: DRM_COL_SLCT for UR/VDW_LST_ROW	00H
19	DRM_PRM1	d0: Bit 8 of UR_1ST_ROW parameter d1: Bit 8 of UR_LST_ROW parameter d2: Bit 8 of FDL_1ST_ROW parameter d4-d3: Bits 17-16 of FDL_LST_WORD param. d5: Bit 8 of VDW_1ST_ROW parameter d6: Bit 8 of VDW_LST_ROW parameter d7: Bit 18 of FDL_LST_WORD param (16M only).	00H
20	DRM_PRM2	d7-d0: Bits 7-0 of UR_1ST_ROW parameter	00H
21	DRM_PRM3	d7-d0: Bits 7-0 of UR_LST_ROW parameter	00H
22	DRM_PRM4	d7-d0: Bits 7-0 of FDL_1ST_ROW parameter	00H
23	DRM_PRM5	d7-d0: Bits 7-0 of FDL_LST_WORD param.	00H
24	DRM_PRM6	d7-d0: Bits 15-8 of FDL_LST_WORD param.	00H
25	DRM_PRM7	d7-d0: Bits 7-0 of VDW_1ST_ROW parameter	00H
26	DRM_PRM8	d7-d0: Bits 7-0 of VDW_LST_ROW parameter	00H

Video Setup and Control Registers:

Reg. Address	Reg. Name	Function	Default Value
27	VIN_REG1	d2-d0: VIN_MODE Digital video input format d3: VSNC_POL Vertical-Sync. pulse polarity d4: HSNC_POL Horizontal-Sync. pulse polarity d5: FID_POL Field Identity signal polarity d6: HVALID_POL Pixel Envelope polarity d7: VCLK_POL ('1'=data valid on up-going clock)	00H
28	VIN_REG2	d0: AUTO_FID Auto Field Identity generation. When set to '1', the ZR36504 ignores the FID input from camera, and generates an internal toggling signal of its own instead.	00H

		d1: NONE_INTERLACE Interlace/Non-Interlace mode. If set to '1', all the input fields from camera are processed, otherwise the odd fields are ignored. d2: NO_HVALID If set to '1', HVALID input ignored. d3: UV_ID If set to '1', use V7 pin as UV-id ('1'=U). d4: FIX_2C If set to '1', U7 & V7 are inverted (2's comp). d5: SEND_FID If set to '1', Frame_Phase[0]=FID. d6: '0' reserved. d7: KEEP_BLANK Set to '1' to drop incoming frames.	

Video Setup and Control Registers (Continued):

Reg. Address	Reg. Name	Function	Default Value
29	LXSIZE_IN	d7-d0: bits 7-0 of input video line length	00H
30	MXSIZE_IN	d1-d0: bits 9-8 of input video line length d7-d2: '000000' reserved.	00H
31	LYSIZE_IN	d7-d0: bits 7-0 of input video number of lines	00H
32	MYSIZE_IN	d1-d0: bits 9-8 of input video number of lines d7-d2: '000000' reserved.	00H
33	LX_OFFST	d7-d0: bits 7-0 of input video horizontal offset	00H
34	MX_OFFST	d1-d0: bits 9-8 of input video horizontal offset d7-d2: '000000' reserved.	00H
35	LY_OFFST	d7-d0: bits 7-0 of input video vertical offset	00H
36	MY_OFFST	d1-d0: bits 9-8 of input video vertical offset d7-d2: '000000' reserved.	00H
37	FRM_RATE	d4-d0: Frame-Rate factor Numerator for video data output d6-d5: Frame-Rate factor Denumerator code: '00': 32, '01': 30, '10': 25 d7: '0' reserved.	00H
38 39	LXSIZE_O MXSIZE_O	d7-d0: bits 7-0 of output video line length d1-d0: bits 9-8 of output video line length d7-d2: '000000' reserved.	00H 00H
40	LYSIZE_O	d7-d0: bits 7-0 of output video number of lines	00H
41	MYSIZE_O	d1-d0: bits 9-8 of output video number of lines d7-d2: '000000' reserved.	00H
42	FILT_CONT	d2-d0: XFILT_CONT Horizontal-Filter select d4-d3: YFILT_CONT Vertical-Filter select d7-d5: '000' reserved.	00H
43	VO_MODE	d5-d0 Digital Video-Out format (4:2:2, 4:2:0, compress.) d6: ('1' = Compressed Vid, '0' = Raw) d7: '0' reserved.	00H
44	INTRA_CYC	d7-d0: Intra-Compression cycle (in frame units)	00H
45	STRIP_SZ	d3-d0: ACT_STRIP Actual Strip width (# of vid.lines) d7-d4: VIRT_STRIP Virtual Strip width (# of vid.lines)	00H
46	FORCE_INTRA	d0: ('1' = Force next frame Intra) d7-d4: MIN_DENUM[3..0] d3-d1: '000' reserved.	00H
47	FORCE_UP	d0: ('1' = Force Up-mode Intra segments) d7-d1: STRIP_DAT_LIMIT[6..0].	00H
48	BUF_THR	d7-d0: Threshold for buffer space Frame-Drop decision (given in units of 2KB).	00H
49	DVI_YUV	d2-d0: Code for YUV re-order processor. d4-d3: BUF_THR[9..8]. Extension for 16Mbit DRAM	00H

		d6: SLOW_CLK12 '1' Select 12MHz for Horiz. blank d7: SLOW_CLK16 '1' Select 16MHz for Horiz. blank d5: '0' reserved.	

Audio & Bulk-Data Port Read/Write Registers:

Reg. Address	Reg. Name	Function	Default Value
50	AUDIO_CONT	d0: E_A - Enable Audio channel ('1' enables, '0' disables) d1: E_B - Enable Bulk-Data port ('1' enables, '0' disables) d3-d2: BPS - bits/samp: 00: 8b, 01: 12b, 10: 14b, 11: 16b d4: S/M - Select Stereo/Mono. '0': Mono, '1': Stereo. d5: FS - Audio Samp.Rate: '0': 8Ks/sec, '1': 16Ks/sec. d7-d6: BK - Bit-Clk Freq: 1: 64, 2: 1544, 3: 2048 [KHz]	00H
51	AUD_PK_LEN	d7-d0: Max. number of bytes in Audio packet (0 to 128).	00H
52	BLK_PK_LEN	d6-d0: Max. number of bytes in Bulk packet (0 to 64). d7: '0' reserved.	00H

USB Watch-Dog Register:

Reg. Address	Reg. Name	Function	Default Value
53	WD_COUNT	d7-d0: USB_frame Watch-Dog delay parameter. A value 0x00 produces a 686 micro-seconds delay. A value of 0xE9 produces a 996 micro-seconds delay. Any value between these two values affects the delay in steps of 1.33 micro-seconds. Values bigger than 0xE9 have no effect.	00H

Compression Ratio Management Registers (Continued):

Reg. Address	Reg. Name	Function	Default Value
56	PCM_THR1	d7-d0: PCM Threshold 1 (unsigned 0-255)	00H
57	PCM_THR2	d7-d0: PCM Threshold 2 (unsigned 0-255)	00H
58	DIST_THR_I	d7-d0: DIST_THR_I (Distortion. Threshold for Inter)	00H
59	DIST_THR_A	d7-d0: DIST_THR_I (Distortion. Threshold for Intra)	00H
60	MAX_DIST_I	d7-d0: MAX_DIST (Maximum Distortion for Inter)	00H
61	MAX_DIST_A	d7-d0: MAX_DIST (Maximum Distortion for Intra)	00H
62	VID_BUF_ LEFT	d7-d0: Space left in ZR36504 DRAM buffer for compressed video data (given in units of 2KB). **Read-Only Register.**	00H
63	LFP_LSB	d7-d0: bits 10-3 of LAST_FRM_PNTR (DRAM pointer). **Read-Only Register.**	00H
64	LFP_MSB	d6-d0: bits 17-11 of LAST_FRM_PNTR (DRAM pointer) d7: RAM_FULL ('1' if event occurred from last Read). **Read-Only Register.**	00H
65	VID/LPF	d1-d0: VID_BUF_LEFT[9..8]. Ext. for 16Mbit DRAM. d3-d2: LPF[19..18]. Extension for 16Mbit DRAM. d7-d4: '0000' reserved. **Read-Only Register.**	00H

3. Power Management

In order to meet the USB standard, the ZR36504 should be able to control USB power supply for the whole device. Two pins of the ZR36504 were dedicated to this task: PWR_DWN and SUSPND. Both pins are Open-Drain, and active when Hi-Z.

The USB standard requires that soon after a device is hot-connected to the computer, it should consume no more than 100mA from USB port; After configuration, the device may consume up to 500mA from the port. Also it is required that in the Suspend mode the device must not consume more than 0.5mA from the USB port.

The ZR36504 uses its power management pins as follows:

⇒ The PWR_DWN pin was designed to switch the USB 5v source to the video/audio source circuit (CCD, DSP, ADC, µ-Controller, Video-Decoder, audio CODEC, etc.). The only ICs that continue to get normal power supply in the Power-Down state are the ZR36504, DRAM, and EEPROM (all these are 3.3v operated).

⇒ The SUSPND pin was designed to enable the designer to shut-down any additional element in the ZR36504 application circuit, which may increase the total current consumption to more than the USB standard allows (> 0.5mA).

Refer to the ZR36504 Application Notes for an example of how the PWR_DWN and SUSPND pins should be used, and for the 3.3v supply in application design.

The ZR36504 software driver can control part of the power-management process through the following registers of the ZR36504:

Parameter	Register address	Usage
SSPND_EN	Reg.0/d1 SSPND_EN	Enable Suspend state: 0: Default (after Reset). Responds to USB Suspend condition as required by USB standard. 1: Suspend state is disabled
PWR_VID	Reg.0/d5 PWR_VID	Apply USB 5v to Video/Audio Source 0: Default (after Reset). Video/Audio Source is OFF 1: Video/Audio Source is powered ON
RES2	Reg.0/d2 RES2	Restart End-Point #2 (Vid. pipe) in the ZR36504: 0: Default (after Reset). Restart ZR36504 video path. 1: Enable ZR36504 Video Processor and Pipe circuit (after video source is powered on).

After USB-Reset, the ZR36504 is in its Power Down state (PWR_DWN pin is Hi-Z). After configuration, software sets PWR_VID bit to '1' to turn on camera circuit

(PWR_DWN='0'). Suspend (if SSPND_EN bit not set by S/W), occurs if USB Idle state detected for 3ms, and it also resets PWR_VID bit.

4. Video Input Interface

The ZR36504 digital video input is YUV format. The ZR36504 interface for this format is flexible and supports 4:4:4 (24-bit) as well as 4:2:2 (8-bit, or 16-bit), and 4:1:1 timings (12-bit). Horizontal and Vertical controls can be physical pulses or coded signals; Also, Pixel Clock and pulse polarity of control signals can be programmed to be either positive or negative.

All the input buffers in the ZR36504 that are supposed to be connected to the digital video source are 5-volt tolerant. This means that a camera that has 5-volt CMOS outputs will not cause any damage to the ZR36504, even though the ZR36504 operating voltage is 3.3 volts.

The ZR36504 digital video input consists of the following signals:

Y0-Y7
In the 4:4:4 format (24-bit), 4:2:2 16-bit, and 4:1:1 (12-bit) modes, this is the Luminance input bus. In the 4:2:2 8-bit mode, this bus is used for mux YUV data. This bus is sampled by the VCLK input clock for the unsigned binary value (0-255) of the Y component (or U and V as well in the 8-bit mode).

U0-U7
This is the Color (U or U/V) input bus. In the 4:4:4 format (24-bit), This bus is sampled by the VCLK input clock for the unsigned binary value (0-255) of the U component. In the 4:2:2 16-bit and 4:1:1 (12-bit) formats, this bus is sampled by the even cycles of VCLK input clock for the binary value (0-255) of the U component, and by the odd cycles of VCLK input clock for the binary value (0-255) of the V component.

V0-V7
This is the Color (V) input bus, which is used in the 4:4:4 format only. This bus is sampled by the VCLK input cbck for the binary value (0-255) of the V component. In the 4:2:2 mode (16-bit or 8-bit) and the 4:1:1 mode (12-bit), most of this bus is ignored by the ZR36504 - only V7 is used as an optional U/V identifier.

VSNC
This is the Vertical Synchronization pulse, which indicates the start of a new video field (in Interlace mode) or the start of a new video frame (in Non-Interlace mode). Normally this pulse is negative.

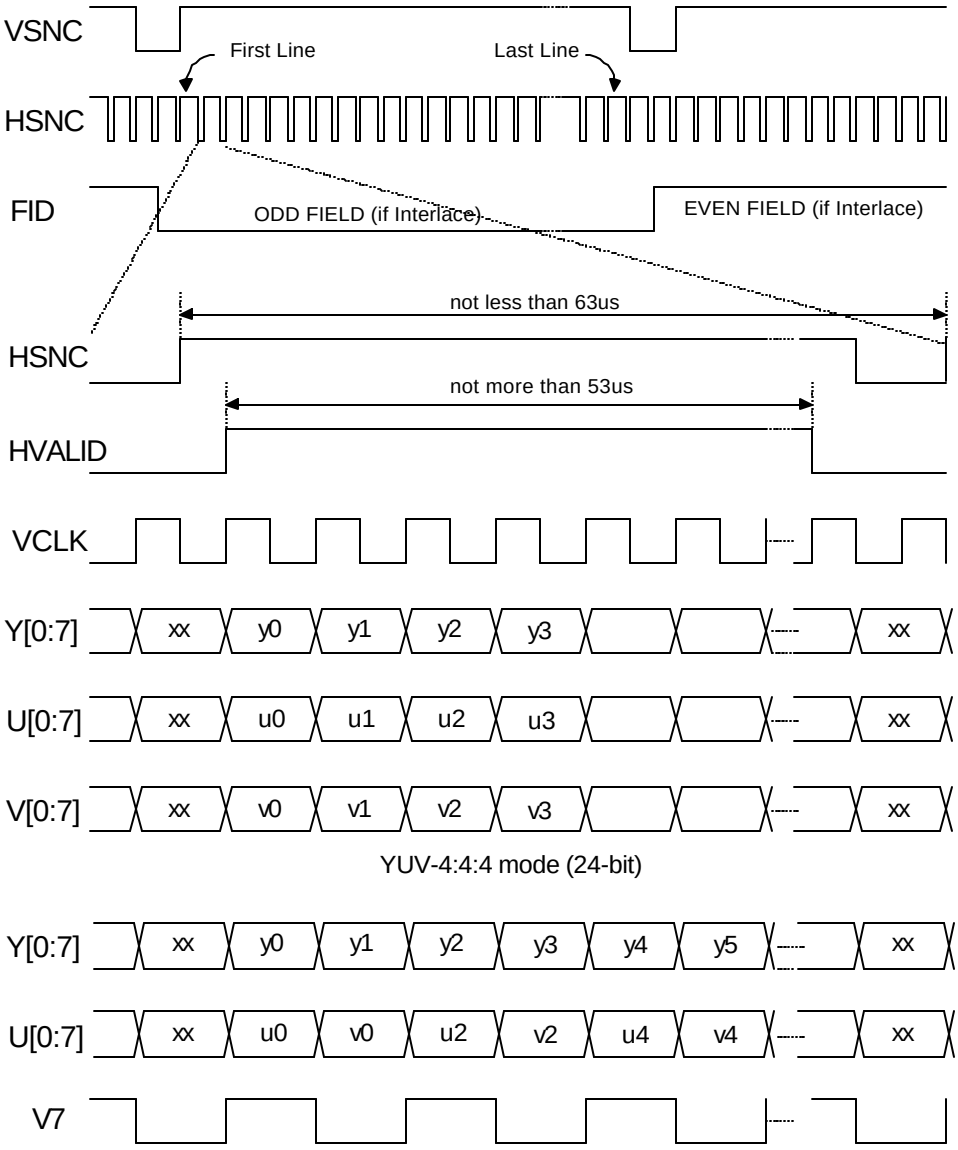
HSNC
This is the Horizontal Synchronization pulse, which indicates the start of a new video line. Normally this pulse is negative.

FID
This signal is used in the Interlace mode, to indicates whether the current field is even or odd. In the Non-Interlace mode this input is ignored by the ZR36504.

VCLK
This signal is the video pixel clock. It is used by the ZR36504 to sample all the other inputs in the digital video interface.

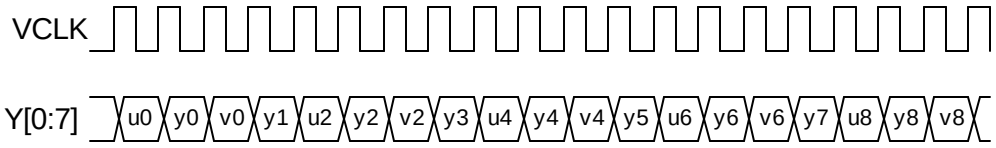
HVALID
This input is the pixel valid qualifier. When not active, the ZR36504 refers to the samples that come from the Y, U, and V buses as Blank pixels (which are not considered a part of the digital image). The ZR36504 can be programmed to ignore the HVALID input.

The timing of a camera signal that the ZR36504 expects to receive in its digital video interface is normally as specified in the following timing diagram:



YUV-4:4:4 mode (24-bit)

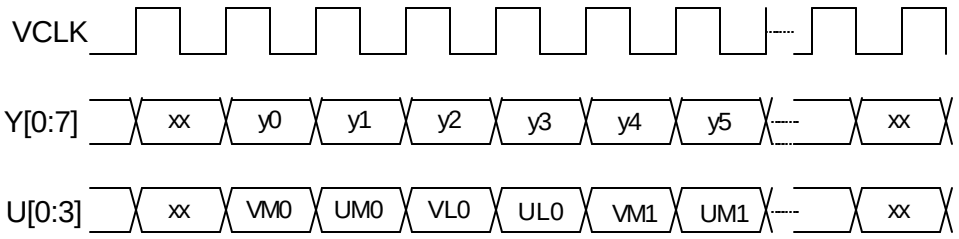
YUV-4:2:2 mode - 16-bit. Note that the order of U/V is set by Reg.49/d0.



YUV-4:2:2 mode 8-bit. Note that the order of Y/U/V is set by Reg.49/d2-d0

Note:

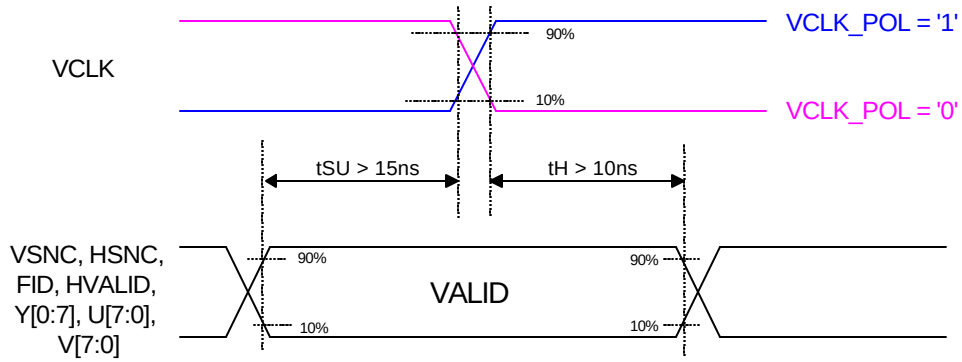
In the YUV 8-bit mode the VCLK frequency is twice the pixel rate.



VM0 = v0[7..4], VL0 = v0[3..0] UM0 = u0[7..4], UL0 = u0[3..0]

YUV-4:1:1 mode (12-bit)

Video Interface Timing Parameters



Input Video Parameters

The ZR36504 was designed to interface to most available YUV formats. To make this possible, most of video parameters are programmable via specific registers from the ZR36504 Register Bank.

The following tables specifies all the parameters that can be set by host computer to fit a specific video source (digital camera, video decoder, etc.):

Parameter	Register address	Usage
VIN_MODE[2..0]	Reg.27/d2-d0 VIN_REG1	Video input mode: 000: 8-bit 4:2:2 mode, using synchronization pulses 001: 8-bit 4:2:2 mode, using CCIR 656 sync. codes 010: 16-bit 4:2:2 mode, using synchronization pulses 011: 16-bit 4:2:2 mode, using CCIR 656 sync. codes 100: 24-bit 4:4:4 mode, using synchronization pulses 110: 12-bit 4:1:1 mode, using synchronization pulses 101, 111: spare.
VSNC_POL	Reg.27/d3 VIN_REG1	Polarity of VSNC pulse: 0: Synchronize on up-going edge 1: Synchronize on down-going edge
HSNC_POL	Reg.27/d4 VIN_REG1	Polarity of HSNC pulse: 0: Synchronize on up-going edge 1: Synchronize on down-going edge
FID_POL	Reg.27/d5 VIN_REG1	Polarity of FID (Field Identifier in Interlace mode) : 0: FID='0' during first (odd) field 1: FID='0' during second (even) field
HVALID_POL	Reg.27/d6 VIN_REG1	Polarity of HVALID signal: 0: input signal HVALID='1' for active pixels 1: input signal HVALID='0' for active pixels
VCLK_POL	Reg.27/d7 VIN_REG1	Polarity of VCLK (pixel clock): 0: Camera data valid at VCLK falling edge 1: Camera data valid at VCLK rising edge
AUTO_FID	Reg.28/d0 VIN_REG2	0: Use external FID signal 1: Generate internal toggling FID. Ignore FID pin.
NON_INTERLACE	Reg.28/d1 VIN_REG2	0: Interlace mode. Only even fields are transferred. 1: Non-interlace mode. All frames are transferred.
NO_HVALID	Reg.28/d2 VIN_REG2	0: Normal operation 1: Ignore the HVALID input (assume constant '1')
UV_ID	Reg.28/d3 VIN_REG2	0: Normal operation 1: Use V7 input as a U/V identifier ('1'=U, '0'=V)
FIX_2C	Reg.28/d4 VIN_REG2	Fix 2's Compliment U/V values 0: Normal operation 1: Invert U[7] and V[7] to fix to Unsigned Binary
XSIZE_IN[9..0]	Regs.29-30 LXSIZE_IN MXSIZE_IN	Number of pixels in active line of video source

(continued...)

Parameter	Register address	Usage
YSIZE_IN[9..0]	Regs.31-32 LYSIZE_IN MYSIZE_IN	Number of active lines in frame (/field) of video source
X_OFFST[9..0]	Regs.33-34 LX_OFFST MX_OFFST	Horizontal offset (number of pixels to be skipped after start of line).
Y_OFFST[9..0]	Regs.35-36 LY_OFFST MY_OFFST	Vertical offset (number of lines to be skipped after start of frame).
DVI_YUV[2..0]	Reg.49/d2-d0 DVI_YUV	Order of Ya/U/V/Yb components of a pixel-pair in 8-bit modes (d0 affects 16-bit mode also): d0: '0': U comes before V '1': U comes after V d1: '0': Ya comes before U/V '1': Ya comes after U/V d2: '0': Yb comes before U/V '1': Yb comes after U/V
SLOW_CLK12 SLOW_CLK16	Reg.49/d7-d6 DVI_YUV	Use these control bits for cameras that have slow VCLK or too short Horiz.Blank time interval: d6: '0': Normal operation '1': Select 12MHz clock during Horiz.Blank d7: '0': Normal operation '1': Select 16MHz clock during Horiz.Blank

Frame-Rate Control

Normally a camera or any other video source provides a fixed number of frames per second - for example, a NTSC based camera will always provide 30 frames/sec.
The ZR36504 allows the application software to modify the effective frame rate to fit its needs; in this way some of the frames coming from camera are dropped before processing, which eliminates the effort that could be wasted on those frames that would be dropped by the computer anyway.

The parameter that controls the effective frame-rate is called FRM_RATE, and is specified in the following table:

Parameter	Register address	Usage
Numerator[4..0]	Reg.37/d4-d0 **n**	Frame Drop factor (**n** = 0-31). Effective frame rate is: NTSC: 30*(**n**+1)/**d** PAL: 25*(**n**+1)/**d**
Denum.code[1..0]	Reg.37/d6-d5 code for **d**	'00': **d**=32 '01': **d**=30 '10': **d**=25

The **n** parameter ranges from 0 to **d**-1. The value **n**=**d**-1 indicates to the ZR36504 to transfer to host computer full frame-rate that is delivered from the video source. Any value **n** that is less than **d**-1 results in a frame-dropping from time to time, so that the effective frame rate is only (**n**+1)/**d** of full frame-rate.

Video Scaling

The ZR36504 has two independent down scalers: one for frame width and one for frame height. It is the responsibility of the software application to select such scale factors that result in a reasonable aspect ratio.

In order to set the scaling factor, the host computer should just specify the desired size of the output frame (assuming XSIZE_IN & YSIZE_IN are initially set). Scaling is done automatically by the ZR36504, regarding the output frame size versus the input frame size.

The following table specifies the parameters that are used to set the output frame size:

Parameter	Register address	Usage
XSIZE_O[9..0]	Regs.38-39 LXSIZE_O MXSIZE_O	Number of pixels in line of scaled output video frame
YSIZE_O[9..0]	Regs.40-41 LYSIZE_O MYSIZE_O	Number of lines in scaled output video frame/field

Note that if host computer specifies the same values for input frame size and output frame size, then no scaling occurs (scaling factor is 1:1).

The ZR36504 performs no Up-Scaling(1). This means that XSIZE_O should never be greater than XSIZE_IN, and YSIZE_O should never be greater than YSIZE_IN.

(1) To produce CIF size from 240-line video fields, a special interpolation process is applied by software driver.

Video Filters

The ZR36504 uses internal programmable anti aliasing filters for the scaling process. There are two filters that are used: One for the horizontal scaling, and the other for the vertical scaling. The filters are programmed independently of each other, and independently of the scaling factors.

Both horizontal and vertical filters use a combination of FIR structure and interpolation to eliminate the pixel jitter in the output frame. The interpolation process effectively improves x4 the resolution of the input frame both horizontally and vertically.

The following table specifies the register that is used to set the filter parameters:

Parameter	Register address	Usage
XFILT_CONT[2..0]	Reg.42/d2-d0 FILT_CONT	Select one of 5 possible Horizontal Filters
YFILT_CONT[1..0]	Reg.42/d4-d3 FILT_CONT	Select one of 3 possible Horizontal Filters

The following table specifies the Horizontal filters:

XFILT_CONT[2..0]	FIR filter applied (Horizontally)	Interpolation (Horizontally)
000	FIR = (1.0)	NO
001	FIR = (1.0)	YES
010	FIR = (0.5, 0.5)	YES
011	FIR = (0.25, 0.5, 0.25)	YES
100	FIR = (0.25, 0.25, 0.25, 0.25)	YES

The following table specifies the Vertical filters:

YFILT_CONT[1..0]	FIR filter applied (Vertically)	Interpolation (Vertically)
00	FIR = (1.0)	NO
01	FIR = (1.0)	YES
10	FIR = (0.5, 0.5)	YES

Video Output Format

The ZR36504 supports 3 different formats for the output video data: One is the Compressed data format, and the other two are YUV 4:2:2 and 4:2:0 Raw data formats.

The following table specifies the register that is used to set the output video format:

Parameter	Register address	Usage
VO_MODE[6..0]	Reg.43/d6-d0 VO_MODE	Select one of 3 Video Output formats: 0x60 = Compressed data format 0x03 = YUV 4:2:2 Interleaved format 0x14 = YUV 4:2:0 Planar format

It is the responsibility of the ZR36504 software driver to make conversions to provide the application software with several OS standard video data formats, but the data that is transferred via USB must be one of these 3 formats.

Compressed Data Format

The ZR36504 compressor is designed to compress YUV 4:2:0 frames (12 bit/pixel) in a factor between 1:3 to 1:15 (resulting in 4 to 0.8 bit/pixel). The compression algorithm is a proprietary development of Zoran, which meets 3 important requirements that were made to guarantee the high performance of the ZR36504:

⇒ Fits the selectable bandwidth of the USB (0.5-7.5 Mbit/sec)
⇒ Variable Compression Rate (in very small steps)
⇒ Requires minimum CPU time for Decompression (also, fits MMX® concept)

The ZR36504 compressor compresses specific frames using its Intra mode, and all the others - using its Inter mode. The Intra mode does not require any one of the previous frames, while the Inter mode is always based on the reconstructed previous frame. The Intra frames provide the algorithm some robustness against error propagation between frames, but consume more bits per pixel than the Inter frames. Error propagation within the frame itself (from higher lines to lower lines) is eliminated by dividing the frame into many horizontal strips.

The ZR36504 uses 6 parameters to determine how deep a compression to apply. These parameters are expected to be dynamically modified by the software driver in order to achieve the desired frame rate for a given USB bandwidth.

The following table specifies the registers that are used to control the Intra/Inter relationship, and the number of lines in every strip. The table also contains the special threshold parameters that affect the compression rate. Note that these parameters are only relevant when using the Compressed data format:

Parameter	Register address	Usage
INTRA_CYC[7..0]	Reg.44 INTRA_CYC	Automatic Intra cycle length. Specifies the number of Inter frames between every two automatic Intra frames: n = 0: Apply Intra mode on all frames n = 1-254: Allow n Inter frames between every two automatic Intra frames. n = 255: Never apply Intra mode automatically
FORCE_INTRA	Reg.46 FORCE_INTRA	Force Intra mode on all new frames. The software driver is supposed to set this bit temporarily to prevent a channel error from propagating to further frames. 0: Normal operation (do not force Intra) 1: Force Intra mode
FORCE_UP	Reg.47 FORCE_UP	Force usage of previous video line to compress current line. The software driver may set this bit to 1 if certain cameras are used as the video source.

		0: Normal operation (do not force) 1: Force dependency on previous line.
ACT_STRIP[3..0]	Reg.45/d4-d0 STRIP_SZ	Actual Strip width. This parameter specifies to the ZR36504 compressor how many video lines should be packed into a single strip packet. A strip packet contains up to 400 bytes.
VIRT_STRIP[3..0]	Reg.45/d7-d4 STRIP_SZ	Virtual Strip width. This parameter specifies to the ZR36504 compressor the maximum number of video lines that are allowed to be dependent. n = 0: Use same value as ACT_STRIP n = 1-14: Use 4xn lines for Virtual strip width n = 15: Use frame full height for Virtual strip width

(continued...)

Parameter	Register address	Usage
STRIP_DAT_ LIMIT[6..0]	Reg.47/d7-d1 FORCE_UP	This parameter specifies the maximum number of bytes to be packed in a single Actual Strip. The default value of this parameter is 0, and it sets the max number of bytes to 400. Any other value N between 1-127 will set the max number of bytes to 273+N.
PCM_THR1[7..0]	Reg.56 PCM_THR1	Compression Threshold 1. Recommended range: [0,20] (0 for best quality, 20 for minimum bits/pixel).
PCM_THR2[7..0]	Reg.57 PCM_THR2	Compression Threshold 2. Recommended range: [0,9] (0 for best quality, 9 for minimum bits/pixel).
DIST_THR_I[7..0]	Reg.58 DIST_THR_I	Compression Average Distortion Threshold for Inter frames. Recommended range: [0,255] (0 for best quality, 255 for minimum bits/pixel).
DIST_THR_A[7..0]	Reg.59 DIST_THR_A	Compression Average Distortion Threshold for Intra frames. Recommended range: [0,200] (0 for best quality, 200 for minimum bits/pixel).
MAX_DIST_I[7..0]	Reg.60 MAX_DIST_I	Compression Maximum Distortion Threshold for Inter frames. Recommended range: [0,50] (0 for best quality, 50 for minimum bits/pixel).
MAX_DIST_A[7..0]	Reg.61 MAX_DIST_A	Compression Maximum Distortion Threshold for Intra frames. Recommended range: [0,28] (0 for best quality, 28 for minimum bits/pixel).

YUV 4:2:2 Interleaved Format

In this format the ZR36504 transfers to host computer 2 bytes per every pixel (16-bit/pixel). The Y-component is available for every pixel, but the U and V components are each available for every second pixel (Y0,U0,Y1,V2,Y2,U2,Y3...).

YUV 4:2:0 Planar Format

In this format the ZR36504 transfers to host computer 3 bytes per every 2 pixels (12-bit/pixel). The Y-component is available for every pixel, but the U and V components are only available for every second pixel in even lines.

In this mode the host computer gets the frame already formatted in the planar mode; this can save CPU time in the host computer in most Video Conferencing applications. The Y and U/V components are packed by the ZR36504 in 64-bytes packets, and have the following structure:

Packet number	Contents
1	Pixels 0-63 of the Y-Image
2	Pixels 64-127 of the Y-Image
3	Pixels 0-63 of the U-Image (or V-Image) The U-Image and V-Image are half-size of the Y-Image in both horizontal and vertical dimensions. The ZR36504 produces a line of U pixels followed by a line of V pixels, and then U pixels again in a toggling manner. These pixels are always packed in this modulo-3 packet. The host computer - knowing the frame-size - can separate between U and V components.
4	Pixels 128-191 of the Y-Image
5	Pixels 192-255 of the Y-Image
6	Pixels 64-127 of the U-Image (or V-Image)
.	
.	
.	

Video Buffer Control registers

The ZR36504 uses a pre-defined DRAM space to store the output video data before being transferred to USB; this buffer is called Video Buffer, and it is used as a Fifo which observes data bursts at the video frame rate (up to 30Hz) and supplies data bursts at the USB frame rate (1000 packets per second).

The size of the Video Buffer is set by the host computer via the DRAM registers. Depending on USB bandwidth and output frame size and rate, this buffer may become full in the middle of a video streaming. In this case, additional frames will be dropped out by the ZR36504, until enough free space is available in buffer. When operating in the Compressed mode, the host computer can alter the compression rate by modifying some threshold registers on the fly; in this way it can prevent most of the "buffer-full" events, which results in a stable frame-rate (that is to say, frames are not dropped). To enable the host computer to monitor the status of the Video Buffer and control frame-dropping, the ZR36504 provides the following registers:

Parameter	Register address	Usage
BUF_THR [9..0]	Reg.48/d7-d0 Reg.49/d4-d3	Minimum remaining buffer space to begin frame dropping (units are in 2KB). "Buffer-Full" occurs when remaining buffer space is less than the value in this register. The host computer sets this register according to the maximum space that a video frame may occupy.
VID_BUF_LEFT [9..0]	Reg.62/d7-d0 Reg.65/d1-d0	This is a Read-Only register that provides the actual remaining buffer space (units are in 2KB). The host computer can prevent "Buffer-Full" occurrence by monitoring this register and changing compression thresholds.
LFP [19..0]	Reg.63/d7-d0 Reg.64/d6-d0 Reg.65/d3-d2	This is a Read-Only register that provides the DRAM address for data write in the Video Buffer at the end of every video-frame (units are in 16-byte). The host computer can keep track of the current compression rate by monitoring this register from time to time.

Special Video Control bits

The ZR36504 has two special bits in the VIN_REG2 register, which can alter the input video sequence. These bits are normally used during still capture operation, and are specified in the following table:

Parameter	Register address	Usage
SEND_FID	Reg.28/d5 VIN_REG2	Send FID information in frame header data. The FID information is used for reconstructing a 2-field frame from an Interlace camera. 0: Default value. 1: FID bit overrides bit 0 of Frame_Phase[4..0].
KEEP_BLANK	Reg.28/d7 VIN_REG2	Force a "blank" position on the input video frame source, and drop new frames. Software driver should take care to switch this bit from '0' to '1' during a true blank position. 0: Default value.

		1: Keep existing blank longer by forcing "blank".

USB Pipe Video Data Format

Data Packets:

The Video data is received by the host computer as a stream of bytes via End-Point 2 Isochroneous pipe. There is an incoming data packet every 1ms (every USB-Frame), and its size is limited by the maximum bandwidth that was initially set for End-Point 2; The maximum byte-count for each packet is one of the following numbers: 959 (for 7.5Mb/sec), 895, 831, 767, 703, 639, 575, 511, 447, 383, 319, 255, 191, 127, or 63 (for 0.5Mb/sec). Regarding the data on the USB - the data of a new Video-Frame always starts in a new data packet, so in most cases the last packet of a video frame is shorter than a normal packet. The ZR36504 sends one ore more empty packets between every two video frames.

Video Frame Synchronization:

In all modes of operation (Compressed or Raw video) two concurrent Video Frames will be separated by at least one empty Data Packet. This is used by the ZR36504 S/W driver to detect a Start-Of-Video-Frame. Also, the first two bytes of the Video Frame Header contain a Start-Of-Video-Frame-Pattern (=0xAA55), which are used by S/W driver as a qualifier to verify that the data represents an uncorrupted Video-Frame.

Video Frame Header:

Every Video Frame has a header that comes first. The header data is organized in Little-Endian format; That's to say, the LSB of a 2-bytes parameter comes prior to the MSB (LSB occupies the lower address). The same header format is used in all modes of operation. The following table specifies the parameters of this header:

Offset	Param. Name	No. of Bytes	Description & Specification
0	Vid_Frm_Patt	2	0xAA55 = Start of Video-Frame Pattern
2	Header_Length	1	Number of bytes in this header = 12
3	Frame_Numb	1	D4-D0: Unsigned integer. Incremented (mod 32) on every frame that is delivered to host computer. D7: Capture_Pressed (active if '1'). D6: Resumed ('1': first frame after Suspend) D5: spare
4	Frame_Phase	1	D4-D0: Unsigned integer. Incremented mod 30 on every frame that is acquired from camera. D7-D5: spare
5	Frame_Latency	1	Unsigned integer. Number of milliseconds elapsed from the moment that the camera began delivery of this frame to ZR36504, to the moment that the ZR36504 began delivery of frame-header to USB.
6	Data_Format	1	D7: '0'=Vendor Specific (like ZR36504) ('1'=Class Specific) D6: '0'=Raw Data, '1'=Compressed Data D5-D0: Vid_Format_Code: 0x03 = YUV-4:2:2 0x14 = YUV-4:2:0 Planar 0x06-0x12, 0x15-0x1F = spare 0x20 = Zoran's Compression
7	Format_Param	1	D7: Intra_Frame ('1'=Intra, '0'=Inter+Intra). This bit should be ignored in raw data frames. D6: spare

			D4-D0: Pix_Depth (number of bits per pixel). These bits should be ignored in compressed data frames.
8	Frame_Width	2	Unsigned Word integer - number of pixels per line.
10	Frame_Height	2	Unsigned Word integer - number of lines in frame.

5. DRAM Control and Interface

The ZR36504 requires an external 16bit x 256K DRAM to operate (VGA cameras require a 16bit x 1024K DRAM to provide 15f/s). The DRAM operation voltage must be 3.3v, and its access time must be 60nS or less. The ZR36504 uses the Fast-Page-Read and Fast-Page-Write DRAM access modes only. Refresh cycles are automatically inserted between Read or Write bursts by the ZR36504.
The ZR36504 allocates two ranges of memory addresses in the external DRAM, that are regarded as memory buffers:

⇒ Video Output data buffer. The ZR36504 uses this buffer as a FIFO, to store output data from its compressor (in the Compressed video mode) or from its scaler (in the Raw video mode). Previously written data is read to be sent to host computer via USB transfers (End-Point 2).

⇒ Video Frame Delay Line buffer. This buffer is used in the Compressed Video mode only. The ZR36504 uses this buffer as a huge FIFO, to store the current reconstructed frame. The compressor always needs to read the previous reconstructed frame as a reference image in the Compression Video mode.

Each of these buffers is assigned a Start-Address and an End-Address (which relate to the physical 20-bit address-space 0x00000-0xFFFFF of the DRAM). These addresses are supposed to be defined by the ZR36504 software driver as a part of the video stream initialization. The following registers of the ZR36504 are used to set the addresses of the two buffers:

Parameter	Register address	Usage
DRAM_SIZE	Reg.18/d1	'0': Selects 4Mbit DRAM (16bit x 256K) '1': Selects 16Mbit DRAM (16bit x 1024K)
DRM_COL_SLCT	Reg.18/d7	Defines address bit a19 for end of Video Output data buffer if 16Mbit DRAM used. This parameter is used as an extension for UR_LST_ROW and VDW_LST_ROW.
UR_1ST_ROW [9..0]	Reg.18/d5, Reg.19/d0, Reg.20/d7-d0	Start Address of Video Output data buffer for Read. Only a18..a9 are specified, a8..a0 are always '0' (start of a DRAM row). The bit a19 is also always '0'.
UR_LST_ROW [9..0]	Reg.18/d6, Reg.19/d1,	End Address of Video Output data buffer for Read. Only a18..a9 are specified, a8..a0 are

	Reg.21/d7-d0	always '1' (end of a DRAM row). The bit a19 is defined by DRM_COL_SLCT parameter.
FDL_1ST_ROW [8..0]	Reg.19/d2, Reg.22/d7-d0	Start Address of Video Frame Delay Line buffer. Only a17..a9 are specified, the other 11 bits are always '0' (start of a DRAM row).

(continued...)

Parameter	Register address	Usage
FDL_LST_WORD [18..0]	Reg.19/d7 Reg.19/d4-d3 Reg.23/d7-d0 Reg.24/d7-d0	End Address of Video Frame Delay Line buffer.
VDW_1ST_ROW [9..0]	Reg.18/d5 Reg.19/d5 Reg.25/d7-d0	Start Address of Video Output data buffer for Write. Normally should be equal to UR_1ST_ROW.
VDW_LST_ROW [9..0]	Reg.18/d6 Reg.19/d6 Reg.26/d7-d0	End Address of Video Output data buffer for Write. Normally should be equal to UR_LST_ROW.

Register 18/d0 of the ZR36504 contains 3 bits named RES_UR, RES_FDL, and RES_VDW. These are used to restart the appropriate FIFO pointers that are used for DRAM access. The ZR36504 software driver is supposed to set these bits to '1' and then to '0' if addresses of any of these buffers were modified.

The ZR36504 performs a Refresh cycle to DRAM from time to time. A special bit - REF - in register 18 specifies the refresh time for the whole address space. This allows the user to use either a 8.2ms refresh chip or a 128ms one (Selecting 8.2ms mode will fit both 4M and 16M DRAM types).

DRAM Interface Signals

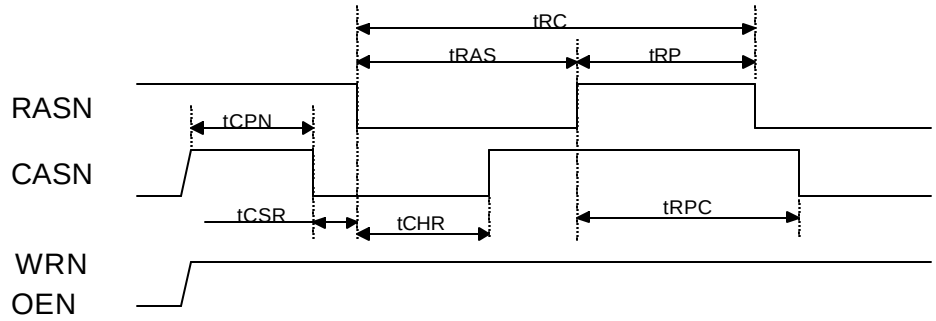
The following signals are used by the ZR36504 for DRAM access:

DA[9..0]: Address-Bus, multiplexed Row address and Column address.
If a 4Mbit DRAM is used, DA[9] should be left open.
DD[15..0]: Data-Bus, bi-directional bus with internal pull-down.
RASN: Raw-Address Select (active Low).
CASN: Column-Address Select (active Low. Can drive two DRAM pins).
WRN: Write Enable signal (active Low).
OEN: Read Enable signal (active Low).

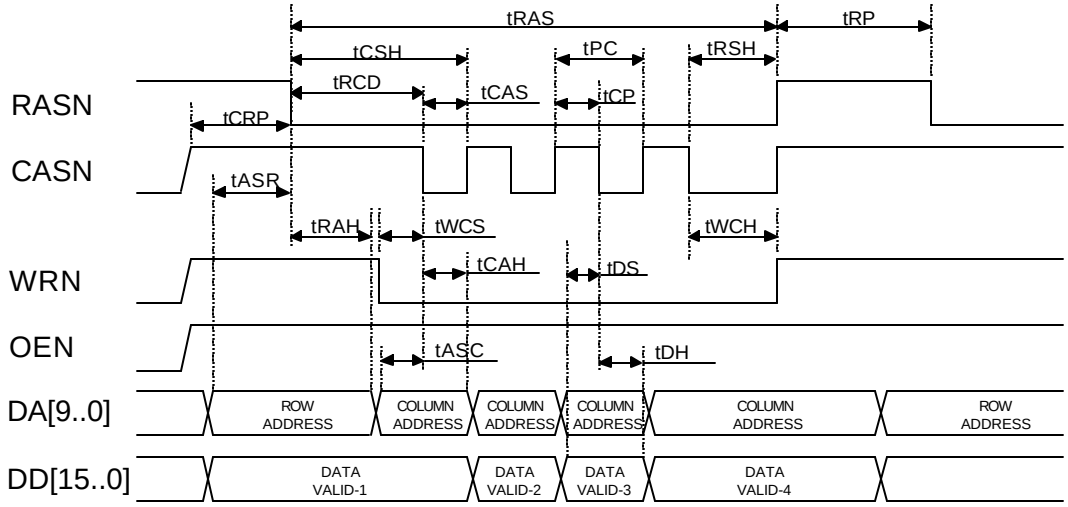
The timing table and diagrams in the following pages specify the Refresh, Fast-Page-Write, and Fast-Page-Read cycles of the ZR36504:

Symbol	Parameter	Min	Max	Unit
t_{RC}	Refresh Cycle Time	144	148	ns
t_{RAS}	RASN low pulse width	82	85	ns
t_{RP}	RASN high pulse width	60	64	ns
t_{CPN}	CASN high pulse width	60	64	ns
t_{CSR}	CASN setup time before RASN low	19	23	ns
t_{CHR}	CASN hold time after RASN low	40	44	ns
t_{RPC}	RASN high to CASN low	40	44	ns
t_{CRP}	CASN high to RASN low	60	64	ns
t_{CSH}	CASNhold time after RASNlow	81	85	ns
t_{RCD}	RASNlow to CASNlow	60	64	ns
t_{CAS}	CASN low pulse width	22	25	ns
t_{PC}	Fast page mode read/write cycle time	40	44	ns
t_{CP}	CASN high pulse width	19	23	ns
t_{RSH}	RASN hold time after CASN low	40	44	ns
t_{ASR}	Row address setup time before RASN low	5	23	ns
t_{RAH}	Row address hold time after RASN low	40	44	ns
t_{ASC}	Column address setup time before CASN low	5	23	ns
t_{WCS}	Write setup time before CASN low	19	23	ns
t_{WCH}	Write hold time after CASN low	40	44	ns
t_{CAH}	Column address hold time after CASN low	19	23	ns
t_{DS}	Write data setup time before CASN low	5	22	ns
t_{DH}	Write data hold time after CASN low	19	37	ns
t_{RAD}	Column address delay time from RASN low	40	55	ns
t_{OCH}	CASN hold time after OEN low	60	64	ns
t_{CPRH}	RASN hold time after CASN precharge	60	64	ns
t_{DSR}	Read data setup time before CASN high	2	-	ns
t_{DHR}	Read data hold time after CASN high	0	-	ns

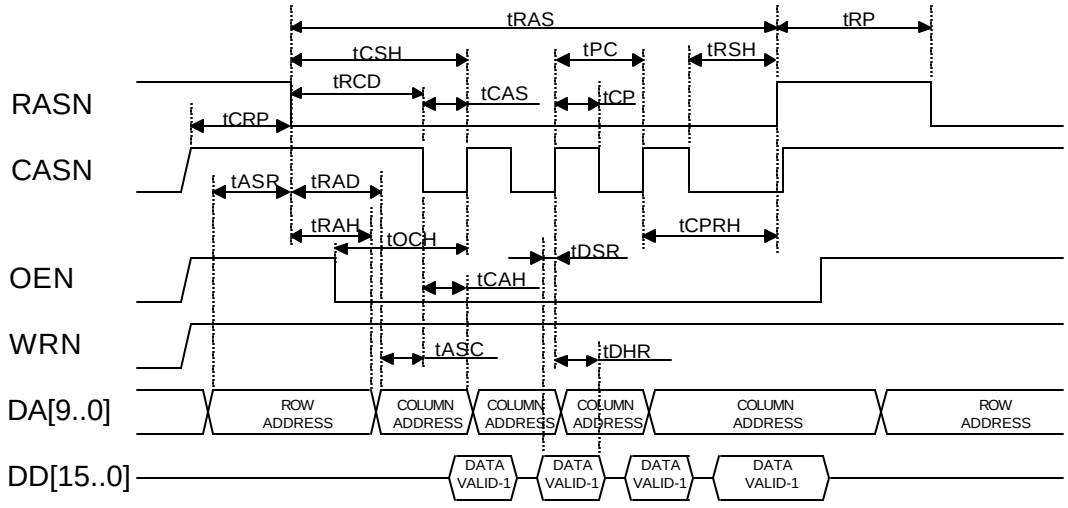
Refresh Cycle Timings



Fast-Page-mode Write Timings



Fast-Page-mode Read Timings



6. Camera Control Serial Port

The ZR36504 has a dedicated Programmable Serial Port intended to be used for camera control; this port has several modes of operation, where the ZR36504 is always the bus-master (one of the more useful modes is IICC). The programmable serial port is controlled by the host computer via the following registers of the ZR36504 register bank: SER_MODE, SER_ADRS, SER_CONT, SER_DAT1, SER_DAT2, SER_DAT3, and SER_DAT4.

Camera Control uses 3 dedicated pins of the ZR36504 pinout:

IICCK is an Open Drain output pin, used to drive the serial port clock signal. It is supposed to be connected to an external 3.3-10KΩ pull-up resistor to 3.3-5v.
IICDT is an Open-Drain bi-directional pin, used to send and receive the serial port data. It is supposed to be connected to an external 3.3-10KΩ pull-up resistor to 3.3-5v.
SENS is an Open Drain output pin, used as a serial control strobe signal in some modes of operation. It is supposed to be connected to an external 3.3-10KΩ pull-up resistor to 3.3-5v.

There are 6 modes of operation available for the Camera Control Port. These are listed in the following table, and described in more detail in the following paragraphs:

Mode Number	Mode Name	Description
0	Soft	Bit-level Software controlled mode
1	SIO	Serial clocked I/O

2	IIC LRACK	IICC with Last Byte Read Acknowledged
3	IIC LRNACK	IICC with Last Byte Read Not Acknowledged
4	CAM1	Camera 1 - refer to timing diagram
5	CAM2	Camera 2 - refer to timing diagram

Modes number 1-5 are referred as Automatic modes: In these modes the host computer only needs to write the data bytes (and the device address byte - in some of them) in certain registers (SER_DAT1 to SER_DAT4, and SER_ADRS) and initiate a transfer request; in a similar way the host computer can read received data from same registers.

The SER_MODE register has some specific bits that can turn the automatic modes into more flexible serial data formats. These register bits are:

CLK_RATE: Writing '0' to this bit will select a 93.75KHz clock at IICCK output.
Writing '1' to this bit will select a 1.5MHz clock at IICCK output.

CLK_POL: Writing '0' to this bit will select the normal polarity at IICCK output.
Writing '1' to this bit will select an inverted polarity at IICCK output.

VSYNC: Writing '0' to this bit will select an immediate transfer.
Writing '1' to this bit will delay start-of-transfer to camera blank period.

Another register that is used by the automatic modes is the SER_CONT register. This register is used by the host computer to control the serial port machine. The SER_CONT register consists of the following control bits:

SER_LEN: This field contains a 3-bits binary integer that specify the number of data bytes that the host wishes to transfer in the serial transaction (the address byte is not counted). The range of this parameter is 0 to 4.

SER_DIR: Writing '0' to this bit selects a Write operation (host to camera).
Writing '1' to this bit selects a Read operation (camera to host).

SER_GO/SER_BUSY: This is used as both a command and a status bit. Writing '1' to this bit will initiate a serial transfer request. The serial transfer will either start immediately, or wait until the vertical blank time interval is detected at the camera video signal (depends on VSYNC bit). The SER_GO/SER_BUSY bit will remain '1' till the end of transaction, to indicate to the host computer when a new transaction can be initiated.

NACK_RCV: This is a Read-Only bit, and it is used in modes 2 and 3 only (IICC

modes). The ZR36504, after completing a serial transfer of this mode, reports to the host computer via this bit whether or not all transmitted bytes were acknowledged by the camera (this includes address byte and all data bytes that were sent from host to camera). A '0' in this bit indicates all ACK, and a '1' indicates a NACK for one or more bytes.

NO_STOP: This bit is used in modes 2 and 3 only (IICC modes), and enables multiple transactions inside a single START/STOP frame. When set to '1', it informs the serial machine to omit the STOP pattern at the end of the following transaction. Combined with the CONTINUE bit, this enables the S/W driver to perform long transactions (i.e. for downloading the Gama-Correction table into camera DSP).

CONTINUE: This bit is used in modes 2 and 3 only (IICC modes), and enables multiple transactions inside a single START/STOP frame. When set to '1', it informs the serial machine to prepare for multiple transactions mode. It will never affect the following transaction, but the one coming after it, which will not contain a START pattern.

The following pages specify all the 6 modes of operation for the camera-control serial port.

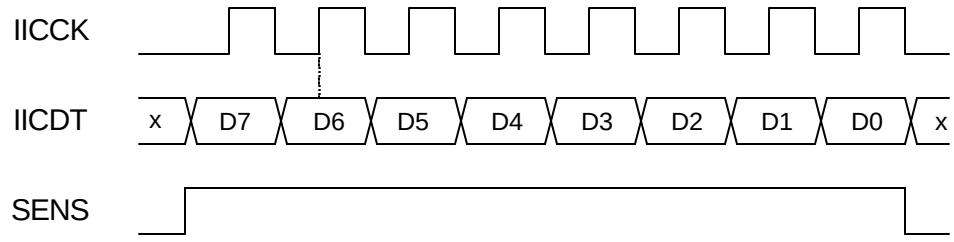
Soft Mode: (MODE=0)

This mode is selected when the MODE field (d7-d4) of the SER_MODE register is set to 0. In this mode the host computer can access the serial port pins directly, in order to enable control of cameras that are not supported by the other automatic modes.

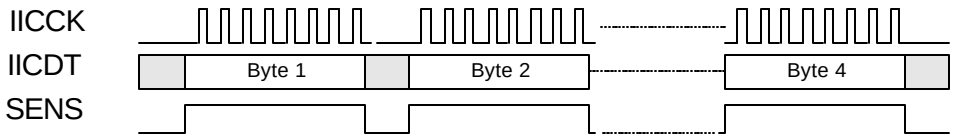
In the Soft mode, the value of CLK_OUT bit (d0) is reflected in the IICCK output pin. A Write operation to the DAT_IO bit (d1) sets the value of the IICDT pin; A Read operation from the same DAT_IO bit reads the actual voltage level at the IICDT pin. The value of SENS_OUT bit (d2) is reflected in the SENS output pin.

SIO Mode: (MODE=1)

This is the Serial Clocked I/O automatic mode, and it is selected when the MODE field (d7-d4) of the SER_MODE register is set to 1. The following waveform describe the SIO mode:



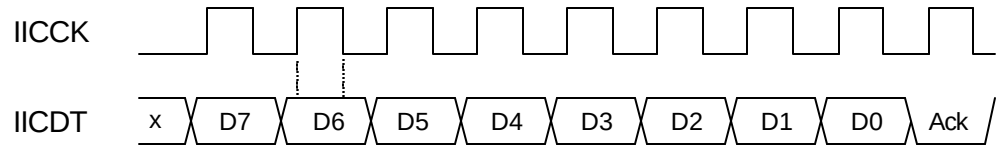
NOTE: In both Read and Write sequence, data is sampled in the up-going edge of the clock IICCK.



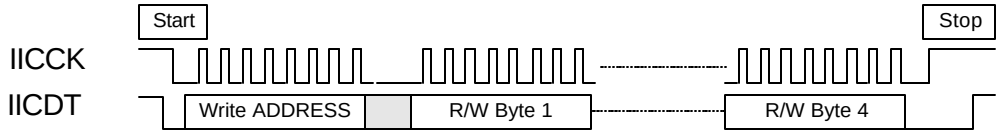
NOTE: In the SIO mode 1 to 4 bytes are written or read.

IIC LRACK Mode: (MODE=2)

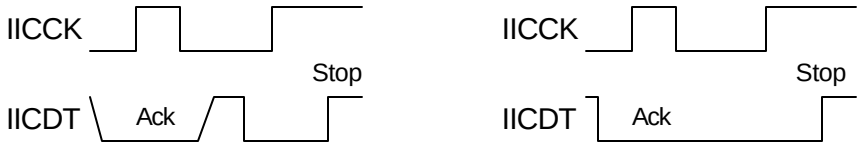
This is the IIC LRACK (Last Read Acknowledged) automatic mode, and it is selected when the MODE field (d7-d4) of the SER_MODE register is set to 2. In this mode, the IICCK frequency is set to 93.75KHz.



NOTE: In both Read and Write sequence, data should be stable during the '1' state of the clock IICCK. D7-D0 are sent by transmitter, Ack is sent by receiver.



NOTE: Start is defined when the IICDT turns from '1' to '0' while the IICCK is '1'. Stop is defined when the IICDT turns from '0' to '1' while the IICCK is '1'. The Address byte is written like any other byte.



End of Write sequence

End of Read sequence

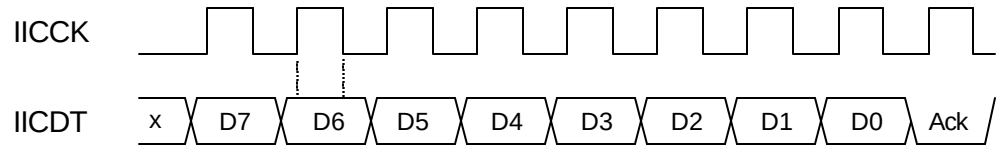
In this mode, The host defines the camera address byte and the data bytes to be written to the camera in the appropriate registers; then the ZR36504 sends these bytes automatically. In a similar way the ZR36504 can read data bytes from the camera. The ZR36504 acknowledges the last byte read like all the other bytes.

By using the NO_STOP and CONTINUE bits, one can perform a concatenation of multiple IICC transactions, in order to send or receive more than 4 bytes in a single START/STOP frame. Also, by using these control bits, one can combine Write/Read operations with a single STOP pattern at the end. Note that the SER_LEN parameter can be set to 0 to further support the concatenation mode of operation.

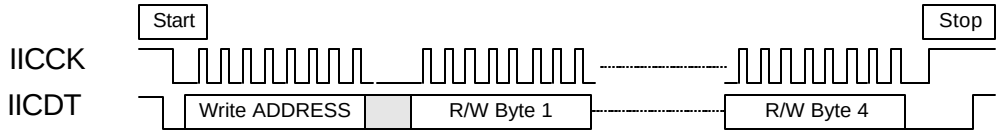
IIC LRNACK Mode: (MODE=3)

This is the IIC LRNACK (Last Read Not Acknowledged) automatic mode, and it is selected when the MODE field (d7-d4) of the SER_MODE register is set to 3. In this mode, the IICCK frequency is set to 93.75KHz.

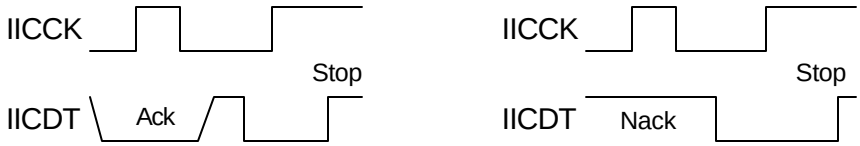
In this mode, the host defines the camera address byte and the data bytes to be written to the camera in the appropriate registers; then the ZR36504 sends these bytes automatically. In a similar way the ZR36504 can read data bytes from the camera. The ZR36504 does not acknowledge the last byte read from camera; this is done as a signaling to the camera, that no more bytes are needed. The waveforms for this mode of operation are specified in the following page.



NOTE: In both Read and Write sequence, data should be stable during the '1' state of the clock IICCK. D7-D0 are sent by transmitter, Ack is sent by receiver.



NOTE: Start is defined when the IICDT turns from '1' to '0' while the IICCK is '1'. Stop is defined when the IICDT turns from '0' to '1' while the IICCK is '1'. The Address byte is written like any other byte.



End of Write sequence

End of Read sequence

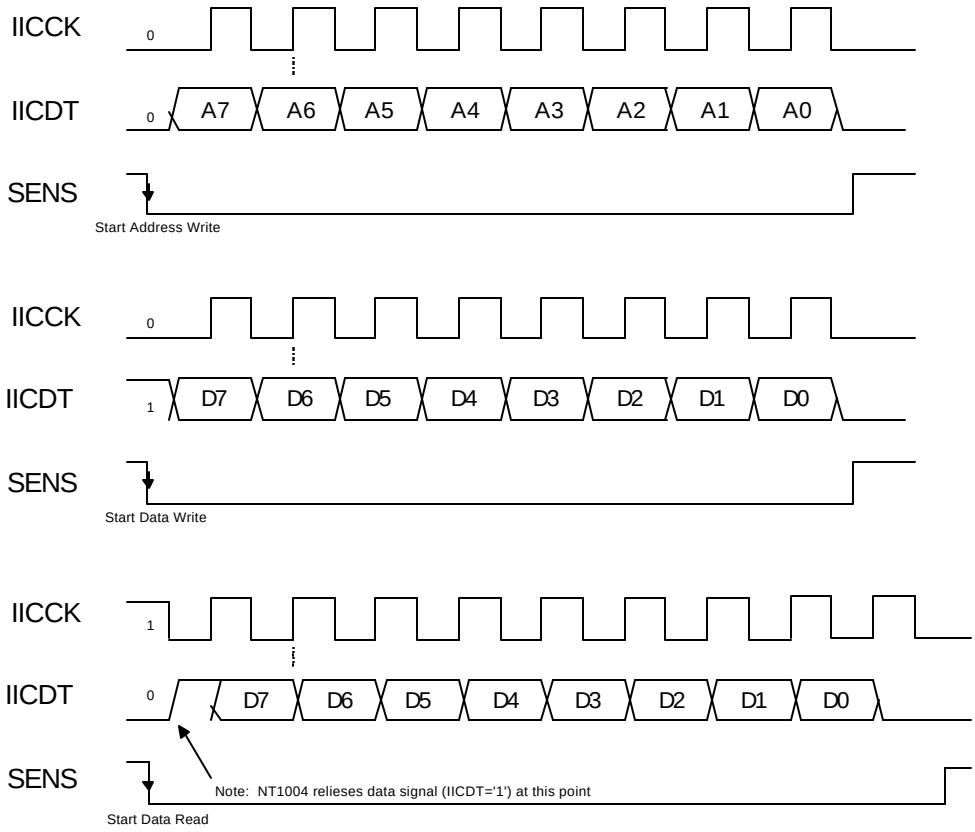
In this mode, The host defines the camera address byte and the data bytes to be written to the camera in the appropriate registers; then the ZR36504 sends these bytes automatically. In a similar way the ZR36504 can read data bytes from the camera. The ZR36504 does not acknowledge the last byte read (Nack).

By using the NO_STOP and CONTINUE bits, one can perform a concatenation of multiple IICC transactions, in order to send or receive more than 4 bytes in a single START/STOP frame. Also, by using these control bits, one can combine Write/Read operations with a single STOP pattern at the end. Note that the SER_LEN parameter can be set to 0 to further support the concatenation mode of operation.

CAM1_Mode: (MODE=4)

This mode is selected when the MODE field (d7-d4) of the SER_MODE register is set to 4. In this mode, the IICCK frequency must not exceed 10MHz.

In this mode three signals are used: IICCK, IICDT, and SENS. The host defines the desired camera register address byte and a single data byte to be written to that register in the appropriate ZR36504 registers; then the ZR36504 first sends the address and then the data automatically. In a similar way the ZR36504 can read a data byte from any given camera register. The waveforms for the CAM1 mode are specified in the following diagram. Note that every byte transfer has its own start condition, which indicates one of 3 possibilities: Address Write, Data Write, or Data Read.



Register Write operation:	Address Write	Data Write
Register Read operation:	Address Write	Data Read

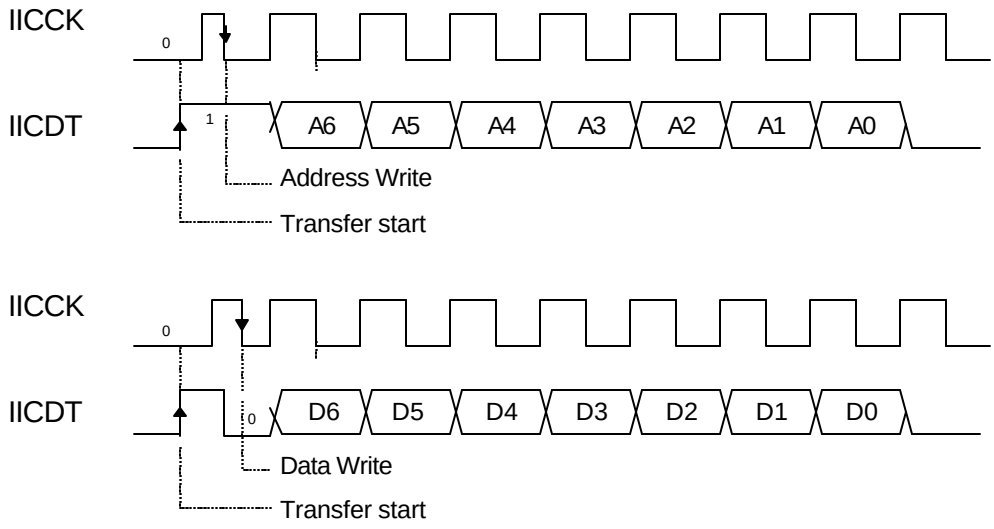
NOTE: A transaction consists of Address Write, followed by Data Write or Data Read.

CAM2 Mode: (MODE=5)

This mode is selected when the MODE field (d7-d4) of the SER_MODE register is set to 5. In this mode, the IICCK frequency must not exceed 10MHz.

In this mode only two signals are used: IICCK, and IICDT. The host defines the desired camera register address byte and a single data byte to be written to that register in the appropriate ZR36504 registers; then the ZR36504 first sends the address and then the data automatically. Note that in this mode both address and data consist of 7-bit only; In this mode there is no way to read data from camera. The waveforms

for the CAM2 mode are specified in the following diagram. Note that every byte transfer has its own Transfer start signaling (which is identical for both address and data), followed by an Address Write condition or a Data Write condition.



Register Write operation:

Address Write	Data Write

NOTE: Data is sampled on the down-going edge of the clock IICCK. A transaction consists of Address Write, followed by Data Write.

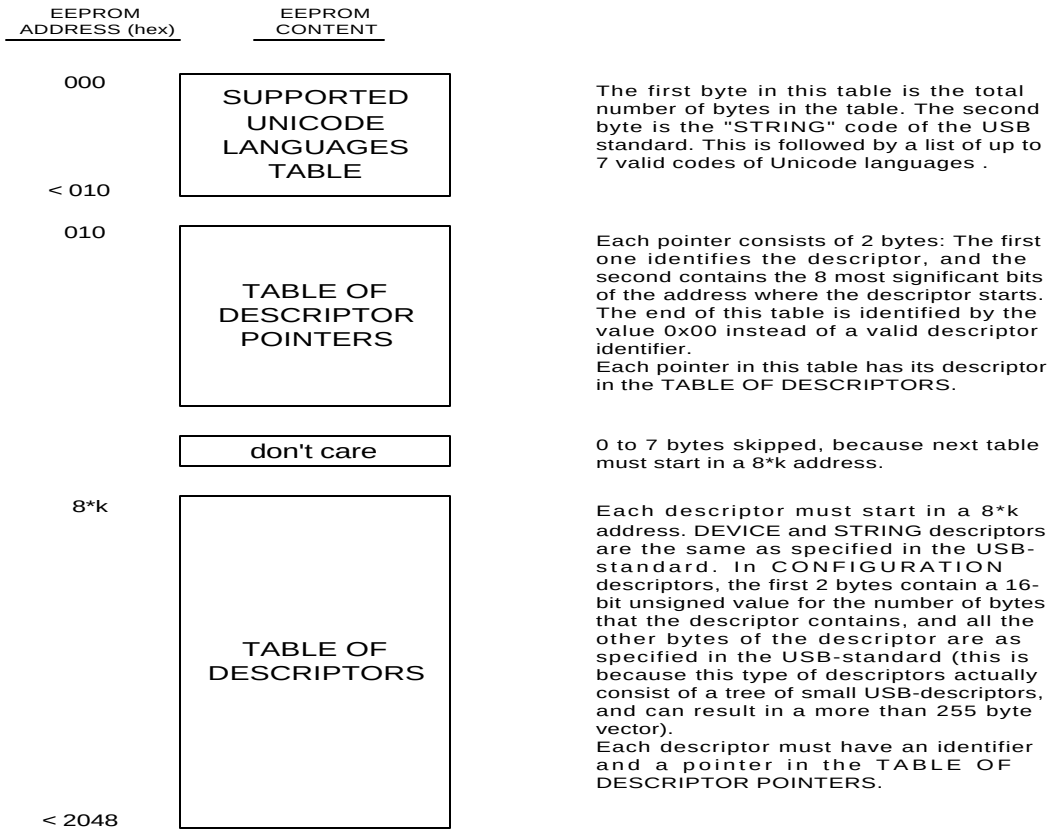
7. External EEPROM

The ZR36504 provides a full USB compliant solution without the need for an external EEPROM (USB Vendor ID is pin programmable). Anyway, when *UNICODE* names are required, the ZR36504 can use an external 3.3v 2KB Serial EEPROM as an optional source for USB descriptors. There are several vendors that produce these 8-pin EEPROM chips, which are pin-to-pin compatible.

Normally the external EEPROM will be only read in a working device (mainly soon after USB insertion). Anyway, the ZR36504 supports On-Board EEPROM programming, which can be used to alter some USB descriptors - especially the product serial number. The ZR36504 register bank includes special registers to perform a byte Read or Write operation to a given address of the EEPROM.

EEPROM Data Structure

The EEPROM contains the Device-descriptor, up to 4 Configuration-descriptors, and up to 15 String-descriptors in up to 7 different languages. The following diagram specifies the block structure of the EEPROM data:


EEPROM ADDRESS (hex)
EEPROM CONTENT
000
SUPPORTED UNICODE LANGUAGES TABLE
< 010
010
TABLE OF DESCRIPTOR POINTERS
don't care
8*k
TABLE OF DESCRIPTORS
< 2048
The first byte in this table is the total number of bytes in the table. The second byte is the "STRING" code of the USB standard. This is followed by a list of up to 7 valid codes of Unicode languages .
Each pointer consists of 2 bytes: The first one identifies the descriptor, and the second contains the 8 most significant bits of the address where the descriptor starts. The end of this table is identified by the value 0x00 instead of a valid descriptor identifier.
Each pointer in this table has its descriptor in the TABLE OF DESCRIPTORS.
0 to 7 bytes skipped, because next table must start in a 8*k address.
Each descriptor must start in a 8*k address. DEVICE and STRING descriptors are the same as specified in the USB-standard. In CONFIGURATION descriptors, the first 2 bytes contain a 16-bit unsigned value for the number of bytes that the descriptor contains, and all the other bytes of the descriptor are as specified in the USB-standard (this is because this type of descriptors actually consist of a tree of small USB-descriptors, and can result in a more than 255 byte vector).
Each descriptor must have an identifier and a pointer in the TABLE OF DESCRIPTOR POINTERS.

Supported UNICODE Language Table:

This table is used as the "string" of index 0, which is defined in the USB-Standard. This "string" is actually a list of all the LANGIDs that are supported by the device. The first two bytes in this table are needed for the standard format of USB String descriptors.

EEPROM ADDRESS (hex)	EEPROM DATA (hex)	DESCRIPTION
000	**blength**	Number of bytes in this table (4-16). This is needed for the standard format of USB String descriptors.
001	**STRING** descriptor type (=03)	Code of STRING descriptor type (=03). This is needed for the standard format of USB String descriptors.
002	**LANGID#1** (LSB)	Bits 7-0 of Language-Identifier of language #1. This language must be supported, and it is also used as the default language if the host specifies a language that is not included in this list.
003	**LANGID#1** (MSB)	Bits 15-8 of Language-Identifier of language #1.
004	LANGID#2 (LSB)	Optional. Bits 7-0 of Language-Identifier of language #2. Must contain FF if not used.
005	LANGID#2 (MSB)	Optional.Bits 15-8 of Language-Identifier of language #2. Must contain FF if not used.
006	LANGID#3 (LSB)	Optional. Bits 7-0 of Language-Identifier of language #3. Must contain FF if not used.
007	LANGID#3 (MSB)	Optional.Bits 15-8 of Language-Identifier of language #3. Must contain FF if not used.
008	LANGID#4 (LSB)	Optional. Bits 7-0 of Language-Identifier of language #4. Must contain FF if not used.
009	LANGID#4 (MSB)	Optional.Bits 15-8 of Language-Identifier of language #4. Must contain FF if not used.
00A	LANGID#5 (LSB)	Optional. Bits 7-0 of Language-Identifier of language #5. Must contain FF if not used.
00B	LANGID#5 (MSB)	Optional.Bits 15-8 of Language-Identifier of language #5. Must contain FF if not used.
00C	LANGID#6 (LSB)	Optional. Bits 7-0 of Language-Identifier of language #6. Must contain FF if not used.
00D	LANGID#6 (MSB)	Optional.Bits 15-8 of Language-Identifier of language #6. Must contain FF if not used.
00E	LANGID#7 (LSB)	Optional. Bits 7-0 of Language-Identifier of language #7. Must contain FF if not used.
00F	LANGID#7 (MSB)	Optional.Bits 15-8 of Language-Identifier of language #7. Must contain FF if not used.

Table Of Descriptor Pointers

This table is used by the ZR36504 to locate the start address of a given descriptor. Each item in this table consists of a Descriptor Identifier byte (first byte), and EEPROM address (second byte - contains only 8 most significant bits of address; the other 3 bits always equal '000').

EEPROM ADDRESS (hex)	EEPROM DATA (hex)	DESCRIPTION
010	**DDI** (=40)	Device-Descriptor Identifier code (=40). This descriptor must exist in EEPROM.
011	**DD address**	Device-Descriptor address in this EEPROM (in this table, units are in 8-byte steps for address pointers).
012	**CDI#0** (=20)	Configuration-Descriptor Identifier # 0 code (=20). This descriptor must exist in EEPROM. bits 7-2: '001000' (code of Configuration-Descriptor)

		bits 1-0: '00' (Configuration Index).
013	**CD#0 address**	Configuration-Descriptor #0 address.
	CDI#1 (=21)	Optional. Configuration-Descriptor Identifier # 1 code.
	CD#1 address	Optional. Configuration-Descriptor #1 address.
	CDI#2 (=22)	Optional. Configuration-Descriptor Identifier # 2 code.

(continued...)

(continued...)

EEPROM ADDRESS (hex)	EEPROM DATA (hex)	DESCRIPTION
	CD#2 address	Optional. Configuration-Descriptor #2 address.
	CDI#3 (=23)	Optional. Configuration-Descriptor Identifier # 3 code.
	CD#3 address	Optional. Configuration-Descriptor #3 address.
	SDI#1,0 (=90)	String-Descriptor Identifier Lang#1 Indx#0 (=90). This descriptor is actually the first table in EEPROM. bit 7: '1' bits 6-4: '001' (Language number in language-table) bits 3-0: '0000' (String Index).
	SDI#1,0 address (=00)	String-Descriptor #1,0 address (=00).
	SDI#2,0 (=A0)	String-Descriptor Identifier Lang#2 Indx#0 (=A0). This descriptor is actually the first table in EEPROM.
	SDI#2,0 address (=00)	String-Descriptor #1,0 address (=00).
	SDI#3,0 (=B0)	String-Descriptor Identifier Lang#3 Indx#0 (=B0). This descriptor is actually the first table in EEPROM.
	SDI#3,0 address (=00)	String-Descriptor #3,0 address (=00).
	SDI#4,0 (=C0)	String-Descriptor Identifier Lang#4 Indx#0 (=C0). This descriptor is actually the first table in EEPROM.
	SDI#4,0 address (=00)	String-Descriptor #4,0 address (=00).
	SDI#5,0 (=D0)	String-Descriptor Identifier Lang#5 Indx#0 (=D0). This descriptor is actually the first table in EEPROM.
	SDI#5,0 address (=00)	String-Descriptor #5,0 address (=00).
	SDI#6,0 (=E0)	String-Descriptor Identifier Lang#6 Indx#0 (=E0). This descriptor is actually the first table in EEPROM.
	SDI#6,0 address (=00)	String-Descriptor #6,0 address (=00).
	SDI#7,0 (=F0)	String-Descriptor Identifier Lang#7 Indx#0 (=F0). This descriptor is actually the first table in EEPROM.
	SDI#7,0 address (=00)	String-Descriptor #7,0 address (=00).
	SDI#n1,m1	Optional. String-Descriptor Identifier Lang#n1 Indx#m1. bit 7: '1' bits 6-4: n1 (Language number in language-table) bits 3-0: m1 (String Index).
	SDI#n1,m1 address	Optional. String-Descriptor #n1,m1 address.
	SDI#n2,m2	Optional. String-Descriptor Identifier Lang#n2 Indx#m2.

SDI#n2,m2 address	Optional. String-Descriptor #n1,m1 address.
. .	. .
SDI#nk,mk	Optional. String-Descriptor Identifier Lang#nk Indx#mk.
SDI#nk,mk address	Optional. String-Descriptor #nk,mk address.
EOT (=00)	End-Of-Table code (=00).

Table Of Descriptors

This table contains the DEVICE descriptor, all CONFIGURATION descriptors, and all STRING descriptors. DEVICE and STRING descriptors are organized exactly as specified in USB standard. CONFIGURATION descriptors start with a word (= 2 bytes - LSB first, then MSB) that specifies the number of total bytes in the descriptor (not including the first 2 bytes), followed by the descriptor's body which is organized exactly as specified in USB standard.

Notes:

- The Supported UNICODE Languages Table is also used as STRING descriptor #0 for all languages.
- There is one and only one DEVICE descriptor, which is always 18 bytes long.
- A descriptor always starts at a 8*k address of the EEPROM (the 3 least significant bits of the address are '000'). This means that there can be up to 7 unused bytes between any two descriptors in the table.

EEPROM Access Registers

EEPROM access via the ZR36504 registers is enabled when the E2_EN bit in the PWR_REG register is set. The following registers are used for EEPROM access:

Parameter	Register address	Usage
E2_EN	Reg.0/d7 E2_EN	Enable EEPROM access. 0: Default after Reset. EEPROM access disabled. 1: Enable EEPROM Read and Write(1)
EE_DATA[7..0]	Reg.14 EE_DATA	Data Byte to be written to EEPROM. Also, last Data Byte that was read from EEPROM.
EE_LSBAD[7..0]	Reg.15 EE_LSBAD	8 Least Significant bits of byte address in EEPROM to be accessed.
EE_MSBAD[10..8]	Reg.16/d2-d0	3 Most Significant bits of byte address in EEPROM to be accessed.
EE_DIR	Reg.16/d3 EE_DIR	Select EEPROM access direction: 0: Select Write operation to EEPROM. 1: Select Read operation from EEPROM.
EE_GO/EE_BUSY	Reg.16/d4 EE_GO/ EE_BUSY	This is used as both a command and a status bit. Writing '1' to this bit will initiate a byte Read or Write. The SER_GO/SER_BUSY bit will remain '1' till the end of operation, to indicate to the host computer when a EEPROM access can begin.(2)

Notes:

(1) Write operation to EEPROM requires EEPROM WP pin to be grounded.

(2) A Write operation requires additional 10ms in the EEPROM internal circuits.

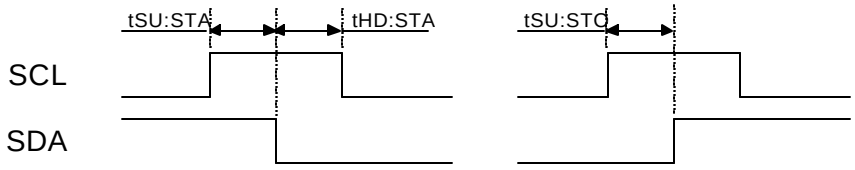
EEPROM Control Signals

The SCL/PWR0 and SDA/EEPROM pins of the ZR36504 are the EEPROM control signals. The SCL/PWR0 is used as the clock output, and the SDA/EEPROM signal is used as the data I/O.
During Reset operation, the ZR36504 samples its SDA/EEPROM pin to determine if an external EEPROM is connected. If an external EEPROM does not exist (SDA/EEPROM='0'), the ZR36504 automatically uses its internal ROM for USB descriptors; in this case, the ZR36504 relates to hard-coding of the pins SCL/PWR0 and PWR1 to determine the current-consumption parameter for the Configuration-Descriptor. The following table summarizes these two modes of operation:

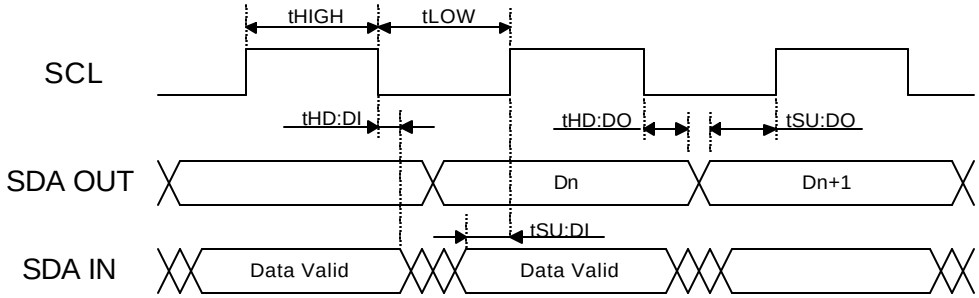
Internal ROM mode	External EEPROM mode
SDA/EEPROM pin connected to GND. SCL/PWR0 and PWR1 pins are hard-coded to determine device current consumption for Configuration-Descriptor: PWR1 SCL/PWR0 Current 0 0 200mA 0 1 300mA 1 0 400mA 1 1 500mA	SDA/EEPROM pin connected to 10K pull-up resistor (3.3v to 5.0v). External Serial 2K*8 EEPROM is connected: SDA/EEPROM connected to Serial-Data (SDA). SCL/PWR0 connected to Serial-Clock (SCL).

The following timing diagram and table specify the EEPROM control waveforms that the ZR36504 generates:

Start/Stop Timings



Data Timings



Symbol	Parameter	Min	Max	Unit
$t_{SU:STA}$	START condition setup time	5300	-	ns
$t_{HD:STA}$	START condition hold time	5300	-	ns
$t_{SU:STO}$	STOP condition setup time	5300	-	ns
t_{HIGH}	Clock high time	5300	-	ns
t_{LOW}	Clock low time	5300	-	ns
$t_{SU:DO}$	Data output setup time	2500	2670	ns
$t_{HD:DO}$	Data output hold time	2500	2670	ns
$t_{SU:DI}$	Data input setup time	20	-	ns
$t_{HD:DI}$	Data input hold time	0	-	ns

8. ZR36504 USB and Status Registers

The ZR36504 has some registers that allow software driver to directly read and affect some USB device parameters. These are specified in the following table:

Parameter	Register address	Usage
CONFIG_REG	Reg.1 CONFIG_ REG	Read Only register. Contains the Device Configuration number.
ADRS_REG	Reg.2/d6-d0 ADRS_REG	Read Only register. Contains the Device Address.
ALTER_REG	Reg.3/d3-d0 ALTER_REG	Read Only register. Contains the Alternate setting for End-Point 2 (Video bandwidth). Regarding this value as a binary number in the range [1,15], the number of bytes sent in the Isochronous pipe of EP2 in every millisecond is: N = (16-ALTER_REG)*64 - 1 USB Bandwidth = (16-ALTER_REG)*0.5 Mbit/sec
NEW_ALT	Reg.4/d3-d0 FORCE_ ALTER_REG	New Alternate setting for End-Point 2, (Video bandwidth), to replace the original setting. This can be used to lower the actual used bandwidth temporarily, without letting know the Operating System.
FORCE_ALT	Reg.4/d7 FORCE_ ALTER_REG	Force New Alternate. 0: Use original setting. 1: Select NEW_ALT value.
VFRM_BLNK	Reg.5/d0 STATUS_ REG	Read Only register. 0: Valid region of input video frame. 1: Blank or unused region of input video frame.
EE_CLK_FORCE [2..0]	Reg.16/d7-d5 EE_CONT	Read Only register. These 3 bits reflect the logical level of the following pins of the ZR36504: EE_CLK_FORCE[0] = SCL/PWR0 pin. EE_CLK_FORCE[1] = PWR1 pin. EE_CLK_FORCE[2] = SDA/EEPROM (1) pin.
WD_EN & WD_COUNT[7..0]	Reg.0/d0 Reg.53/d7-d0	Some USB host controllers may start an Isochronuos IN transaction too much time after the SOF (Start of USB Frame point). This means that long IN transactions may exceed the 1mS time interval of the USB frame, and cause the USB host controller to disconnect the device. The ZR36504 uses an internal Watch Dog timer to eliminate such problems. The Watch Dog operates if WD_EN control bit is set to '1'. It then starts to count 686uS after the SOF pattern, and automatically terminates any Isochronuos transaction when reaching the value of WD_COUNT register. Every one count is equivalent to 1.33uS. Note that the value of WD_COUNT should be no more than 0xE9 in order to take any effect.

(1) As sampled during Reset operation. '1' indicates existence of external EEPROM.

9. Programmable I/O Pins and 48MHz output pin

The ZR36504 has two programmable I/O pins for general purpose usage. These are IO-1 and IO-2 pins, which are Open-Drain.

Each of these pins - if used - must be connected to an external pull-up resistor to 3.3-5.0v (if not used, it can be tied to GND). The external pull-up resistor should be in the range 1-10KΩ.

To use these pins as inputs, the host computer should write '1' to the appropriate bit in the IOPIN_REG register (in the ZR36504 register bank); these are IO_1 and IO_2 bits respectively. In this condition, the voltage level presented on the IO-1 or IO-2 pin can be read by the host computer via the appropriate bit ('0' represents <0.8v, '1' represents >2.0v).

To use these pins as outputs, the host computer should write the output value to the appropriate bit in the IOPIN_REG register; In this condition, and assuming that no external device forces the voltage level presented on the IO-1 or IO-2 pin, the written value will be reflected out ('0' will generate 0v, '1' will generate 3.3-5.0v).

Upon a Power On Reset or a USB-Reset operation, the IO-1 and IO-2 pins are cleared to '0'. In the Suspend mode these pins are temporarily set to High-Z.

The ZR36504 can provide a 48MHz clock output for general purpose usage. The pin CLK48 is dedicated for this usage, and is enabled when the CLK48_EN bit is set to '1' (Reg.0/d3). When not enabled, the output level in this pin is constant '0'.
The 48MHz output is 50% duty cycle with 1nS jitter, and is derived from the external 12MHz crystal (an internal analog PLL is used).

10. Audio Channel

The audio channel in the ZR36504 is based on a serial 64-512Kb/s data stream from the ZR36504 to the host computer (USB Isochronuos mode is used for this stream). The 64-512Kb/s stream comes from a 8,000/16,000 S/sec 16/8-bit audio samples at the external audio CODEC(s). Two external CODECs should be used for Stereo mode recordings. The 8/16KHz sampling clock is derived from the 12MHz external crystal.

The ZR36504 pins for the external Codec interface are BCLK, FS_L, FS_R, and DAT_IN.

The following table specifies the AUDIO_CONT register (Register address = 50):

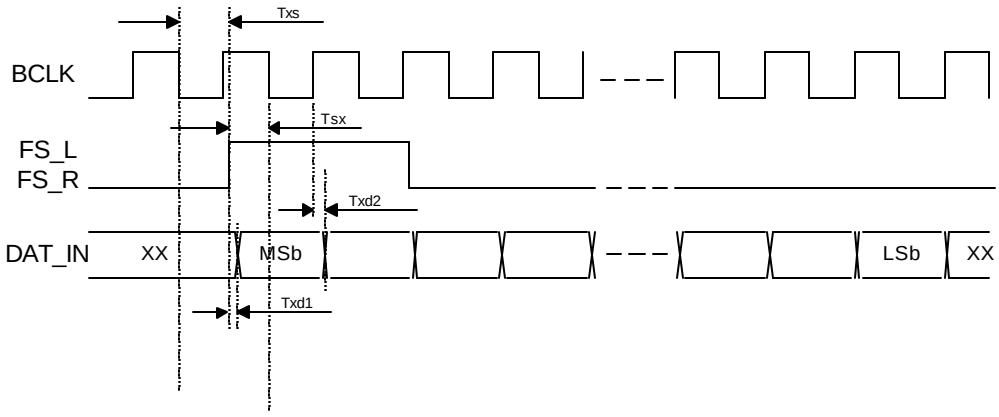
Bit #	Name	Description
0	E_A	'0': Disables Audio channel. Set FS_L and FS_R outputs to constant '0'. If E_B is also '0', BCLK is set to constant '0'. '1': Enable Audio channel.
1	E_B	'0': Disable Bulk Data input. Set BLK_FULL output to constant '0'. If E_A is also '0', BCLK is set to constant '0'. '1': Enable Bulk Data input.
3-2	BPS	'00': 8-bit per sample. '01': 12-bit per sample (Occupies 2 bytes. Bits d3-d0 of second byte are set to '0000'). '10': 14-bit per sample (Occupies 2 bytes. Bits d1-d0 of second byte are set to '00'). '11': 16-bit per sample.
4	S/M	'0': Selects Mono mode. FS_L output is active, FS_R output is constant '0'. '1': Selects Stereo mode. Both FS_L and FS_R outputs are active.
5	FS	'0': Set sampling rate to 8,000 Samp/Sec. '1': Set sampling rate to 16,000 Samp/Sec.
7-6	BK	'00': BCLK frequency is not defined. '01': Select BCLK frequency = 64KHz. '10': Select BCLK frequency = 1.544MHz. '11': Select BCLK frequency = 2.048MHz.

In addition to the AUDIO_CONT register, there is the AUD_PK_LEN register (Register address = 51), to select the maximum packet size to be sent via the audio Isochronuos pipe. This number is limited by 128, which is the maximum number of bytes that the ZR36504 audio fifo can contain. The S/W driver should set this register to a value that fits the USB descriptor for the E.P#3 maximum packet length (which is 66 if not using an external EEPROM).

Codec Interface

The Codec Interface is Long Frame Sync Timing based. The BCLK frequency can be selected to be - 2048KHz, 1536KHz, or 64KHz, which enables the designer to use almost any family of low cost Codecs available in market.

In the Long Frame Sync Timing modes, the MSb of the "transmitted" data is always expected soon after the rising edge of the FS_L (or FS_R) signal. The ZR36504 produces a positive pulse of 2 BCLK cycles in these output pins every 125us (8KHz) or every 62.5us (16KHz), which indicates the start of sample as specified in the following waveform diagram:



The BCLK is derived out of the 12MHz clock from the crystal. This results in a 4.3% jitter at the BCLK signal.

The following table specifies the minimum and maximum time intervals for the Codec Interface waveform diagram:

Parameter	Symbol	Min	Max	Unit
Hold Time from BCLK Low to FS_L / FS_R High	Txs	180	-	ns
Setup Time from FS_L / FS_R High to BCLK Low	Tsx	180	-	ns
Delay Time to valid data from FS_L / FS_R	Txd1	-	200	ns
Delay Time from BCLK High to DAT_IN valid	Txd2	-	200	ns
Jitter at the Bit Clock signal BCLK	Cj	-	4.3	%

11. Bulk Channel

The Bulk channel in the ZR36504 is capable of transferring serial data from an external source to the host computer at a bit rate of up to 2Mbit/sec. It uses a bulk end point (E.P#4), with a maximum packet length that can be specified a value between 1-64 bytes (the USB standard does not allow a bulk packet of more than 64 bytes).

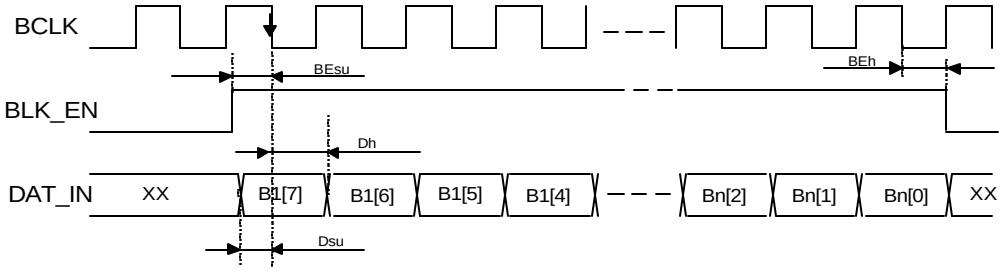
The Bulk channel takes advantage of the existing interface for the audio codec. In order to work simultaneously with the audio channel, the external data source should be able to stop the data transfer from time to time - as specified in the Bulk waveform diagram.

The ZR36504 pins for the Bulk channel interface are BCLK, DAT_IN, BLK_EN, and BLK_FULL. The signals FS_L and FS_R should be monitored by the data source logic, in order to coexist with the audio channel.

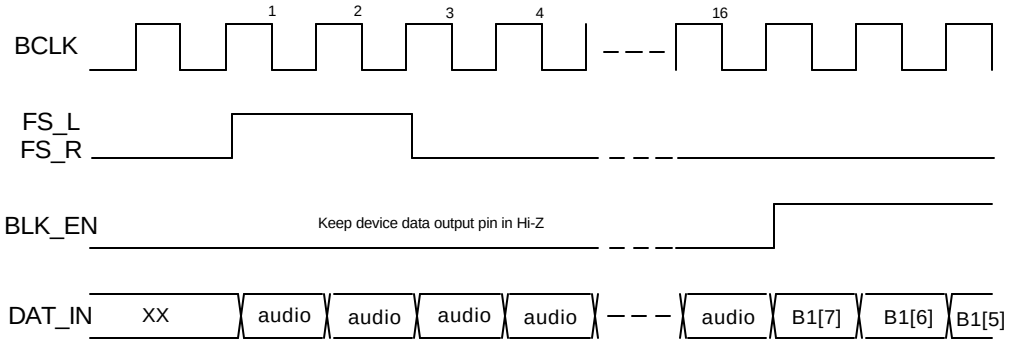
The following table specifies the control registers that are used for controlling the Bulk channel:

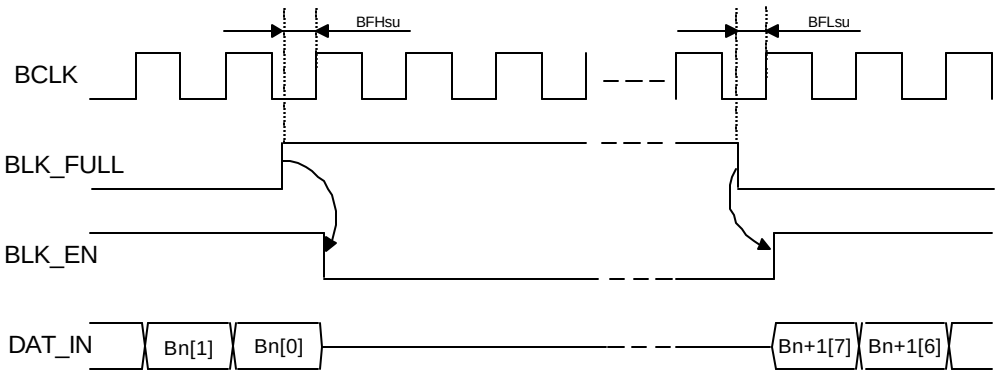
Control Name	Description
E_B Reg.50/d1	'0': Disable Bulk Data input. Set BLK_FULL output to constant '0'. If E_A is also '0', BCLK is set to constant '0'. '1': Enable Bulk Data input.
BLK_PK_LEN[6..0] Reg.52/d6-d0	This register specifies the maximum number of bytes to be sent in a single USB Bulk packet. This must be a number between 0-64, and it should fit the content of USB descriptor (64 if no external EEPROM used). This register directly affects the bit rate capability of the Bulk channel. The actual bit rate is also limited by the BCLK frequency, which can be 64KHz, 1544KHz, or 2048KHz. A bit rate of 2Mbit/sec can be reached only in computers that are capable of performing more than one packet in a USB frame (OHCI).

The following waveform diagrams specifies the procedure and timings for the ZR36504 Bulk interface. Note that the input data is sampled on the falling edge of the BCLK clock signal. The BLK_EN input is set to '1' by the sending device to indicate the beginning of a byte sequence; it should always turn to '1' before the most significant bit of the first byte, and return to '0' after the least significant bit of the last byte in sequence. When the BLK_FULL output of the ZR36504 turns '1', the sending device should wait (by switching BLK_EN to '0') until the BLK_FULL indication returns to '0'.



If the audio channel is enabled, the sending device should wait at least 16 clock cycles after the FS_L (or FS_R) pulse before beginning to send its own data. During this time it should keep its data out signal in the Hi-Z state, in order not to interfere with the audio data.





Parameter	Symbol	Min	Max	Unit
Setup Time from BLK_EN High to BCLK Low	BEsu	100	-	ns
Hold Time from BCLK Low to BLK_EN Low	BEh	100	-	ns
Setup Time from DAT_IN valid to BCLK Low	Dsu	100	-	ns
Hold Time from BCLK Low to DAT_IN valid	Dh	100	-	ns
Setup Time from BLK_FULL High to BCLK High	BFHsu	80	-	ns
Hold Time from BLK_FULL Low to BCLK High	BFLsu	0	-	ns
Jitter at the Bit Clock signal BCLK	Cj	-	4.3	%

12. Software Package

Following is a description of the software components provided with the ZR36504:

WDM Video streaming class MiniDriver -

- MS® standard connection and streaming in kernel mode (Capture, Still)
- MS® standard property sets (TV Tuner, Crossbar)
- MS® standard way of exposing data formats.
- MS® standard way of controlling stream flow.

all interfaces are exposed through DirectShow architecture. VFW interfaces are also available via WDM to VFW mapper, provided by Microsoft.

WDM Audio streaming class MiniDriver - streamss audio data from the ZR36504 chip.

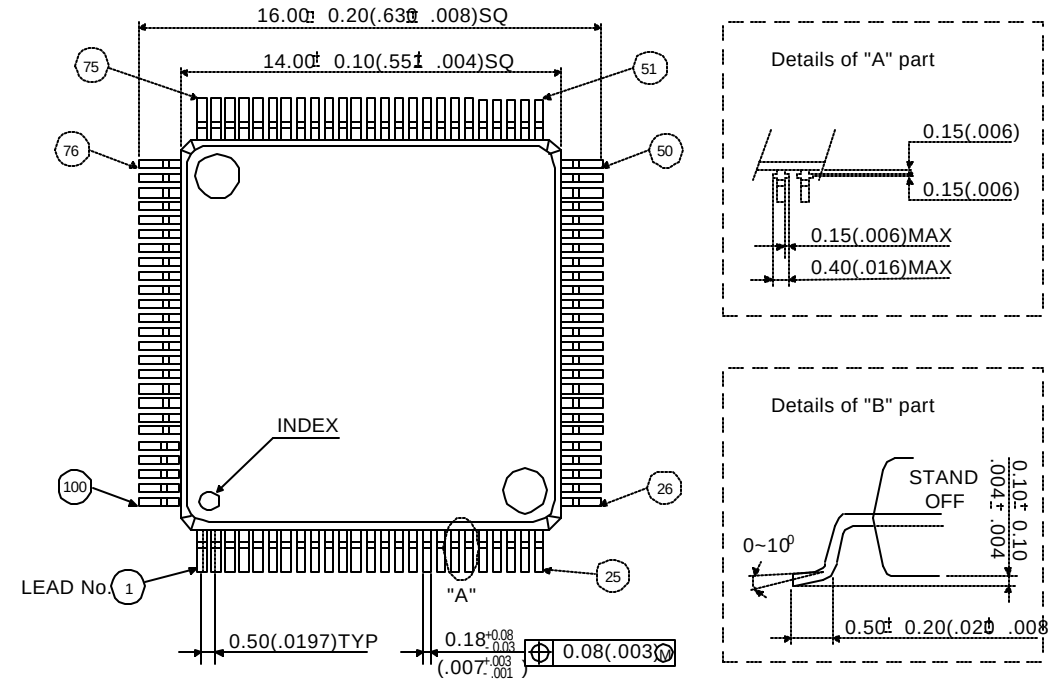
TWAIN Compliant Driver - The package includes a TWAIN compliant driver for high resolution still capture. The GUI of the TWAIN driver displays live video for preview.

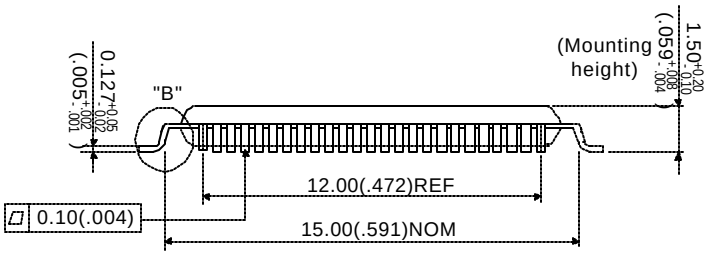
EEPROM Programming Application - An application for programming the ZR36504 EEPROM to contain vendor specific USB Descriptors. It allows to set the Device and Manufacturer names as well as the Serial Number for the device.

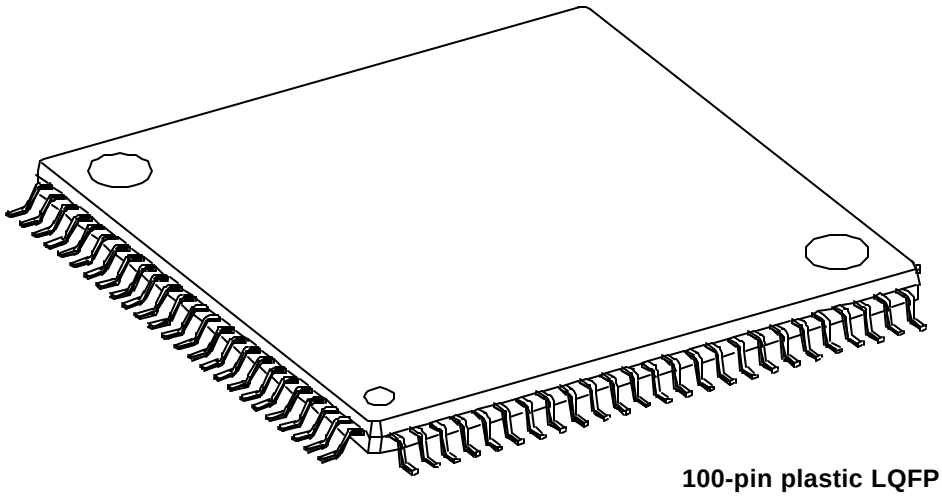
The drivers are supplied with INF file for easy installation. Customization is done by modifying the name strings in the INF file.

13. Mechanical Specification

Dimensions in mm (inches).







100-pin plastic LQFP

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