CMOS 4-BIT MICROCONTROLLER

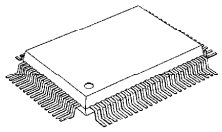
TMP47P847VF

The 47P847V is the system evaluation LSI of 47C647/847 with 64K bits one-time PROM. The 47P847V programs / verifies using an adapter socket to connect with PROM programmer, as it is in TMM2764AD.
In addition, the 47P847V and the 47C647/847 are pin compatible. The 47P847V operates as the same as 47C647/847 by programming to the internal PROM.

PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P847VF	OTP 8192 × 8-bit	512 × 4-bit	QFP80-P-1420-0.80B	BM1135

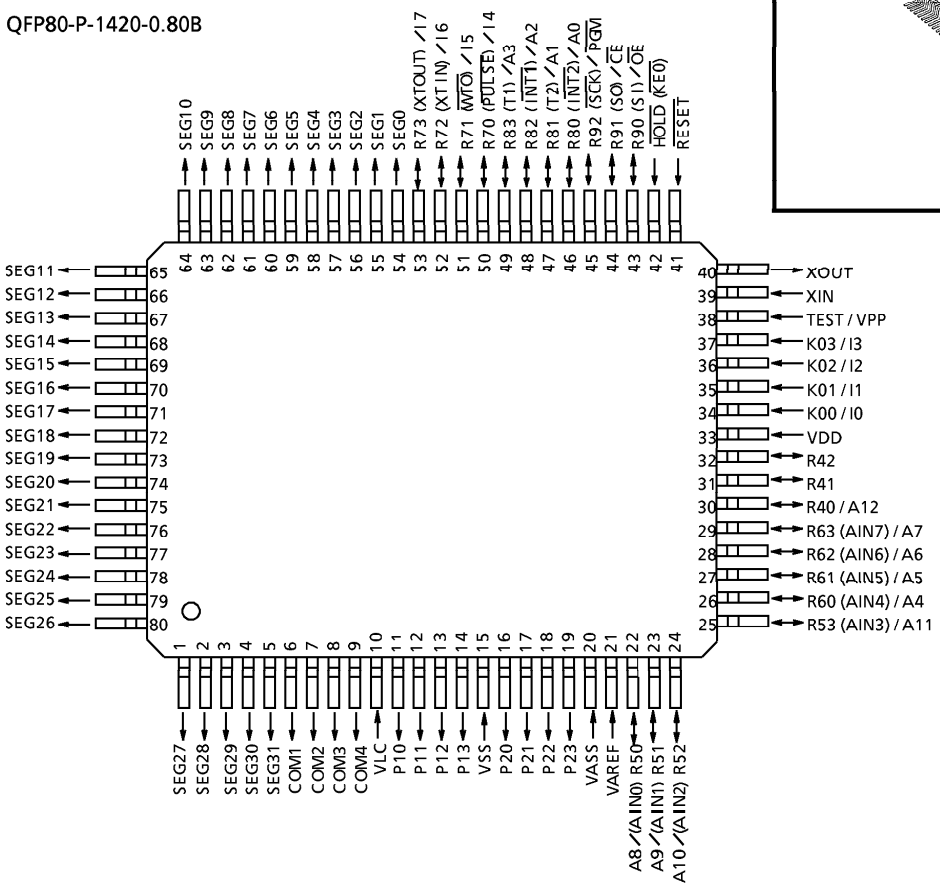
PIN ASSIGNMENT (TOP VIEW)

QFP80-P-1420-0.80B



TMP47P847VF

QFP80-P-1420-0.80B



PIN FUNCTION

The 47P847V has MCU mode and PROM mode.

(1) MCU mode

The 47C847 and the 47P847V are pin compatible (TEST pin for out-going test, Be fixed to low level).

(2) PROM mode

PIN NAME	Input/Output	FUNCTIONS	PIN NAME (MCU MODE)
A12	Input	Address inputs	R40
A11 - A8			R53 - R50
A7 - A4			R63 - R60
A3 - A0			R83 - R80
I7 - I4	I/O	Data inputs / outputs	R73 - R70
I3 - I0			K03 - K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
SEG31 - SEG0	Output	Open	
COM4 - COM1			
VLC	Power supply		
P13 - P10	I/O	Be fixed to low level	
P23 - P20			
R42 - R41			
$\overline{RESET}$	Input	PROM mode setting pins. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pins	
XOUT	Output		
VAREF	Power supply	Be fixed to VSS level	
VASS			

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P847V.
The 47P847V is the same as the 47C647 / 847 except that an EPROM or OTP is used instead of a Mask ROM.

1. OPERATION MODE

The 47P847V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST / VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C647 / 847, except that the TEST / VPP pin does not have pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C847. Data conversion tables must be set in two locations when using the 47P847V to check 47C647 operation.

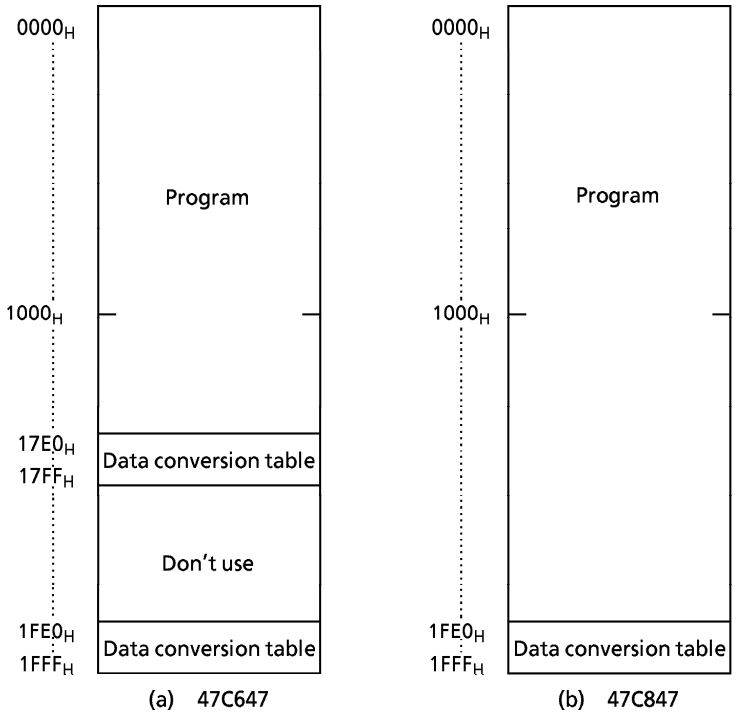


Figure 1-1. Program area

1.1.2 Data Memory

The 47P847V has 512x4-bit data memory banks (RAM).
When using the 47P847V as a 47C647 evaluator, do not write data to address 80_H and following, even though the bank1 addresses are 00 to FF_H. There is no necessary to take into consideration a special function Shared area because one is built in bank0.

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C647/847 except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the 47P847V is the same as I/O code GA of the 47C647/847.
External resistance, for example, is required when using as evaluator of other I/O codes (GB to GC) (Refer to Figure 1-2).

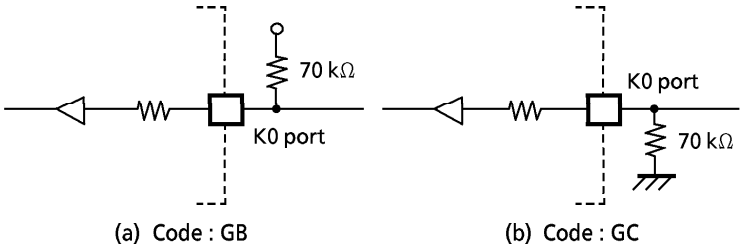


Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, K00 and K01 pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM2764AD).

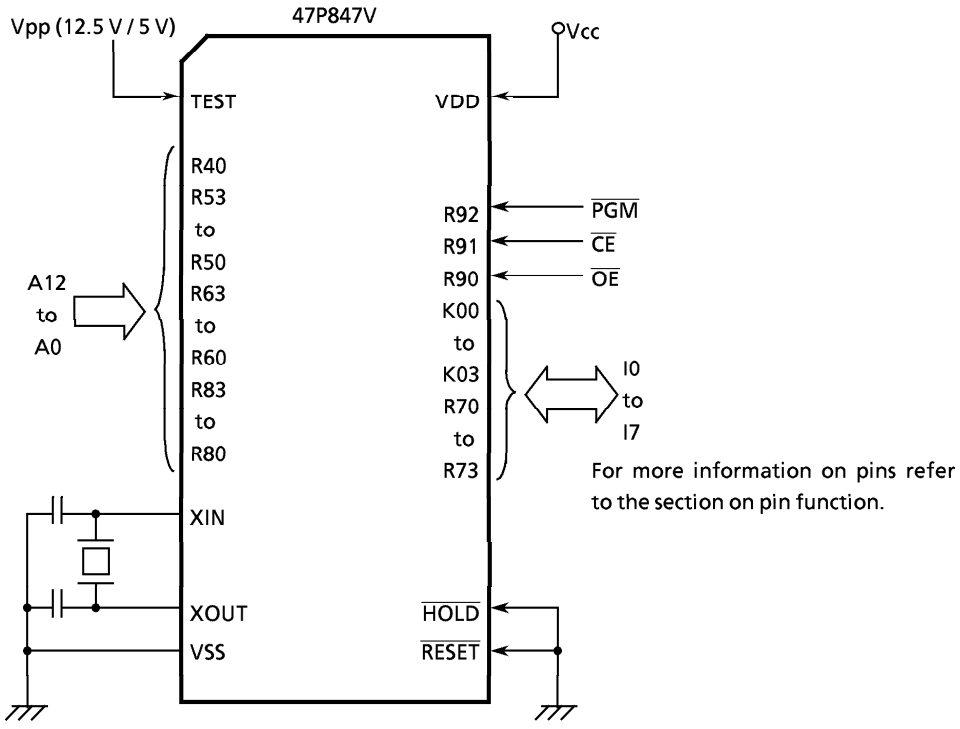


Figure 1-3. Setting for PROM mode

1.2.1 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (12.5V) is applied to the Vpp terminal with Vcc = 6V and $\overline{PGM}$ = V_{IH4}. The programming is achieved by applying a Single TTL low level 1 msec, pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 msec is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

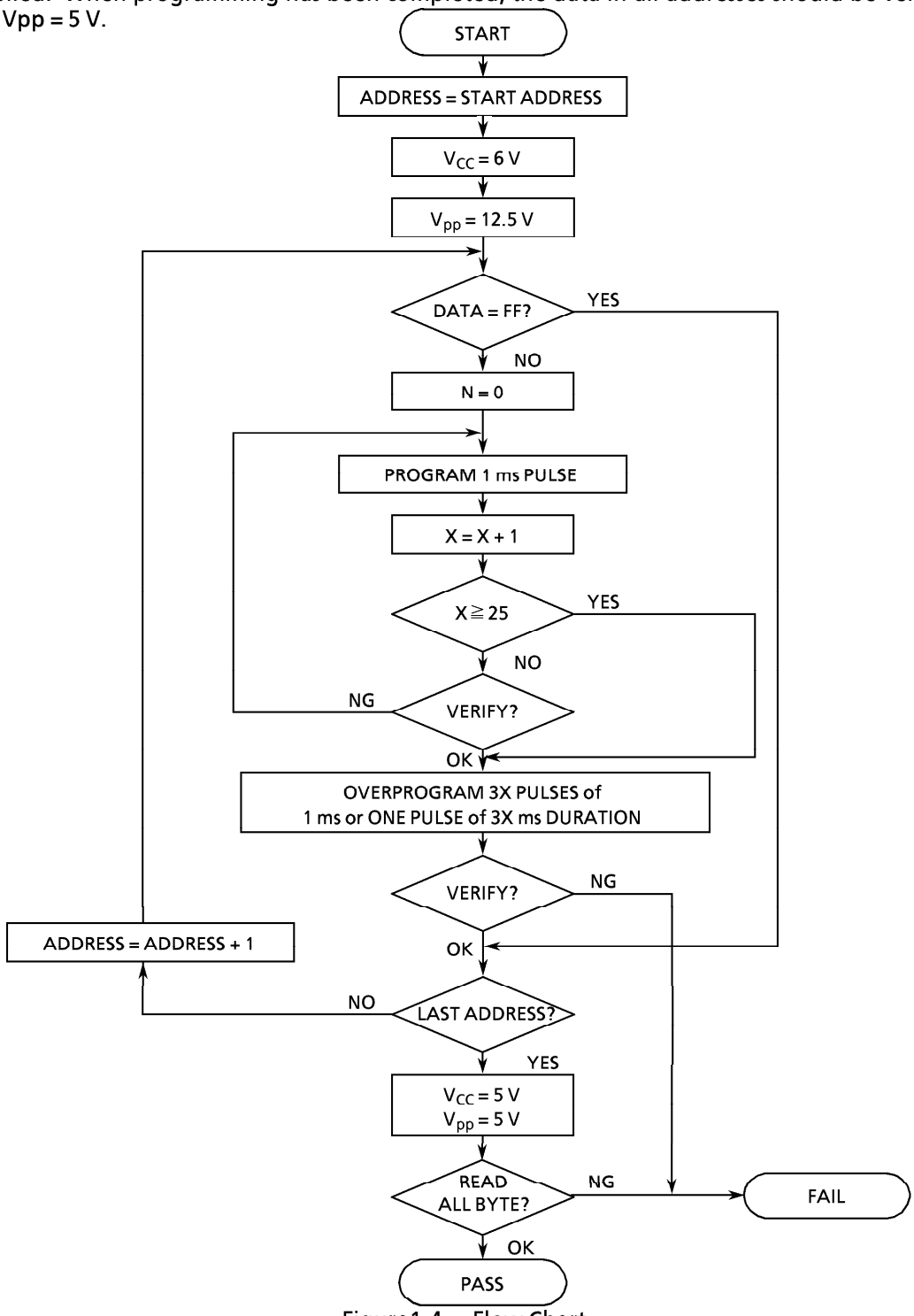


Figure1-4. Flow Chart

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Program Voltage	V_{PP}	TEST/VPP pin	– 0.3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	R4, R5, R7, Push-pull ports	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	P1, P2, R6, R8, R9 ports	– 0.3 to 10	
Output Current (per 1 pin)	I_{OUT1}	Ports P1, P2	15	mA
	I_{OUT2}	Ports R4 to R9	3.2	
Output Currnent (Total)	ΣI_{OUT1}	Ports P1, P2	60	mA
Power Dissipation [T_{opr} = 70 ℃]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 40 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the SLOW mode	2.7		
			In the SLEEP mode			
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	kHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the SLOW, SLEEP and HOLD mode.

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Open drain R port					
Input Low Current	I_{IL}	Push-pull R port	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Input Registance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO}	Open drain ports P, R	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output High Voltage	V_{OH}	Push-pull R port	V_{DD} = 4.5V, I_{OH} = – 200 μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT XTOUT and ports P1, P2	V_{DD} = 4.5V, I_{OL} = 1.6 mA	—	—	0.4	V
Output Low Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	—	10	—	mA
Segment Output Low Registance	R_{OS1}	SEG pin	V_{DD} = 5V, V_{DD} – V_{LC} = 3V	—	20	—	kΩ
Segment Output Low Registance	R_{OC1}	COM pin					
Common Output High Registance	R_{OS2}	SEG pin		—	200	—	
Common Output High Registance	R_{OC2}	COM pin					
Segment/Common Output Registance	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4 MHz	—	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0V, fs = 32.768 kHz	—	30	60	μA
Supply Current (in the SLEEP mode)	I_{DDL}			—	15	30	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Output Resistance R_{OS}, R_{OC} ; Shows on-resistance at the level switching.

Note 4. $V_{O2/3}$; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5. $V_{O1/2}$; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.

Note 6. $V_{O1/3}$; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 7. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3V/0.2V
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.

Note 8. Supply Current I_{DDS}, I_{DDL} ; V_{IN} = 2.8V/0.2V.
Only low frequency clock is only osillated (connecting XTIN, XTOUT).

Note 9. When using LCD, it is necessary to consider values of $R_{OS1/2}$ and $R_{OC1/2}$.

Note 10. Times for SEG / COM output switching on ; R_{OS1}, R_{OC1} : 2/fs (s)
R_{OS2}, R_{OC2} : 1/(n · f_F)
(1/n : duty, f_F : frame frequency)

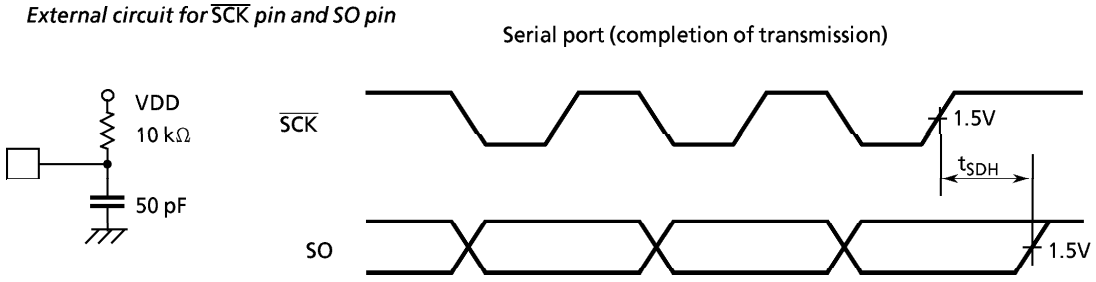
A / D CONVERSION CHARACTERRISTICS (T_{opr} = – 40 to 70 ℃)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	1.5	
Analog Reference Voltage Range	ΔV_{AREF}	$V_{AREF} - V_{ASS}$	2.5	–	–	V
Analog input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}		–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 4.5 to 6.0V, V_{SS} = 0.0V $V_{AREF} = V_{DD} \pm 0.001V$ V_{ASS} = 0.000V	–	–	± 1	LSB
Zero pornt Error			–	–	± 1	
Full scale Error			–	–	± 1	
Totar Error			–	–	± 2	

A.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70 ℃)

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode	1.3	–	20	μs
		in the SLOW mode	235	–	267	
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low level Clock Pulse Width	t_{WCL}					
A / D Conversion Sampling Time	t_{AIN}	fc = 4 MHz	–	4	–	μs
Shift Data Hold Time	t_{SDH}		0.5 t_{cy} – 300	–	–	ns

Note. Shift data Hold Time:
External circuit for $\overline{SCK}$ pin and SO pin



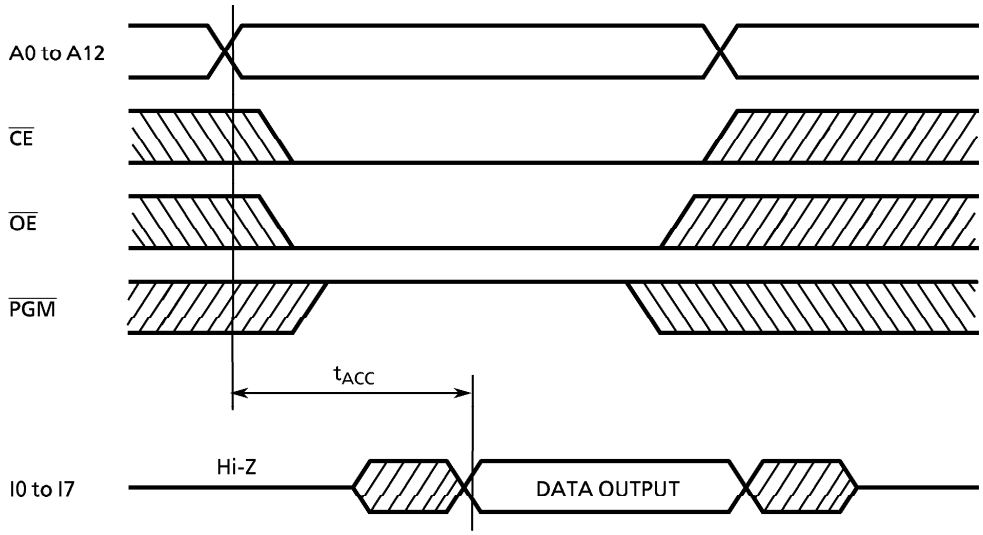
RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70 ℃)

Recommended oscillating conditions of the 47P847V are equal to the 47C847's.

DC/AC CHARACTERISTICS (V_{SS} = 0V)

(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.1$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	0	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.1$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.00	12.50	13.00	V
Programming Pulse Width	t_{PW}	V_{CC} = 6.0 ± 0.25V	0.95	1.0	1.05	ms