LH531000B

CMOS 1M (128K × 8) MROM

FEATURES

- 131,072 words × 8 bit organization
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 192.5 mW (MAX.)
  Standby: 550 µW (MAX.)
- Programmable $\overline{CE}$/OE/$\overline{OE}$
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
- Mask ROM specific pinout

DESCRIPTION

The LH531000B is a mask-programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

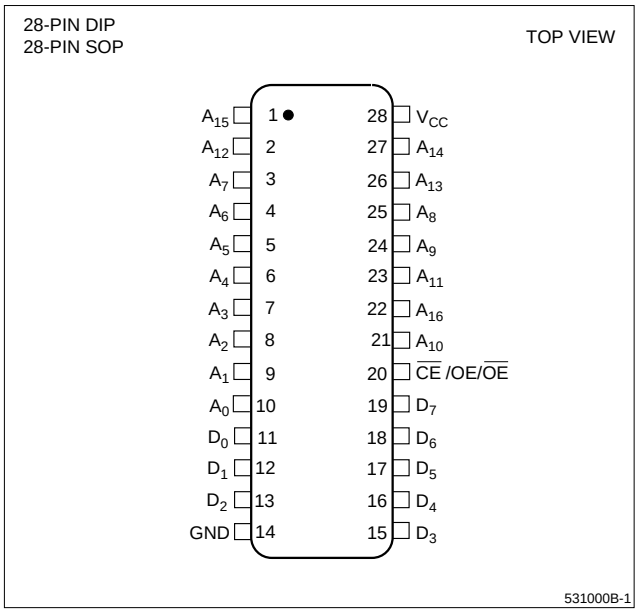


Figure 1. Pin Connections for DIP and SOP Packages

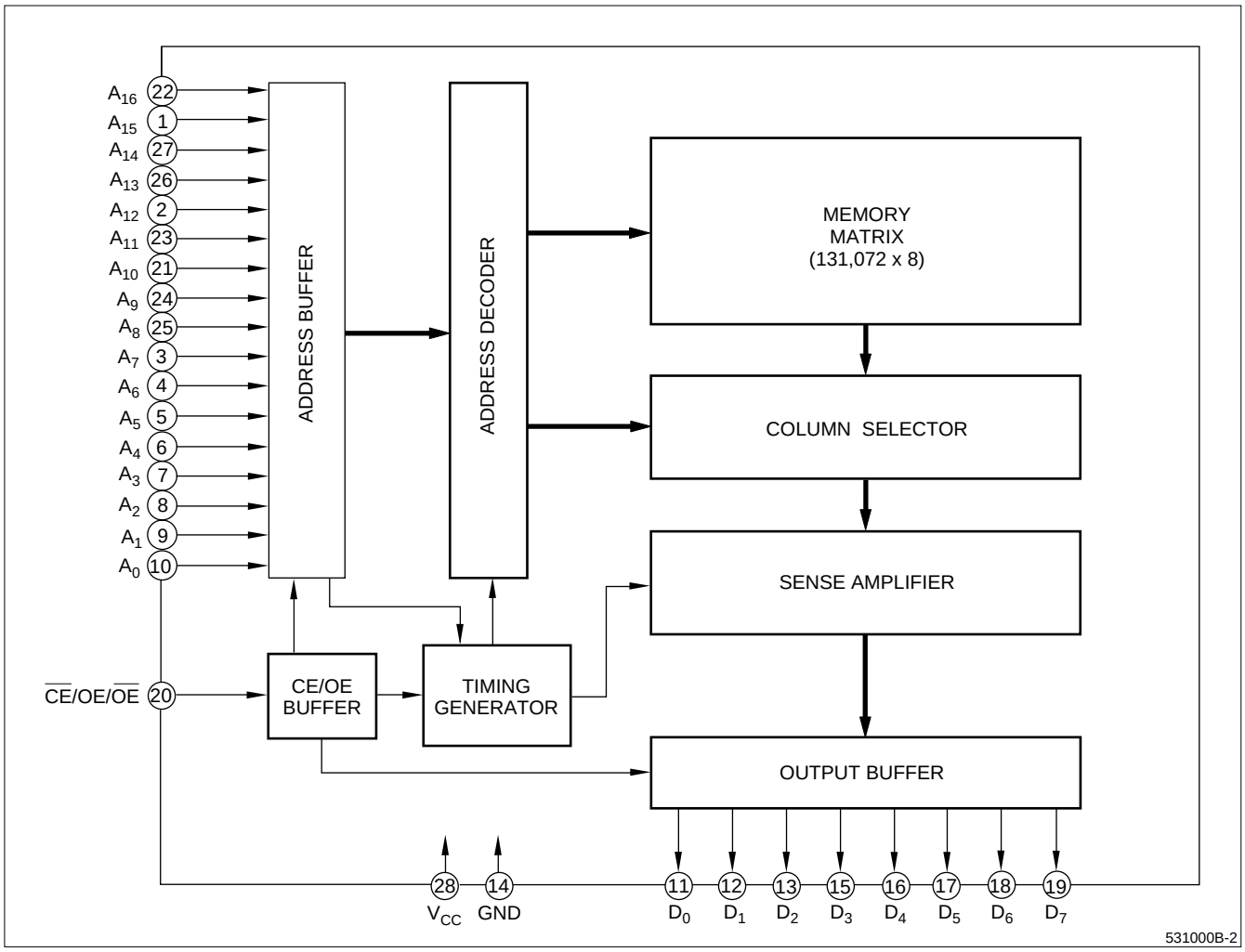


Figure 2. LH531000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$/OE/$\overline{OE}$	Chip Enable input or Output Enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active level of $\overline{CE}$/OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

PIN 20	$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT
CE type	L	–	Selected	D_{OUT}	Operating (I_{CC})
	H	–	Non selected	High-Z	Standby (I_{SB})
OE type	–	H/L	Selected	D_{OUT}	Operating (I_{CC})
	–	L/H	Non selected	High-Z	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	–0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		–0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = –400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} – 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz T_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V. $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable time	t_{OE}			70	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

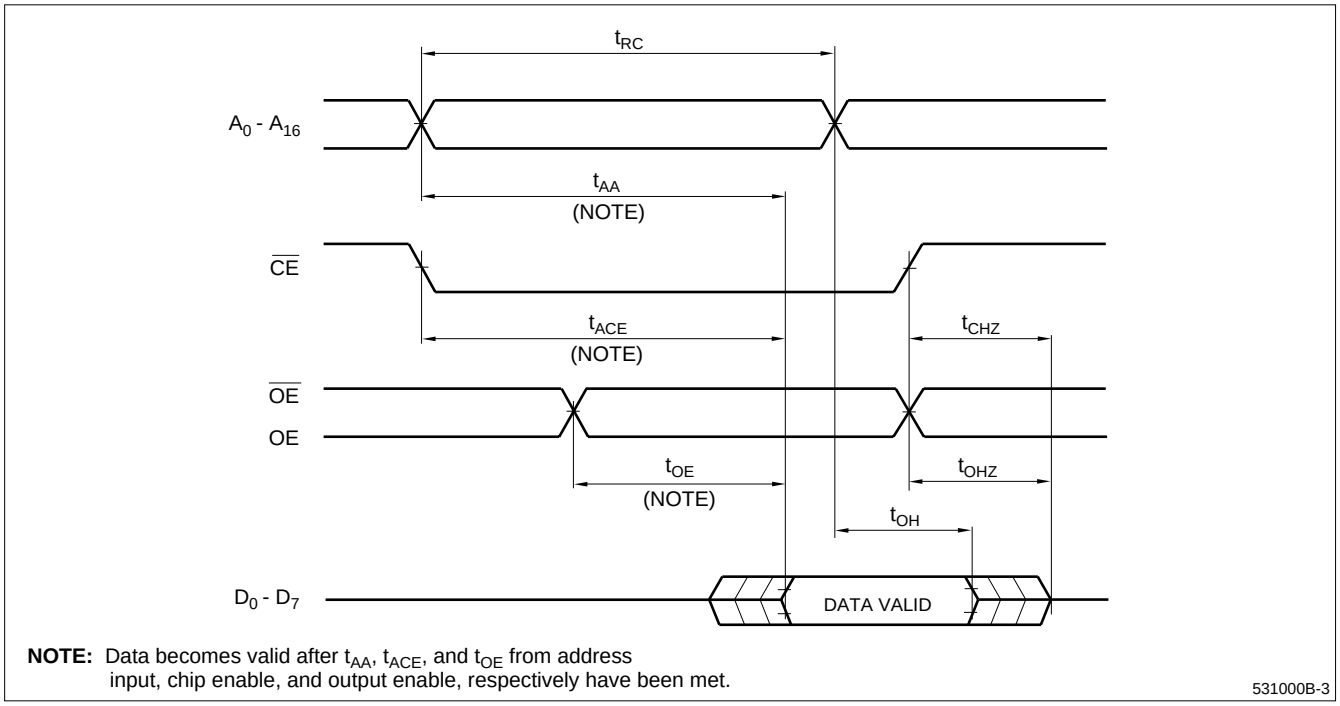
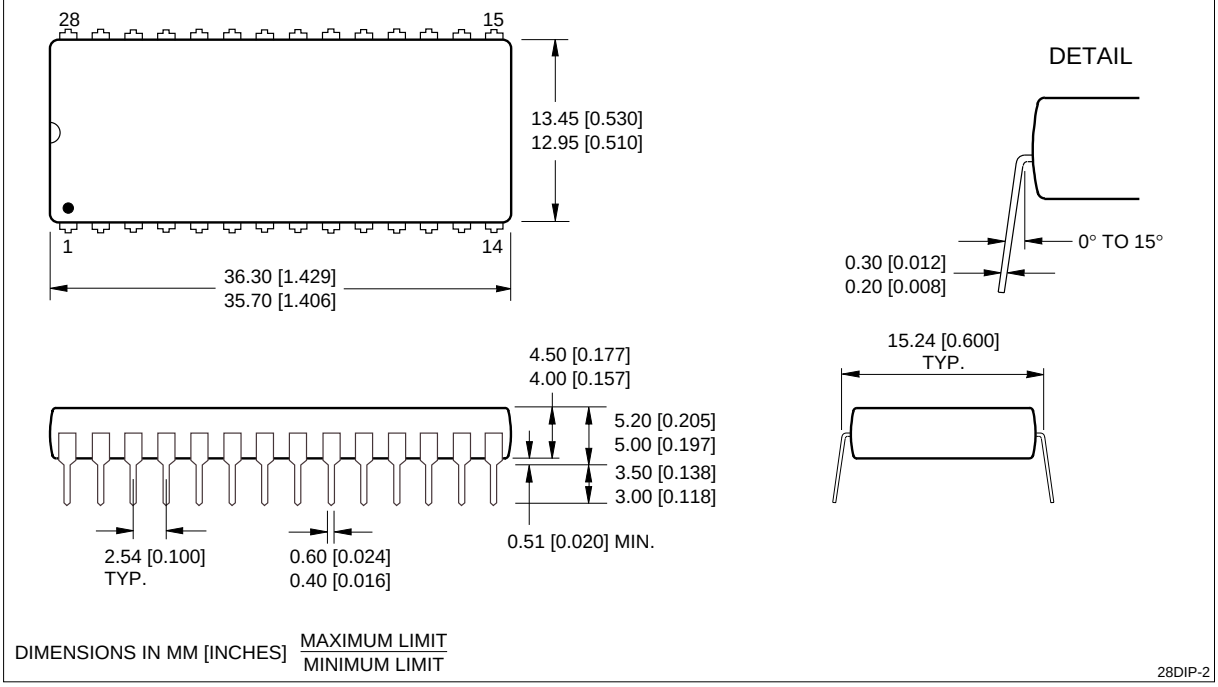


Figure 3. Timing Diagram

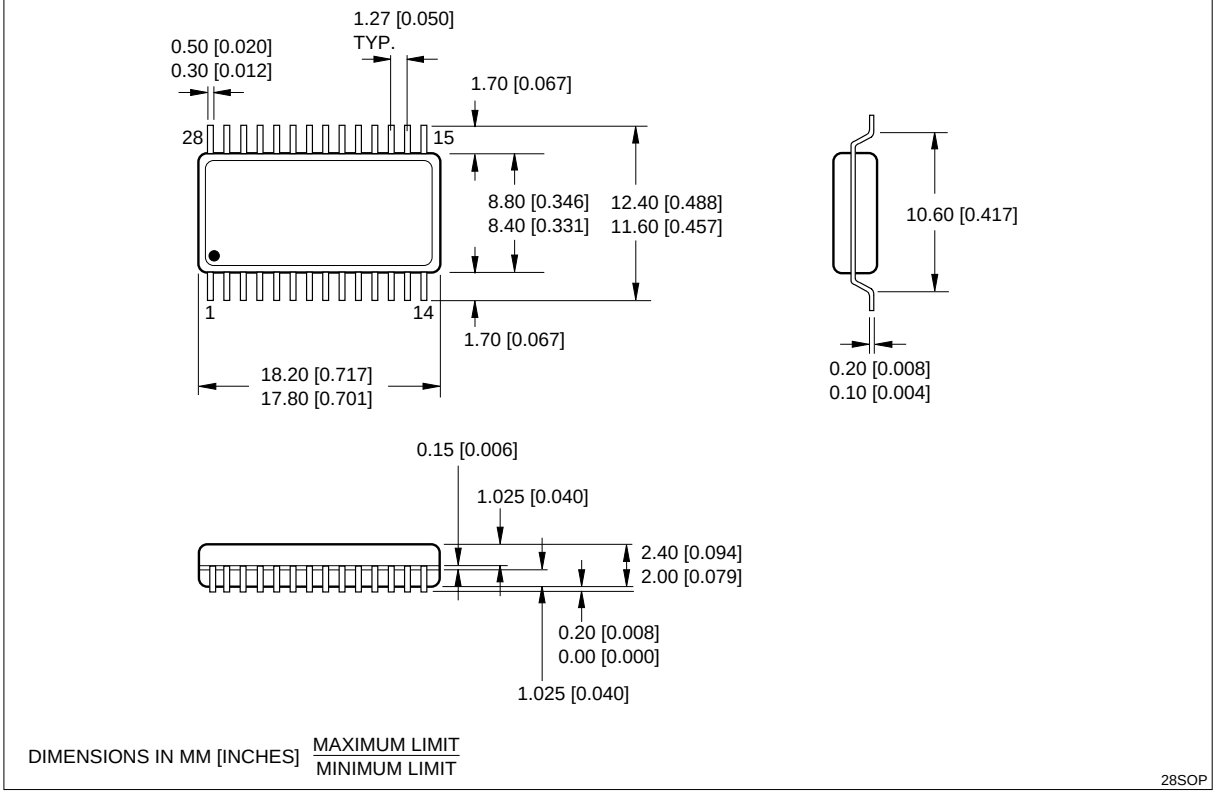
PACKAGE DIAGRAMS

28DIP (DIP028-P-0600)



28-pin, 600-mil DIP

28SOP (SOP028-P-0450)



28-pin, 450-mil SOP

ORDERING INFORMATION