FAN8741/FAN8742

Spindle motor and 6-CH actuator driver [Spindle(PWM), Sled 2-CH(PWM) 4-CH(Linear)]

FAN8741 Features

Common

- Built-in thermal shutdown circuit (TSD)
- 8 Independent voltage sources
- Corresponds to 3.3V or 5V DSP
- 4 selectable mute

Spindle

- Output PWM mode control
- FG output: open collector type
- Selectable brake(short & reverse brake)
- Built in hall bias
- 180^{o} commutation(compatible with conventional BLDC spindle motor)
- Built in arm short preventer

BTL(Sled 2-channels)

- Output PWM mode control
- Built in arm short preventer

BTL(Other 4-channels)

- Output LINEAR mode control

Typical Applications

- Compact disk ROM (CD-ROM)
- Compact disk RW (CD-RW)
- Digital video disk ROM (DVD-ROM)
- Digital video disk RAM (DVD-RAM)
- Digital video disk Player (DVDP)
- Other compact disk media
- Game console

Description

The FAN8741G/FAN8742G is a monolithic IC suitable for a 3-phase BLDC(Brush Less Direct Current) spindle motor driver with PWM, 2-ch motor drivers with PWM for sled motor and 4-ch linear drivers which drive the focus actuator, tracking actuator, tilt actuator and loading motor of the optical media applications. Since FAN8741G/FAN8742G aims to high-speed/high-density optical media applications its power stage is made by D-MOS transistors which have extremely low RDS on. This enables less heat generation and guarantees more reliable lifetime.

56-SSOP

Ordering Information

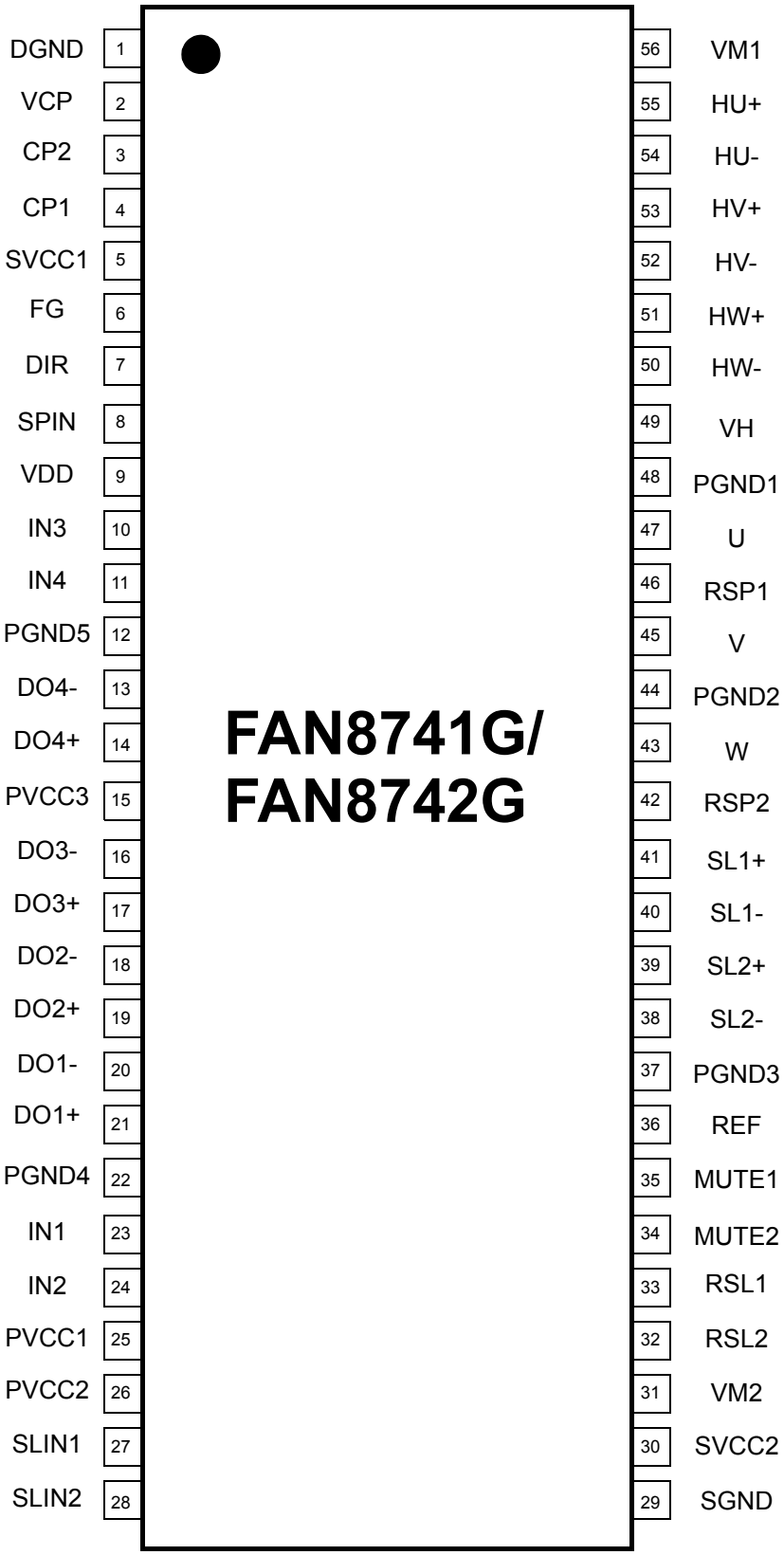
Device	Package	Operating Temp.
FAN8741G	56-SSOP	–25°C ~ +75°C
FAN8741GX	56-SSOP	–25°C ~ +75°C
FAN8742G	56-SSOP	–25°C ~ +75°C
FAN8742GX	56-SSOP	–25°C ~ +75°C

X:Tape & Reel type

FAN8741G:FG3X

FAN8742G:FG1X

Pin Assignments



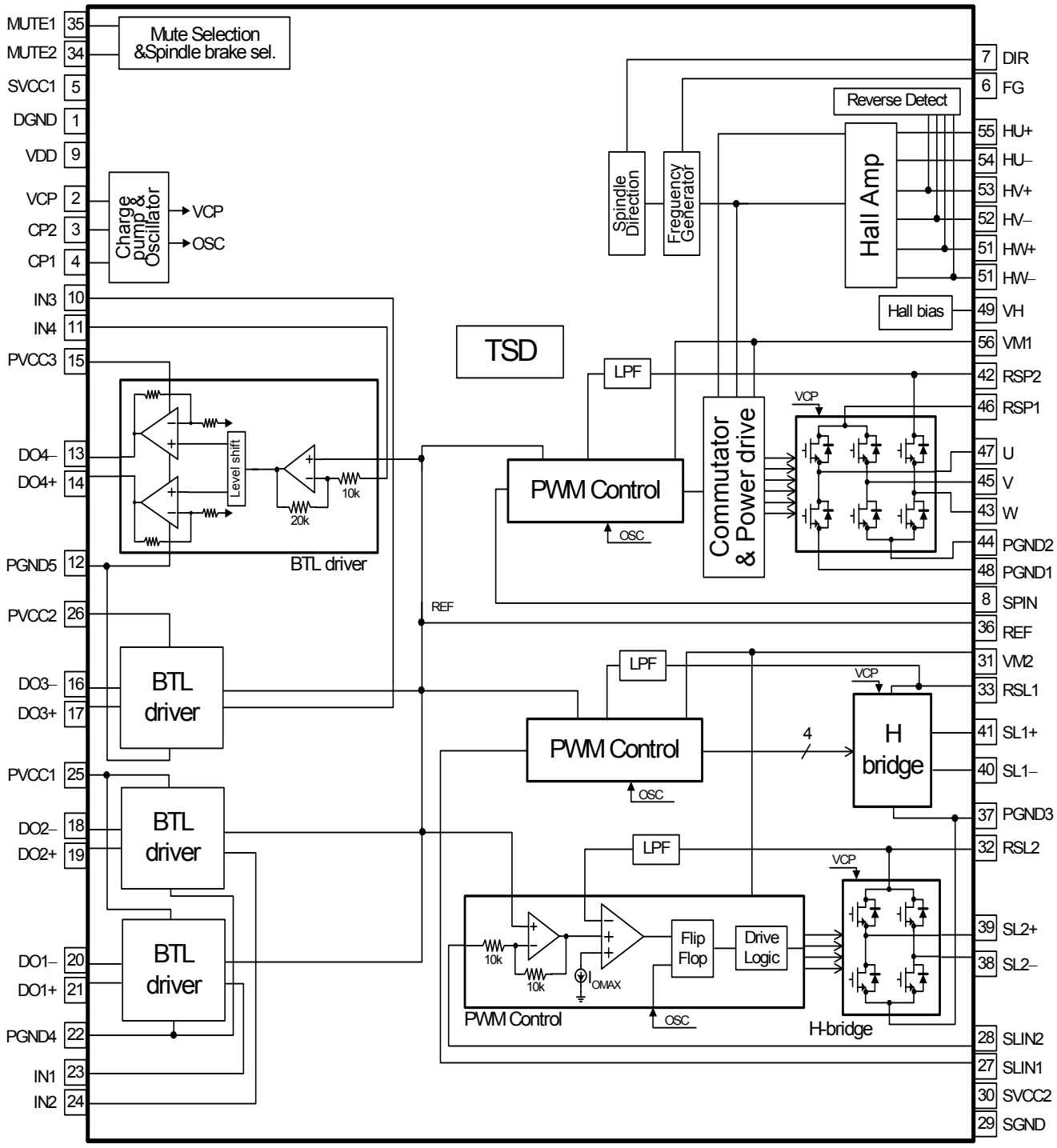
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	DGND	P	Ground for digital block
2	VCP	A	Charge pumped voltage
3	CP2	A	Charge pump capacitor2
4	CP1	A	Charge pump capacitor1
5	SVCC1	P	Power supply for signal block
6	FG	O	Spindle frequency generator (FAN8741G:3X, FAN8742G:1X)
7	DIR	O	Spindle rotational direction output
8	SPIN	A	Spindle channel input
9	VDD	P	Power supply for digital block
10	IN3	A	Channel 3 input
11	IN4	A	Channel 4 input
12	PGND5	P	Power ground for BTL CH3/4
13	DO4 -	A	Channel 4 drive output -
14	DO4 +	A	Channel 4 drive output +
15	PVCC3	P	Power supply for BTL CH4
16	DO3 -	A	Channel 3 drive output -
17	DO3 +	A	Channel 3 drive output +
18	DO2 -	A	Channel 2 drive output -
19	DO2 +	A	Channel 2 drive output +
20	DO1 -	A	Channel 1 drive output -
21	DO1 +	A	Channel 1 drive output +
22	PGND4	P	Power ground for BTL CH1/2
23	IN1	A	Channel 1 input
24	IN2	A	Channel 2 input
25	PVCC1	P	Power supply for BTL CH1/2
26	PVCC2	P	Power supply for BTL CH3
27	SLIN1	A	Sled channel 1 input
28	SLIN2	A	Sled channel 2 input

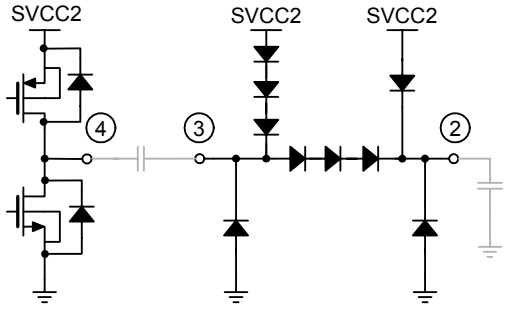
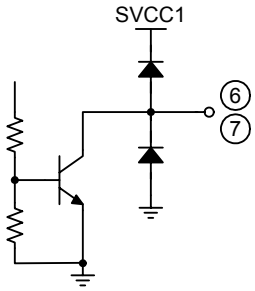
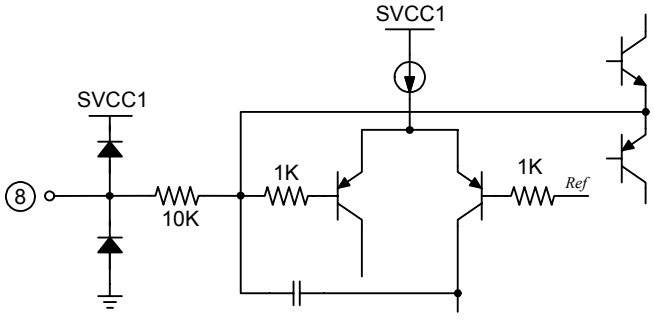
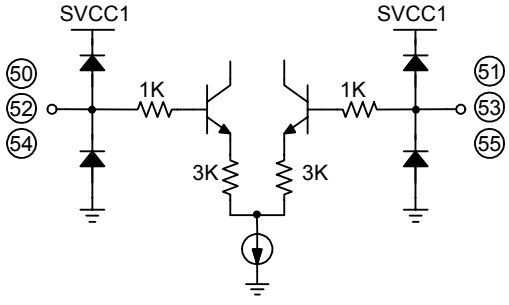
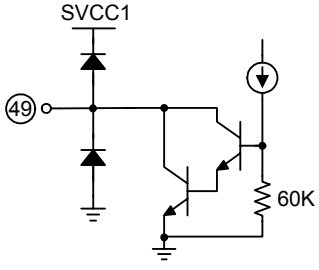
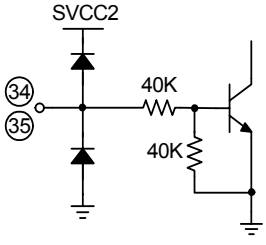
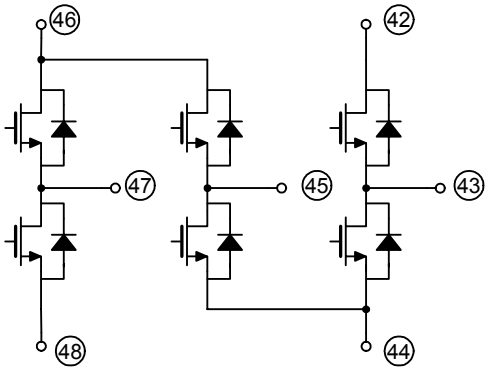
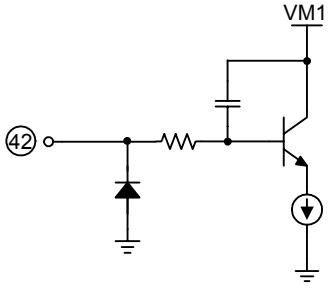
Pin Definitions(continued)

Pin Number	Pin Name	I/O	Pin Function Description
29	SGND	P	Signal ground for BTL signal block
30	SVCC2	P	Power supply for BTL Pre driver
31	VM2	P	Power supply for sled
32	RSL2	A	Sled current sensing 2
33	RSL1	A	Sled current sensing 1
34	MUTE2	A	Mute input 2
35	MUTE1	A	Mute input 1
36	REF	A	Reference voltage input
37	PGND3	P	Power ground for sled channels
38	SL2-	A	Sled channel 2 drive output -
39	SL2+	A	Sled channel 2 drive output +
40	SL1-	A	Sled channel 1 drive output -
41	SL1+	A	Sled channel 1 drive output +
42	RSP2	A	Spindle current sensing 2
43	W	A	3-phase output W for spindle
44	PGND2	P	Power ground 2 for spindle channel
45	V	A	3-phase output V for spindle
46	RSP1	A	Spindle current sensing 1
47	U	A	3-phase output U for spindle
48	PGND1	P	Power ground 1 for spindle channel
49	VH	A	Hall bias
50	HW-	A	Hall signal input(Hw-)
51	HW+	A	Hall signal input(Hw+)
52	HV-	A	Hall signal input(Hv-)
53	HV+	A	Hall signal input(Hv+)
54	HU-	A	Hall signal input(Hu-)
55	HU+	A	Hall signal input(Hu+)
56	VM1	P	Power supply for spindle

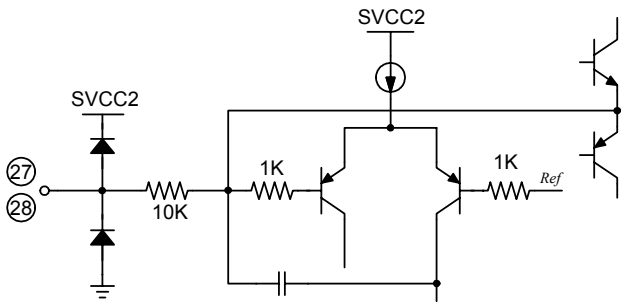
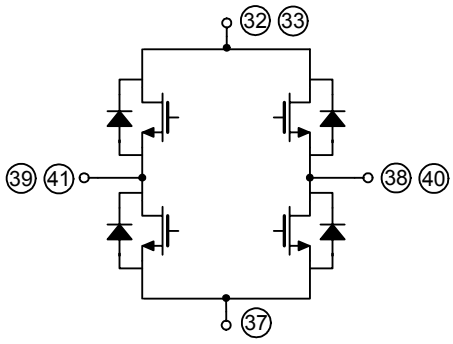
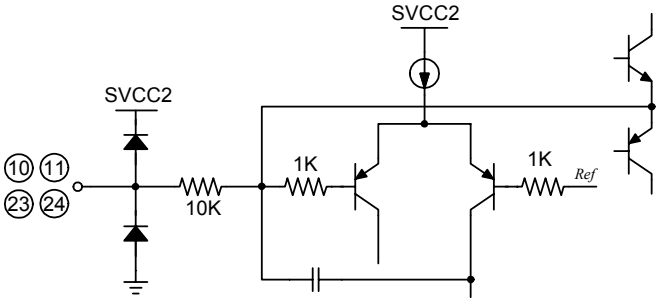
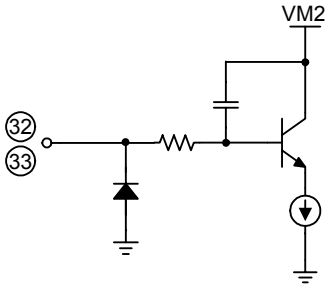
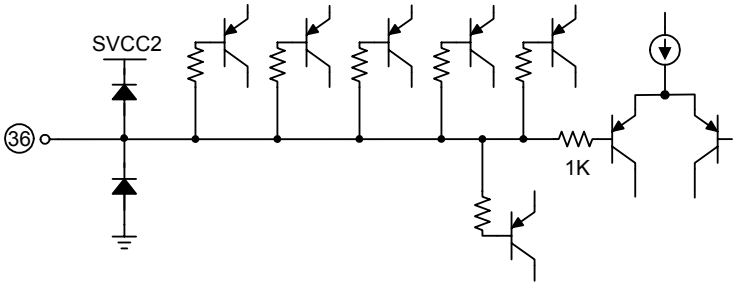
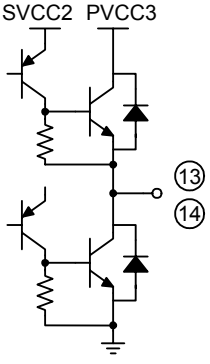
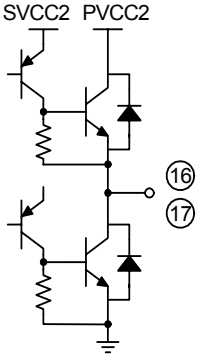
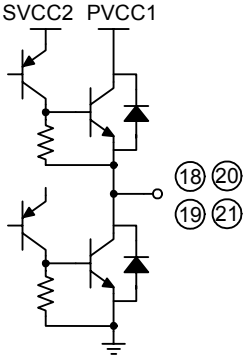
Internal Block Diagram



Equivalent Circuits

Charge Pump Outputs	FG/DIR Outputs
	
Spin Input	**Hall Inputs**
	
Hall Bias Input	**Mute1 & 2 Inputs**
	
Spindle Drive Outputs	**Spindle Current Sensing Input**
	

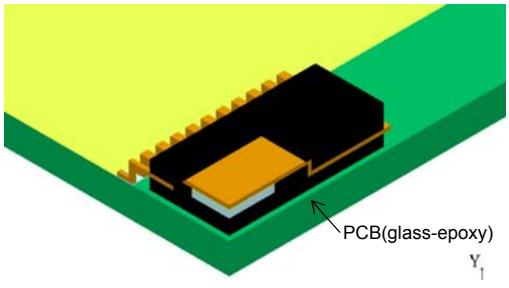
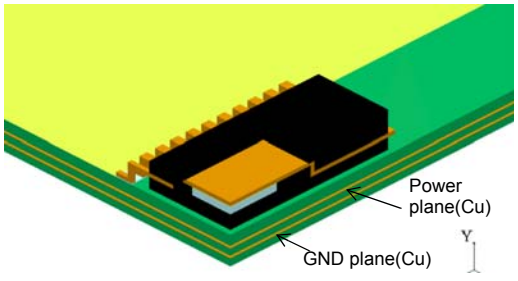
Equivalent Circuits(continued)

Sled 1 & 2 Inputs	Sled Drive Outputs
	
CH1/2/3/4(BTL Channels) Inputs	**Sled 1 & 2 Current Sensing Inputs**
	
Reference Input	**CH4 Outputs**
	
CH3 Outputs	**CH1 & 2 Outputs**
	

Absolute Maximum Ratings (Ta = 25°C)

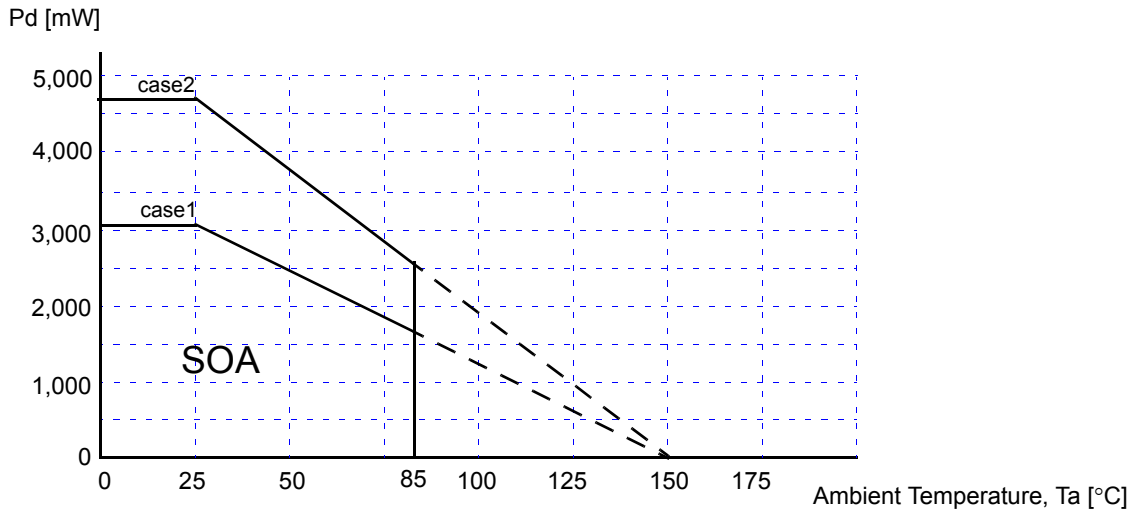
Parameter	Symbol	Value	Unit
Supply Voltage (Signal block)	SV_{CC1max}	7	V
Supply Voltage (Digital block)	V_{DDmax}	7	V
Supply Voltage (Spindle driver)	VM_{1max}	15	V
Supply Voltage (Sled driver)	VM_{2max}	15	V
Supply Voltage (BTL driver)	$PV_{CC1,2,3max}$	15	V
Supply Voltage (BTL Pre driver)	SV_{CC2max}	15	V
Power dissipation	P_D	3.1/4.7	W
Operating Temperature Range	T_{OPR}	-20 ~ +75	°C
Storage temperature Range	T_{STG}	-40 ~ +150	°C
Maximum Output Current (Spindle)	I_{Omax1}	2.0	A
Maximum Output Current(CH1/2/3/4)	I_{Omax2}	1.0	A
Maximum Output Current (Sled)	I_{Omax3}	1.0	A

NOTE:

Case 1	Case 2	Remark
		Pd is measured base on the JEDEC/STD(JESD 51-2)
Pd=3.1W	Pd=4.7W	

1. Case 1: Single layer PCB with 1 signal plane only, PCB size is 76mm × 114mm × 1.6mm.
2. Case 2: Multi layer PCB with 1 signal, 1 power and 1 ground planes, PCB size is 76mm × 114mm × 1.6mm, Cu plane sizes for power and ground is 74mm × 62mm × 0.035mm.
3. These are simulation datum.
4. Power dissipation is reduced by -24.8mW/°C for using above Ta=25°C in case 1.
5. Power dissipation is reduced by -37.6mW/°C for using above Ta=25°C in case 2.
6. Do not exceed P_D and SOA (Safe Operating Area).

Power Dissipation Curve



Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (Spindle Signal block)	SV_{CC1}	4.5	5	5.5	V
Supply Voltage (Digital block)	V_{DD}	4.5	5	5.5	V
Supply Voltage (Spindle driver)	VM_1	4.5	12	13.2	V
Supply Voltage (Sled driver)	VM_2	4.5	12	13.2	V
Supply Voltage (BTL driver)	$PV_{CC1,2,3}$	4.5	12	SV_{CC2}	V
Supply Voltage (BTL signal block)	SV_{CC2}	4.5	12	13.2	V
Output current(Spindle)	I_{O1}	-	1.0	1.5	A
Output current(Focus, Tracking, Loading)	I_{O2}	-	0.5	0.8	A
Output current(Sled)	I_{O3}	-	0.5	0.8	A

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

(Ta=25ºC, SVCC1=VDD=PVCC1=VM2=5V,VM1=SVCC2=PVCC2=PVCC3=12V unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
COMMON PART						
Quiescent Circuit Current 1	I_{SVCC1}	Mute1=L, Mute2=L	-	1	-	mA
	I_{SVCC2}		-	1	-	
Quiescent Circuit Current 2	I_{SVCC1}	Mute1=L, Mute2=H	-	1.5	-	mA
	I_{SVCC2}		-	9.5	-	
Quiescent Circuit Current 3	I_{SVCC1}	Mute1=H, Mute2=H	-	4	-	mA
	I_{SVCC2}		-	13	-	
Mute Low Voltage	V_{MLOW}	MUTE=variation	-	-	0.8	V
Mute High Voltage	V_{MHIGH}	MUTE=variation	3.0	-	-	V
Mute Input Current	I_{MUTEIN}	MUTE=5V	-	130	-	μA
Charge Pump Voltage 1	V_{PUMP1}	I_{PUMP}=0mA	-	19	-	V
Charge Pump Voltage 2	V_{PUMP2}	I_{PUMP}=-1mA	-	18	-	V
THERMAL SHUTDOWN						
Operating Temperature*	T_{TSD}		-	150	-	C
Hysteresis Temperature*	T_{HYS}		-	25	-	C
SPINDLE DRIVE PART						
Control Input Deadzone11	V_{DZSPF}	SPIN>VREF	20	50	100	mV
Control Input Deadzone12	V_{DZSPR}	SPIN<VREF	-100	-50	-20	mV
Control Voltage Input Range	V_{INSP}		0	-	5	V
Output Gain	G_{MSP}	$G_{MSP}=G_{VO}/RCS_{SP}$, RCS_{SP}=0.33Ω, G_{VO}=1[V/V]	2.55	3.0	3.45	A/V
Output On Resistance(upper)	R_{ONUSP}	Io=500mA	-	0.4	-	Ω
Output On Resistance(lower)	R_{ONLSP}	Io=500mA	-	0.4	-	Ω
Output Limit Current	$I_{LIMITSP}$	RCS_{SP}=0.33Ω	-	1.5	-	A
Hall Amp Common Mode Input Range	VH_{COM}	-	1	-	4	V
Minimum Hall Input Level*	V_{HMIN}	-	50	-	-	mV
Hall Bias Output Voltage	V_{HB}	I_{HB}=10mA	0.5	1.0	1.5	V
Hall Bias Input Current	I_{VH}		-	1	5	μA
FG Low Voltage	V_{FGL}	I_{FG}=3mA	-	-	0.5	V
DIR Low Voltage	V_{DIRL}	I_{DIR}=3mA	-	-	0.5	V
SLED DRIVE PART						
Control Input Deadzone21	V_{DZSLF}	SLIN1/SLIN2 > VREF	0	15	30	mV
Control Input Deadzone22	V_{DZSLR}	SLIN1/SLIN2 < VREF	-30	-15	0	mV
Output Gain	G_{MSL}	$G_{MSL}=G_{VO}/RCS_{SL}$, RCS_{SL}=1Ω, G_{VO}=1[V/V]	0.85	1.0	1.15	A/V
Output On Resistance(upper)	R_{ONUSL}	Io=250mA	-	1.0	-	Ω
Output On Resistance(lower)	R_{ONLSL}	Io=250mA	-	1.0	-	Ω
Output Limit Current	$I_{LIMITSL}$	RCS_{SL}=1Ω	-	0.5	-	A

* : Design guarantee specification

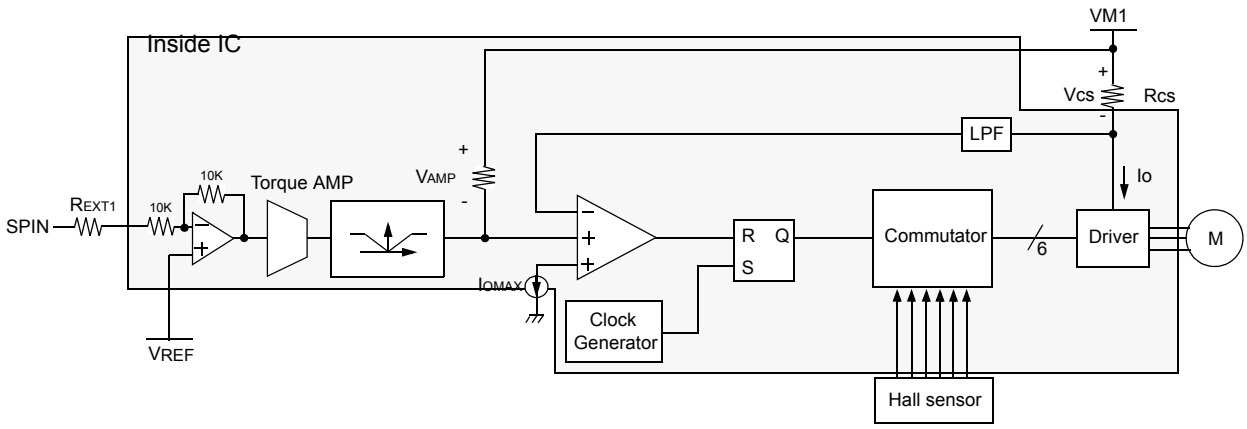
ELECTRICAL CHARACTERISTICS (Ta = 25°C, continued)

(Ta=25ºC, SVCC1=VDD=PVCC1=VM2=5V,VM1=SVCC2=PVCC2=PVCC3=12V unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
CH1,CH2 DRIVE PART (TYPICALLY ACTUATOR DRIVER)						
Output Saturation Voltage H	V_{OHFT12}	I_O=500mA		0.5		V
Output Saturation Voltage L	V_{OLFT12}	I_O=500mA		0.5		V
Closed Loop Voltage Gain	G_{VFT12}	-	16.5	18	19.5	dB
Output Offset Voltage	V_{OFFT12}	VREF=IN1=IN2=1.65V	-50	-	50	mV
CH3,CH4 DRIVE PART (TYPICALLY TILT,LOADING DRIVER)						
Output Saturation Voltage H	V_{OHFT34}	I_O=500mA		1.0		V
Output Saturation Voltage L	V_{OLFT34}	I_O=500mA		0.5		V
Closed Loop Voltage Gain	G_{VFT34}	-	16.5	18	19.5	dB
Output Offset Voltage	V_{OFFT34}	VREF=IN3=IN4=1.65V	-50	-	50	mV
CH1,CH3 GAIN DIFFERENCE SPEC (TYPICALLY FOCUS,TILT DRIVER)						
CH1-CH3 Gain Difference	G_{1TO3}	G_{VFT12} - G_{VFT34}	-0.5	0	0.5	dB

Application Information

1. TORQUE CONTROL & OUTPUT CURRENT CONTROL OF 3-PHASE BLDC MOTOR

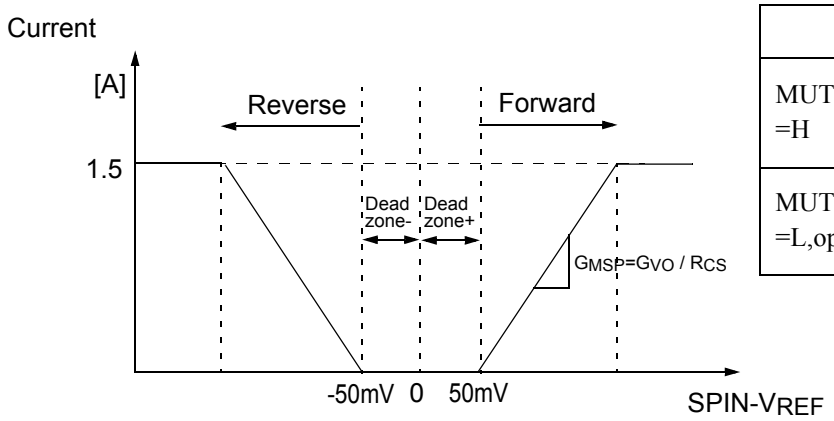


1) By amplifying the voltage difference between V_{REF} and SPIN from Servo IC(or DSP), the Torque AMP produces the input voltage(V_{AMP}) which means input current command.
2) The output current (I_O) is converted into the voltage (V_{CS}) through the sense resistor (R_{CS}) and compared with the V_{AMP}.
3) The clock generator always make the RS latch become set periodically, this enables output driver on state and when the V_{CS} and the V_{AMP} is equal the state becomes off.
4) By the negative feedback loop, the sensed output voltage V_{CS} equals to the V_{AMP}.
5) Commuting sequence is selected by hall sensor input, and the minimum hall input is 50mV.
6) The gain and limit current is calculated as below table.($Gvo=V_{AMP}/(SPIN-V_{REF})=1[V/V]$).

Limit current	Input/Output gain[A/V]	Remark
$\frac{0.5}{Rcs}$	$\frac{10K}{R_{EXT1}+10K} \bullet \frac{G_{VO}}{R_{CS}}$	$\frac{10K}{R_{EXT1}+10K}$ is gain scaler

7) Spindle block adopts 180^o commutation methodology which is full compatible with conventional BLDC spindle motor. Users don't need to change or modify their spindle motor.

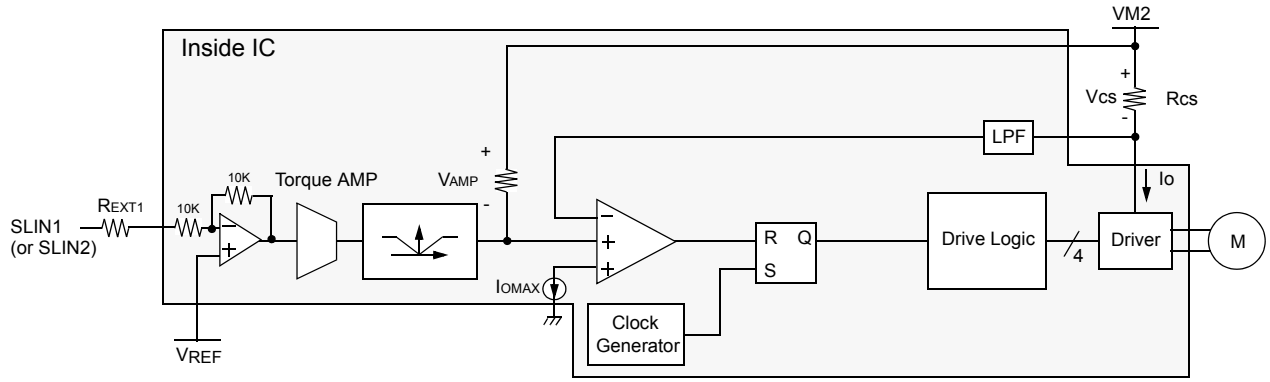
8) The range of the input voltage is as shown below when Rcs=0.33Ω, R_{EXT1}=0.



		Rotation
MUTE2 =H	SPIN > V_{REF}	Forward rotation
	SPIN < V_{REF}	Reverse brake
MUTE2 =L,open	SPIN ≠ V_{REF}	Short brake
		Short brake

The input range of SPIN is 0 V ~ 5 V

2. TORQUE CONTROL & OUTPUT CURRENT CONTROL OF SLED MOTOR(2-PHASE STEP MOTOR)



1) By amplifying the voltage difference between V_{REF} and SLIN1(or SLIN2) from Servo IC(or DSP), the Torque AMP produces the input voltage(V_{AMP}) which means input current command.

2) The output current (I_O) is converted into the voltage (V_{CS}) through the sense resistor (R_{CS}) and compared with the V_{AMP}.

3) The clock generator always make the RS latch become set periodically, this enables output driver on state and when the V_{CS} and the V_{AMP} is equal the state becomes off.

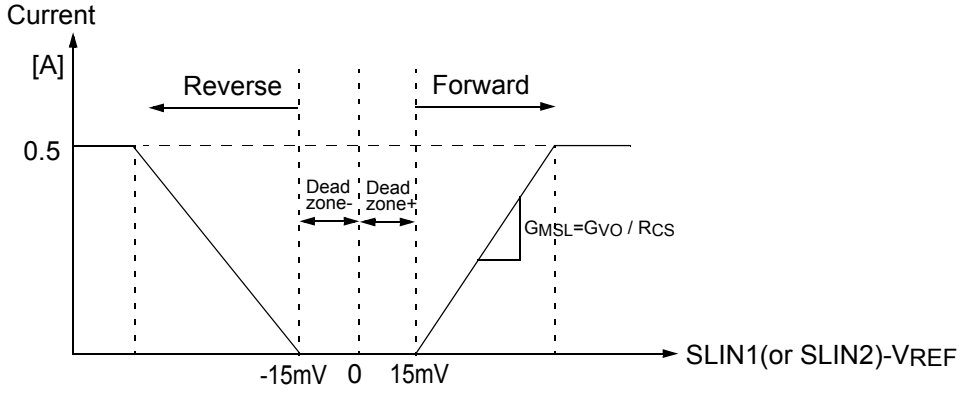
4) By the negative feedback loop, the sensed output voltage V_{CS} equals to the V_{AMP}.

5) To avoid output upper and lower transistor's short through, switch trick is needed. Turn on delay time is 1usec, so the phase delay time,when change the current direction is 1usec.

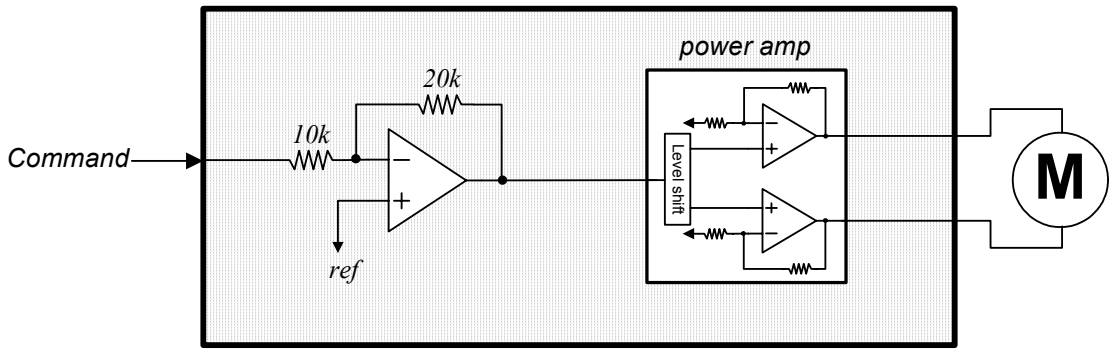
6) The gain and limit current is calculated as below table.($G_{VO}=V_{AMP}/[SLIN1(or\ SLIN2)-V_{REF}]=1[V/V]$

Torque limit current	Input/Output gain[A/V]	Remark
$\frac{0.5}{Rcs}$	$\frac{10K}{R_{EXT1}+10K} \bullet \frac{G_{VO}}{R_{CS}}$	$\frac{10K}{R_{EXT1}+10K}$ is gain scaler

8) The range of the torque voltage is as shown below when Rcs=1Ω, R_{EXT1}=0.



3. CHANNEL 1~4 SCHEMATIC



- The reference voltage(ref) is given externally through pin36.
- The input OP-amp output signal is amplified by (20K/10K) times and then fed to the power amplifier. The gain of power amplifier is 4 so the total max gain of channel 1~4 is 8.

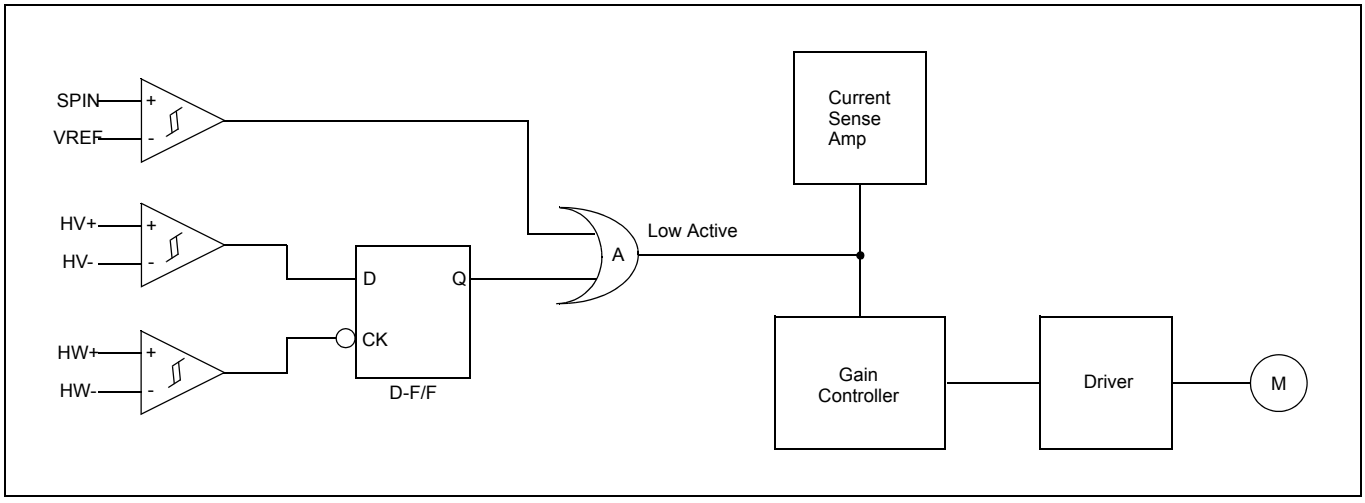
4. MUTE INPUTS

FAN8741 has 2 independent mute pins those are, pin #14(MUTE1) and pin #13(MUTE2). Detailed logics are as below.

MUTE1	MUTE2	SPINDLE	SLED	CH1/2/3	CH4(typ. loading driver)	SPINDLE brake type
H	H	Enable			Disable	Reverse brake when SPIN<VREF
H	L	Enable			Disable	Short brake SPIN ≠ VREF(note)
L	H	Disable	Enable	Disable	Enable	-
L	L	Disable				-

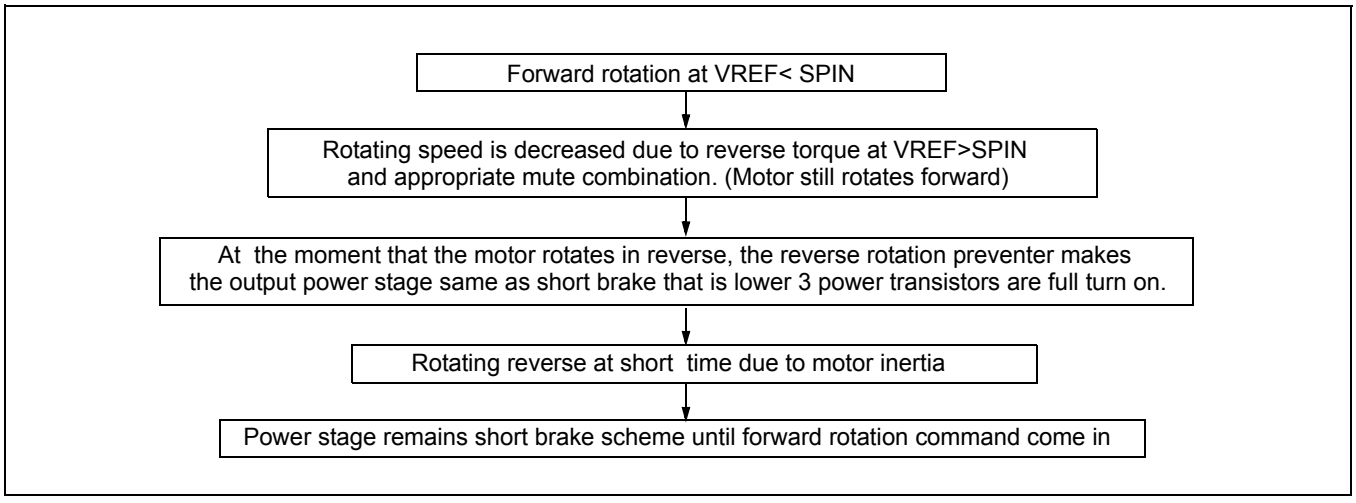
(Note)
To make spindle short brake, MUTE2 goes low and spindle command must not be in deadzone(±50mV). When the spindle command is within deadzone, spindle block goes to disable mode even though MUTE2 is low.

5. REVERSE ROTATION PREVENTION(SPINDLE)

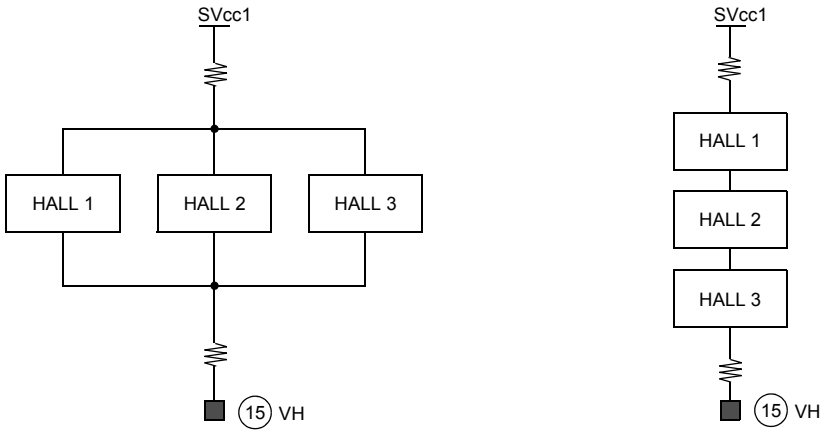


1) As in the state of the forward rotation, the D-F/F output, Q is HIGH and the motor rotates normally. At this state, if the control input is changed such that VREF>SPIN, then the motor rotates slowly by the reverse commutation in the Driver. When the motor rotates in reverse direction, the D-F/F output becomes Low and the OR Gate output, becomes LOW. This prevents the motor from rotating in reverse direction. The operation principle is shown in the table and the flow chart.

Rotation	HV	HW	D-F/F (Q)	Reverse Rotation Preventer	
				V_{REF}<SPIN	V_{REF}>SPIN
Forward	H	H→L	H	Forward	-
Reverse	L	H→L	L	-	Brake and Stop



6. HALL SENSOR CONNECTION



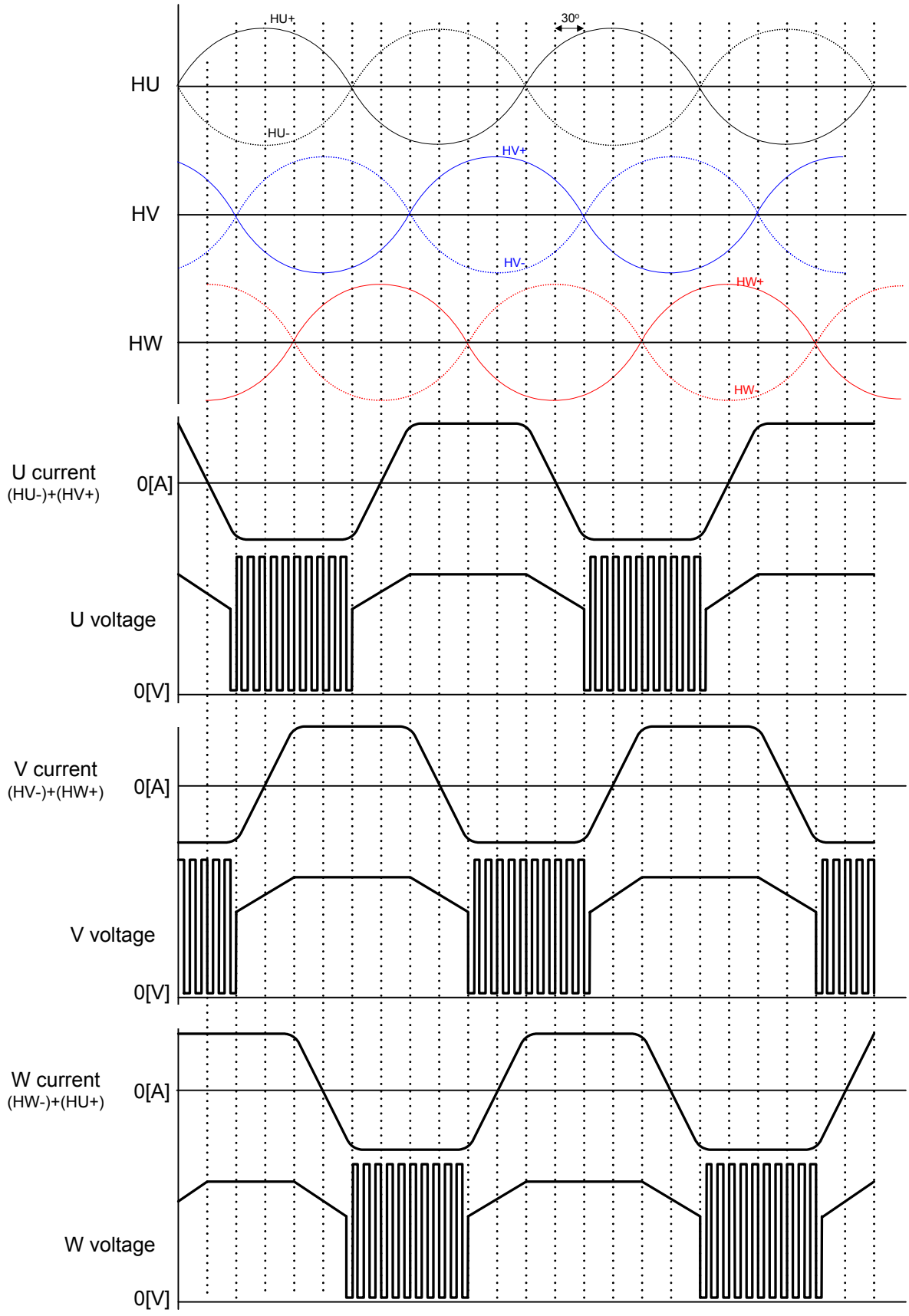
7. PWM FREQUENCY

PWM operation of spindle and sled channels are controlled by internal clock generator. Its typical frequency is 100KHz.

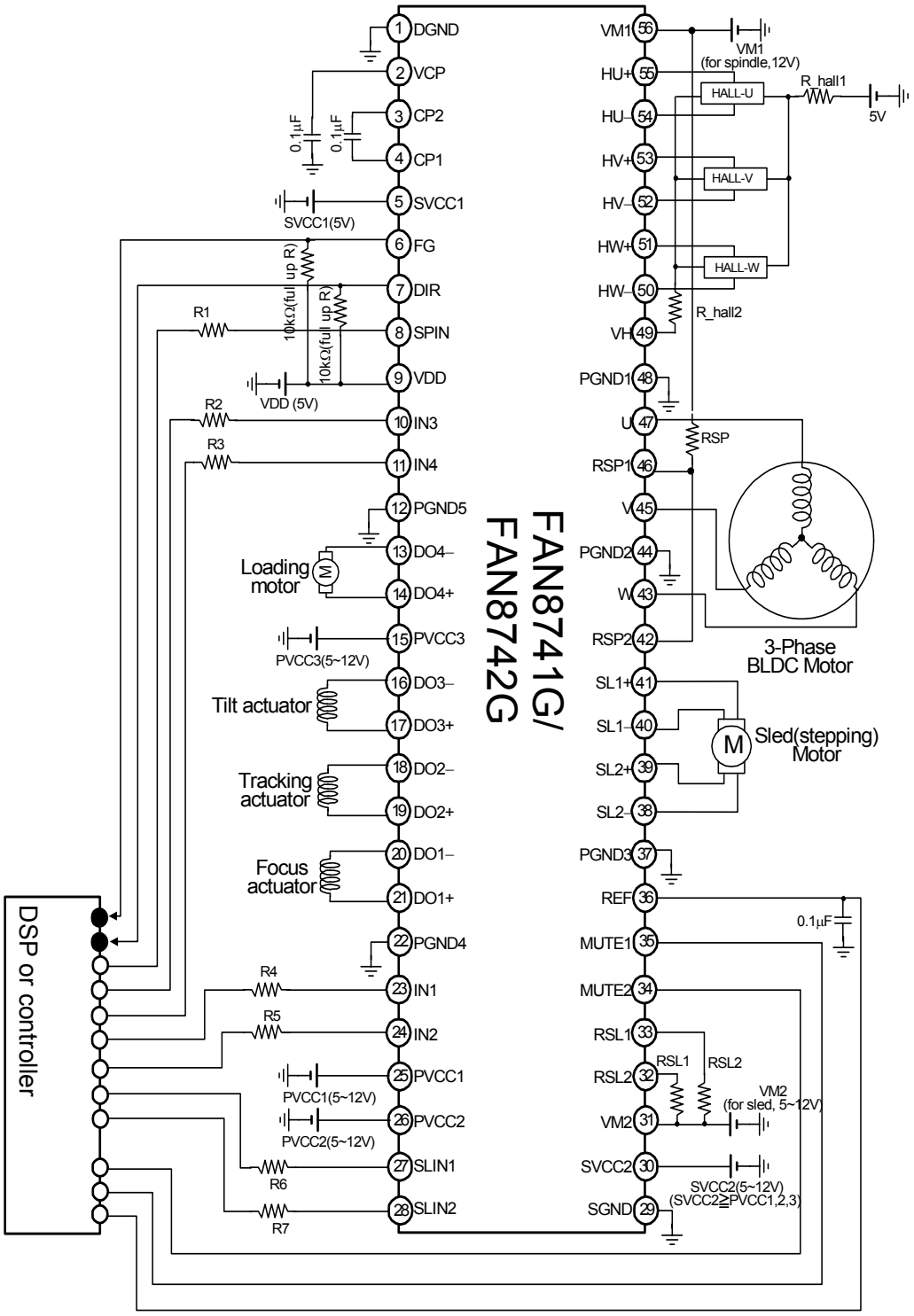
8. ETC

1) FG, DIR output are open-collector type.
2) By-pass capacitors are recommended at hall sensor inputs, power supply inputs.

9. SPINDLE PART INPUT-OUTPUT TIMING CHART

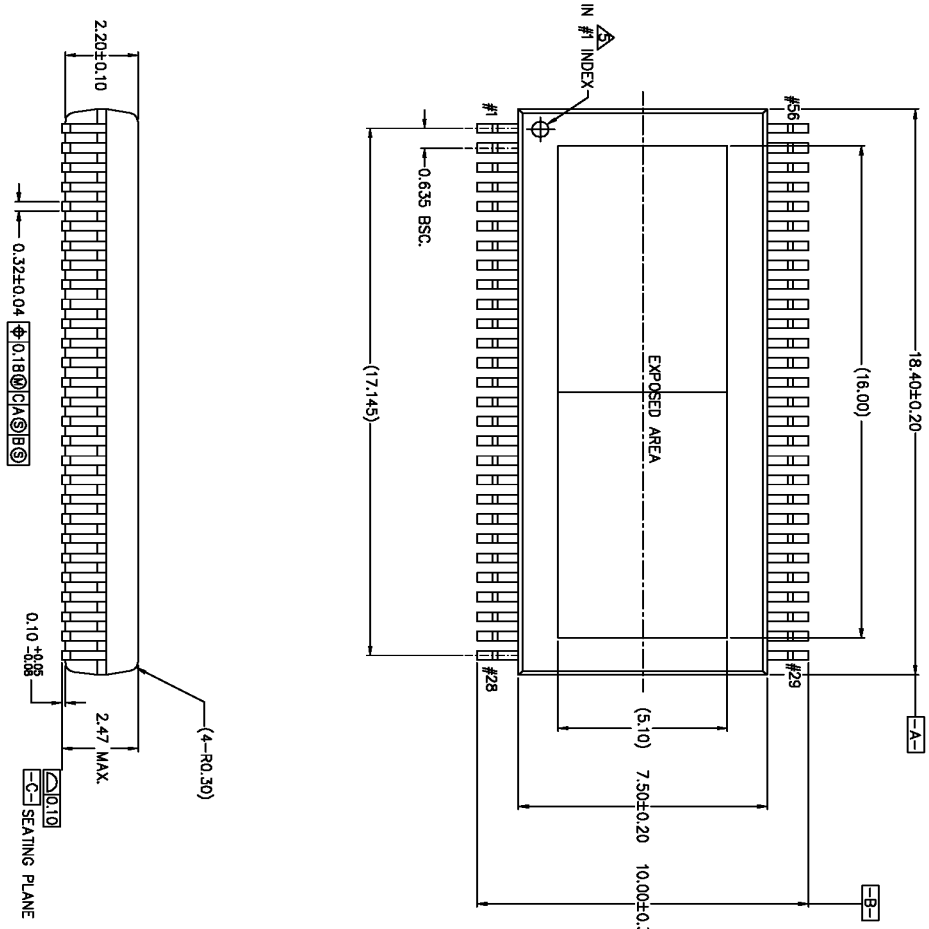


Typical Application Circuits



Component	Reference value	Remark
R1~R7	10kΩ	Gain scaling resistors. Please refer to 12,13,14 pages.
R_hall1,R_hall2	100Ω	Hall bias resistors
RSL1,RSL2	1Ω	Rcs at sled driver. (I_limit=0.5A,Gain=0.5A/V@R6,R7 are 10kΩ)
RSP	0.33Ω	Rcs at spindle driver. (I_limit=1.5A,Gain=1.5A/V@R1 is 10kΩ)
Bypass electrolytic capacitors(47~100μF) are recommended at power supply inputs.		

Package Dimension(exposed area is exposed to the top)



NOTE ;

1. CONTROLLING DIMENSIONS ARE MM.
   ( ) IS REFERENCE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y 14.5M – 1982.
3. "A" AND "B" ARE REFERANCE DATUMS ON THE MOLDED BODY
   AND DO NOT INCLUDE MOLD FLASH/PROTRUSIONS.
   MOLD FLASH/PROTRUSIONS AT "A" SHALL NOT EXCEED 0.152MM(0.00
   PER SIDE.
   INTER-LEAD FLASH/PROTRUSIONS AT "B" SHALL NOT
   0.254MM(0.010") PER SIDE.
4. PIN NUMBERS START WITH PIN #1 AND CONTINUE COUNTERCLOCKWISE
   PIN #56 WHEN VIEWED FROM TOP.

Ⓐ PIN #1 INDEX MUST BE INDENFIED BY LASER MARK.

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