PM3351

ELAN 1X100

ANSWERS TO FREQUENTLY ASKED QUESTIONS REGARDING THE PM3351 ELAN-1X100 DEVICE

ISSUE 1: FEBRUARY 1998

CONTENTS

1 REFERENCES

[1] PCI SIG, “PCI Local Bus Specification,” June 1995, Version 2.1

[2] PCI Industrial Computers Manufacturers Group, “PCI Compact Specification,” 1995, Version 1.0

[3] PMC-Sierra, PMC-970109, “Eight Port Ethernet Switch,” PM3350 Standard Product Datasheet, Issue 1

[4] PMC-Sierra, PMC-970113, “Single Port Fast Ethernet Switch,” PM3351 Standard Product Datasheet, Issue 1

[5] PMC-Sierra, PMC-970391, “PM3350 ELAN 8x10 24-port Ethernet Switch Reference Design”, Issue 4

[6] PMC-Sierra, PMC-970390, “PM3351 ELAN 1x100 2-port Ethernet Switch Reference Design”, Issue 4

2 GLOSSARY OF TERMS

BGA	Ball Grid Array. This term refers to a type of pack for ICs. The package is electrically connected to the circuit board via conductive balls arranged in a grid pattern on the underside of the package. The PM3350 device is packaged in a 256 pin Super BGA. The PM3351 device is packaged in a 208 pin PQFP (Plastic Quad Flat Pack).
Back Pressure Flow Control	A flow control algorithm for half-duplex ports of an Ethernet Switch. Backpressure is activated to slow a sending device and ensure no packets are lost. It implements this by sending a JAM sequence (including an appropriate inter-frame gap) to the transmitting port. Once the port is cleared, normal operation is resumed. In full duplex ports, PAUSE frames are used for flow control.
CRC	Cyclic Redundancy Check. This is a method of detecting bit errors by dividing a received bit stream by a binary polynomial and comparing the remainder with a received CRC value.
DRAM	Dynamic RAM
CSMA/CD	Carrier Sense Multiple Access with Collision Detect. CSMA/CD is the protocol used by Ethernet LANs. CSMA/CD uses contention to arbitrate access for multiple devices to a shared medium. In other words, several devices may choose to use the medium at the same time in which case a collision occurs resulting in all the devices waiting a random back off period before retransmitting.
DMA	Direct Memory Access
ELAN	Ethernet Local Area Network. This is PMC-Sierra's mnemonic for its family of current generation Ethernet products.
Head of Line Blocking	This occurs when a packet at the head of the FIFO has a destination port that is occupied or busy, and the next packet in the queue has a destination port which is available. This next packet cannot go through the FIFO since it is waiting on the packet in the "head of the line".
IC	Integrated Circuit.

MAU	Media Access Unit
MAC	Media Access Controller.
MIB	Management Information Base
PCI2.1	Peripheral Component Interconnect Bus Specification Version 2.1
PERL	Practical Extraction and Reporting Language
RAM	Random Access Memory.
RISC	Reduced Instruction Set Controller. This term is used generically to refer to microcontrollers which have been optimized for fast execution cycles by reducing the number of possible instructions (thereby decreasing the time to decode the instruction).
RMON	Remote Monitoring
RTOS	Real Time Operating System
SNMP	Simple Network Management Protocol
SRAM	Static RAM.
TCP/IP	Transmission Control Protocol / Internet Protocol.
Uplink	An uplink is a port (or ports) on a switch that has higher capacity than the remaining ports and is dedicated to the purpose of transferring data to a LAN server or printer

3 BACKGROUND AND OVERVIEW

PMC-Sierra's PM3351, ELAN1x100 Single Port Fast Ethernet Switch and PM3350 ELAN-8x10 Eight Port Ethernet Switch are full-featured devices which can be used separately or together to implement highly integrated switched Ethernet networking equipment like desktop and workgroup switches.

In order to help customers quickly find the answers to their questions, the following list of answers to frequently asked questions regarding the PM3351 has been compiled.

A separate list of answers to frequently asked questions is available for the PM3350 device.

In this document, the term “PM3351” will refer to the ELAN-1x100 device.

4 ANSWERS TO FREQUENTLY ASKED QUESTIONS

Q1) Is there a reference design available for the PM3351?

A1) Yes. There is a reference design available for the PM3351.

The PM3351 ELAN 1x100 2-Port Fast Ethernet Switch Reference Design (PMC-970390) shows a 2 port 10/100 Base-T Ethernet switch.

PMC-Sierra Sales Representatives have copies of this document available for distribution. It is suggested that customers periodically query their local PMC-Sierra Sales Representative for the latest documentation for the PM3351.

PMC-Sierra also has a World Wide Web site at **http://www.pmc-sierra.com** from which documentation can be ordered or downloaded. Furthermore, customers can register themselves on the Web site to be notified in the event of changes to the documentation.

Q2) Does the PM3351 require external memory?

A2) The PM3351 requires external memory for packet buffering, data structures, and auxiliary program storage. The PM3351 has a small amount of internal RAM which is used for packet switching firmware.

Q3) What kind and size of memory is recommended for use with the PM3351?

A3) For the PM3351 device, the minimum memory recommended is ½ Mbyte of 15 ns asynch SRAM in a (4 x 128k x 8) configuration.

Additional memory may be desired to support large address tables or packet buffering space. PMC Sierra can assist the customer in selecting the optimum memory configuration.

In addition the master device in the system requires 256K of 150 ns EPROM or EEPROM in a (1 x 256k x 8) configuration.

Q4) How many ports can the ELAN family support in non-blocking configurations?

A4) The ELAN supports a scalable architecture. The following table summarizes the non-blocking configurations.

Table 1 Non-Blocking Configurations

# PM3350 Devices	# PM3351 Devices	Switch Port Configuration
8	0	64x10
7	1	56x10 + 1x10/100
6	1	48x10 + 1x10/100
5	2	40x10 + 2x10/100
4	2	32x10 + 2x10/100
3	2	24x10 + 2x10/100
2	3	16x10 + 3x10/100
1	4	8x10 + 4x10/100
0	4	4x10/100

A switch will be non-blocking as long as the bandwidth required on the switching fabric (in this case the PCI bus) does not exceed the limits (peak and average) of that switching fabric. If the limit is exceeded, blocking/collisions will occur, and packets will be dropped.

In the case of the PM3351, which uses a 32-bit, 33 to 45 MHz PCI bus, it has a peak aggregate bandwidth of 1 Gbit/s and a sustained average bandwidth of 500 Mbit/s.

Q5) What speed of PCI bus does the PM3351 support?

A5) The PM3351 was designed and characterized to operate with a 33 to 45 MHz PCI bus. There are currently no plans for the PM3351 to support the 66 MHz PCI bus.

Q6) Can the PM3351 run without an external microcontroller for control and monitoring?

A6) Yes, the PM3351 is controlled and monitored by PMC-Sierra's proprietary SmartPath™ RISC processor.

This processor is primarily responsible for performing the Ethernet/IEE802.3 packet switching functions. It also manages other functions such backpressure, flow control, address aging, topology changes, spanning tree protocol (IEEE802.1d), and hosting an on chip SNMP agent.

Q7) What functions of the PM3351 are performed in hardware, and which are performed in firmware?

A7) The PM3351 uses an implementation which mixes hardware and firmware functionality for both high performance and flexibility.

In the PM3351, the hardware is responsible for:

- Processing received Ethernet frames and placing them into packet buffers;
- Performing the hash table address lookup;
- Transferring packet buffers to the port for transmission;
- Transferring packets over the PCI bus that are destined for another ELAN device for transmission; and
- Providing a consistent, accurate clock and programmable alarms used for address aging.

In the PM3351, the firmware is responsible for everything else, including:

- Making filtering decisions;
- Making forward versus flood decisions (based on results of address lookup);
- Queuing packets to the appropriate transmit queue;
- Initiating the transmission of a packet in the transmit queue; and
- Maintaining the list of free packet buffers and other data structures.

Q8) What firmware is provided with the PM3351?

A8) Customers using the PM3351 can obtain firmware free of charge. There are two versions of the firmware available: one supporting unmanaged operation, and a second supporting managed operation including SNMP agent, and Universal MIB.

A number of configuration variables can also be set for each specific system including the number of MAC addresses supported, and the number of packet buffers.

The current firmware is compatible with standard SNMP managers such as HP OpenView. PMC-Sierra does not provide a management GUI or management application software.

Q9) Can I customize the firmware for the PM3351's integrated RISC processor for my specific application?

A9) The PM3351 has PMC-Sierra's embedded SmartPath™ RISC processor. Currently no development platform is available for customers, and any custom functionality must be supported by PMC-Sierra.

For information on customizing the firmware, please contact Louis Pengue, Director of Marketing. He can be reached at louis@pmc-sierra.com or 503-520-1800.

Q10) How many MAC addresses can be supported by the PM3351?

A10) The maximum number of MAC addresses that can be supported is 32,768. This is also limited by the amount of memory in the system. Each address supported requires 64 bytes of memory. The number for a specific system is set when the firmware is configured.

Q11) What happens when the PM3351's address learning limit is exceeded?

A11) If the design's learning limit is exceeded, packets will be flooded through the switch. The previously learned addresses will not be flushed until they have aged out.

PM3351's can learn addresses up to a limit determined at firmware configuration.

Q12) What is the difference between "flooding" and "broadcasting"?

A12) PMC-Sierra uses the term "flooding" to refer to packet broadcasts performed because the destination address has not been learned. Flooding and

broadcasting both have the same effect — the same packet is transmitted on all ports.

Q13) Does the PM3351 support address aging?

A13) Yes, the PM3351 fully supports address aging. The maximum age for an address is configurable from 2 to 4000 seconds with the default being 300 seconds. Address aging allows the system to reclaim the resources (hash buckets) used by inactive addresses.

Q14) In a switch supporting SNMP, how do multiple PM3351 devices share memory data structures?

A14) One device acts as the master hosting the SNMP agent. Each slave device keeps track of per port and per MAC statistics. Periodically the slave device updates the master using a chip-to-chip messaging system.

Q15) How should a MIB (Management Information Base) be designed for the PM3351?

A15) A MIB is a collection of information on the managed device. There are three standard MIBs that are supported by the PM3351 (IETF rfc1643, rfc1213, and rfc1493).

Additionally PMC-Sierra is defining a private or enterprise MIB that gives the network manager access to data unique to an ELAN-based switch. For example, ELAN-based switches support backpressure even though backpressure is not standardized. With the enterprise MIB, backpressure may be turned on or off.

Once provided with the MIB definition, a MIB compiler takes the ASN.1 representation of the MIB data and converts it into one or more C-language source files that can be compiled with the management software source code. These source files include access routines to manipulate the MIB data.

Q16) Is a PCI arbiter design available for the PM3351?

A16) Yes. Whenever multiple devices are stacked on a PCI bus, a PCI arbiter is required. This arbiter is implemented external to the PM3351 device. A free description for an 8-device PCI arbiter is available (synthesized from a Verilog implementation) from PMC-Sierra and can be used to program a programmable logic device.

Q17) What temperature range does the PM3351 support?

A17) The PM3351 is classified as a Commercial device (0 C to 70 C). However, the part will operate over a wider temperature range. Please see the data sheet after final characterization for the requirements for extended temperature operation.

Q18) What is the power consumption of PM3351?

A18) The power consumption of the PM3351 will be given in the data sheet after final characterization. The current power estimate is from approximately 1 to 1 ¼ W.

Q19) Must the BIAS5V pin of the PM3351 be connected?

A19) Yes. To avoid damage to the device, the BIAS5V signals must be connected to a voltage that is equal to or higher than the VDD[28:1] power supplies

Q20) How should multiple PM3351 devices be connected to a single PCI bus?

A20) Access to multiple PM3351 devices sharing a PCI bus is system specific. The PM3351 evaluation board and PM3351 reference design show a specific example of an implementation.

The firmware on the master PM3351/PM3351 writes, upon boot-up, to the PCI configuration space register on each of the ELAN devices in the system. As per the PCI Local bus specification, the configuration register write operation makes use of the IDSEL pin on the device, with the IDSEL pin connected to one of the AD bus lines through a 1.0 k-ohm resistor.

The general equation used by firmware for mapping IDSEL to the AD bus is given below:

(1) in a system comprised of a mix of PM3350/PM3351 devices :

(1.a) IDSEL mapping to the PM3350 devices in the system:

- for first PM3350 device: AD[16]
- for second PM3350 device: AD[17]
- for third PM3350 device: AD[18]
- for fourth PM3350 device: AD[19]
- for fifth PM3350 device: AD[20]
- for sixth PM3350 device: AD[21]
- for seventh PM3350 device: AD[22]
- for eighth PM3350 device: AD[23]

(1.b) IDSEL mapping to the PM3351 devices in the system:

- for first PM3351 device: AD[29]
- for second PM3351 device: AD[28]
- for third PM3351 device: AD[27]
- for fourth PM3351 device: AD[26]

(2) in a system comprised solely of PM3351 devices :

- for first PM3351 device: AD[31]
- for second PM3351 device: AD[30]
- for third PM3351 device: AD[29]
- for fourth PM3351 device: AD[28]

Failure to connect the IDSEL of a device to the correct AD bus line will cause the firmware boot sequence to not complete correctly; this will be indicated by the LED pattern output during the boot-up.

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PM-971167 (R1) Issue date: April 1998