HD404019R Series

HITACHI

Rev. 6.0
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Description

The HD404019R series are HMCS400-series CMOS 4-bit single-chip microcomputers. Each device incorporates a ROM, RAM, I/O, serial interface, and two timer/counters, and contains high-voltage I/O pins including high-current output pins to directly drive fluorescent displays.

The HD404019R series includes four chips. The HD404019R and HD40L4019R are Mask ROM versions. The HD4074019 and HD407L4019 are PROM versions. The HD40L4019R and HD407L4019 are low-voltage operation versions.

Features

- 16,384-word × 10-bit ROM
  - — Mask ROM: HD404019R, HD40L4019R
  - — PROM: HD4074019, HD407L4019
- 992-digit × 4-bit RAM
- 58 I/O pins, including 26 high-voltage I/O pins (40 V max.)
- Two timer/counters
  - — 8-bit free-running timer
  - — 8-bit auto-reload timer/counter
- Clock synchronous 8-bit serial interface
- Five interrupt sources
  - — Two by external sources
  - — Two by timer/counters
  - — One by serial interface
- Subroutine stack, up to 16 levels including interrupts
- Minimum instruction execution time: 0.89 µs
- Low-power dissipation modes
  - — Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
  - — Stop: Stops instruction execution and clock oscillation while retaining RAM data

Hitachi semiconductor

- On-chip oscillator
  - — Crystal or ceramic oscillator
  - — External clock
- Packages
  - — 64-pin shrink type plastic DIP
  - — 64-pin flat plastic package
  - — 64-pin shrink type ceramic DIP with window

Ordering Information

Type	Product Name	Model Name	Package
Mask ROM	HD404019R	HD404019RS	DP-64S
		HD404019RH	FP-64A
		HD404019RFS	FP-64B
	HD40L4019R	HD40L4019RS	DP-64S
		HD40L4019RH	FP-64A
ZTAT™	HD4074019	HD4074019S	DP-64S
		HD4074019H	FP-64A
		HD4074019FS	FP-64B
		HD4074019C	DC-64S
	HD407L4019	HD407L4019S	DP-64S
		HD407L4019H	FP-64A

ZTAT™: Zero Turn Around Time. ZTAT is a trademark of Hitachi Ltd.

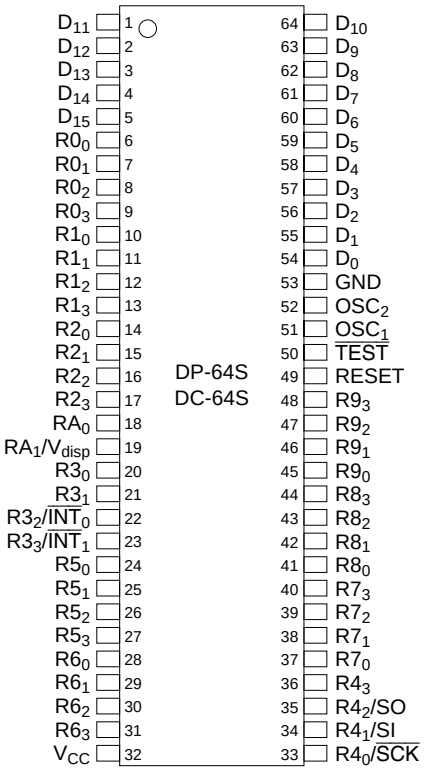
Differences between ZTAT™ and Mask ROM Version

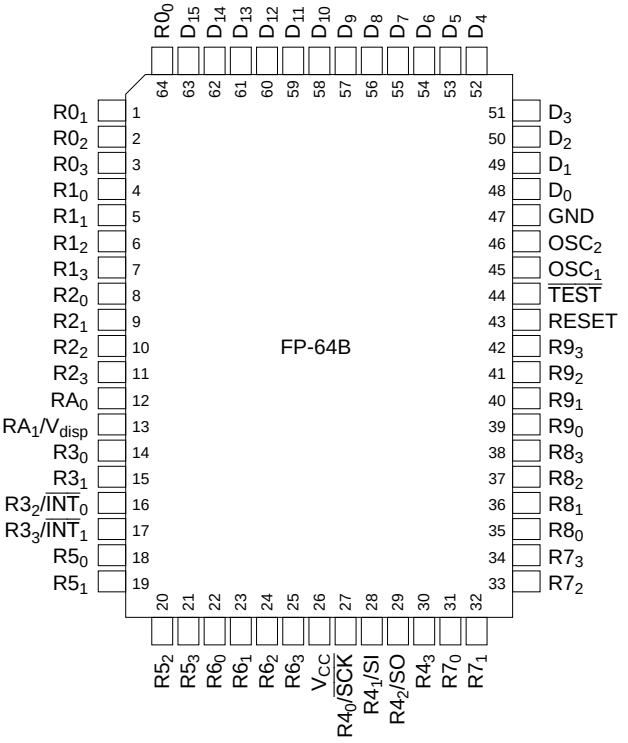
		ZTAT™		Mask ROM Version	
Item		**HD4074019**	**HD407L4019**	**HD404019R**	**HD40L4019R**
Power supply voltage (V)		4.5 to 5.5 V	3.0 to 5.5 V	3.5 to 6.0 V	2.7 to 6.0 V
Instruction cycle time (t_{cyc})		0.89 to 20 µs	1.12 to 20 µs	0.89 to 10 µs	1.12 to 10 µs
ROM (word)		16,384 × 10-bit	16,384 × 10-bit	16,384 × 10-bit	16,384 × 10-bit
RAM		992 × 4-bit	992 × 4-bit	992 × 4-bit	992 × 4-bit
I/O pin circuit*[1]	Standard pins	NMOS open drain	NMOS open drain	Each pin can be without pull-up MOS (NMOS open drain), with pull-up MOS, or CMOS	
	High voltage pins	PMOS open drain	PMOS open drain	Each pin can be without pull-down MOS (PMOS open drain) or with pull-down MOS	
Oscillator stabilization*[2]	Crystal	Available	Available	Available	Available
	Ceramic	Available	Available	Available	Available
Package	DP-64S	Available	Available	Available	Available
	FP-64A	Available	Available	Available	Available
	FP-64B	Available	—	Available	—
	DC-64S	Available	—	—	—

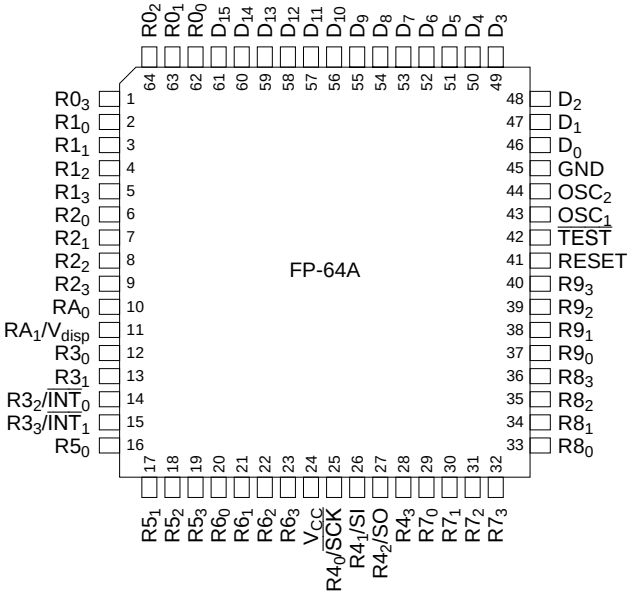
—: Not available

Notes: 1. See table 17.
2. See table 20.

Pin Arrangement

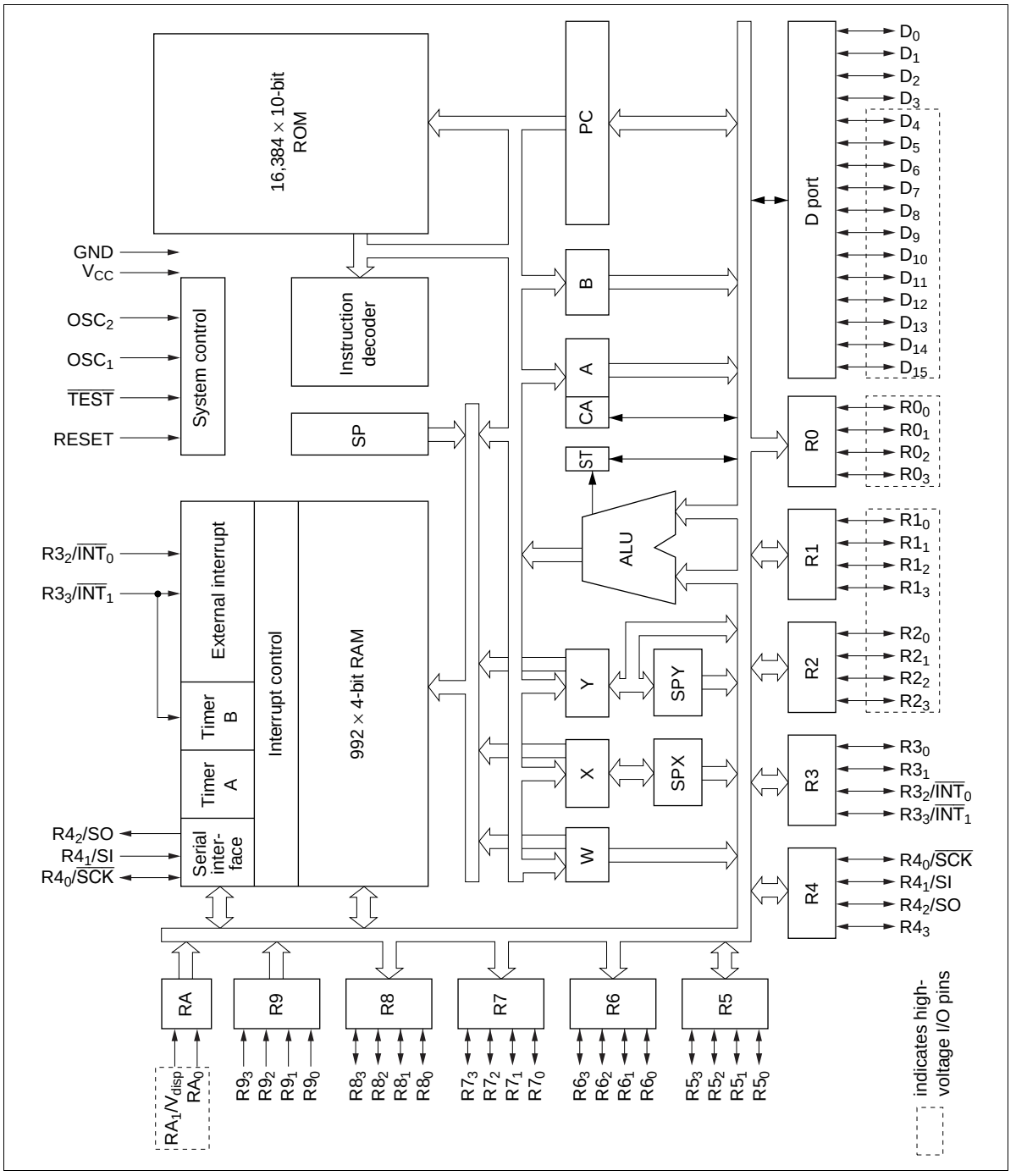






Top view

Block Diagram



Pin Functions

Power Supply

V_{CC}: Apply the power supply voltage to this pin.

GND: Connect to ground.

V_{disp}: Power supply pin (multiplexed with RA_1) for high-voltage I/O pins with a maximum voltage of 40 V (V_{CC} – 40 V). For details, see the Input/Output section.

$\overline{\text{TEST}}$: For test purposes only. Connect it to V_{CC}.

RESET: Resets the MCU. For details, see the Reset section.

Oscillators

OSC_1, OSC_2: OSC_1 and OSC_2 can be connected to a crystal resonator, ceramic resonator or an external oscillator circuit. For details, see the Internal Oscillator Circuit section.

Ports

D_0 to D_{15} (D Port): An input/output port addressed by bits. These 16 pins are all input/output pins. D_0 to D_3 are standard pins and D_4 to D_{15} are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see the Input/Output section.

R0 to RA_1 (R Ports): R0 to R9 are 4-bit I/O ports. Only RA is a 2-bit port. R9 and RA are input ports, and R0 to R8 are I/O ports. R0, R1, R2, and RA are high-voltage ports, and R3 to R9 are standard ports. Each pin has a mask option which selects its circuit type. The pins $R3_2$, $R3_3$, $R4_0$, $R4_1$, and $R4_2$ are multiplexed with $\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$, $\overline{\text{SCK}}$, SI, and SO, respectively. For details, see the Input/Output section.

Interrupts

$\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$: External interrupts for the MCU. $\overline{\text{INT}}_1$ can be used as an external event input pin for timer B. $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ are multiplexed with $R3_2$ and $R3_3$, respectively. For details, see the Interrupt section.

Serial Interface

$\overline{\text{SCK}}$, SI, SO: The transmit clock I/O pin ($\overline{\text{SCK}}$), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. $\overline{\text{SCK}}$, SI, and SO are multiplexed with $R4_0$, $R4_1$, and $R4_2$, respectively. For details, see the Serial Interface section.

Memory Map

ROM Memory Map

The MCU contains a 16,384-word × 10-bit ROM (mask ROM or PROM). It is described in the following paragraphs and by the ROM memory map in figure 1.

Vector Address Area ($0000 to $000F): Locations $0000 through $000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt programs. After reset or an interrupt routine is processed, the program is executed from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F are reserved for subroutines. The CAL instruction branches to subroutines.

Pattern Area ($0000 to $0FFF): Locations $0000 through $0FFF are reserved for ROM data. The P instruction can refer to the ROM data as a pattern.

Program Area ($0000 to $3FFF): Locations from $0000 to $3FFF can be used for program code.

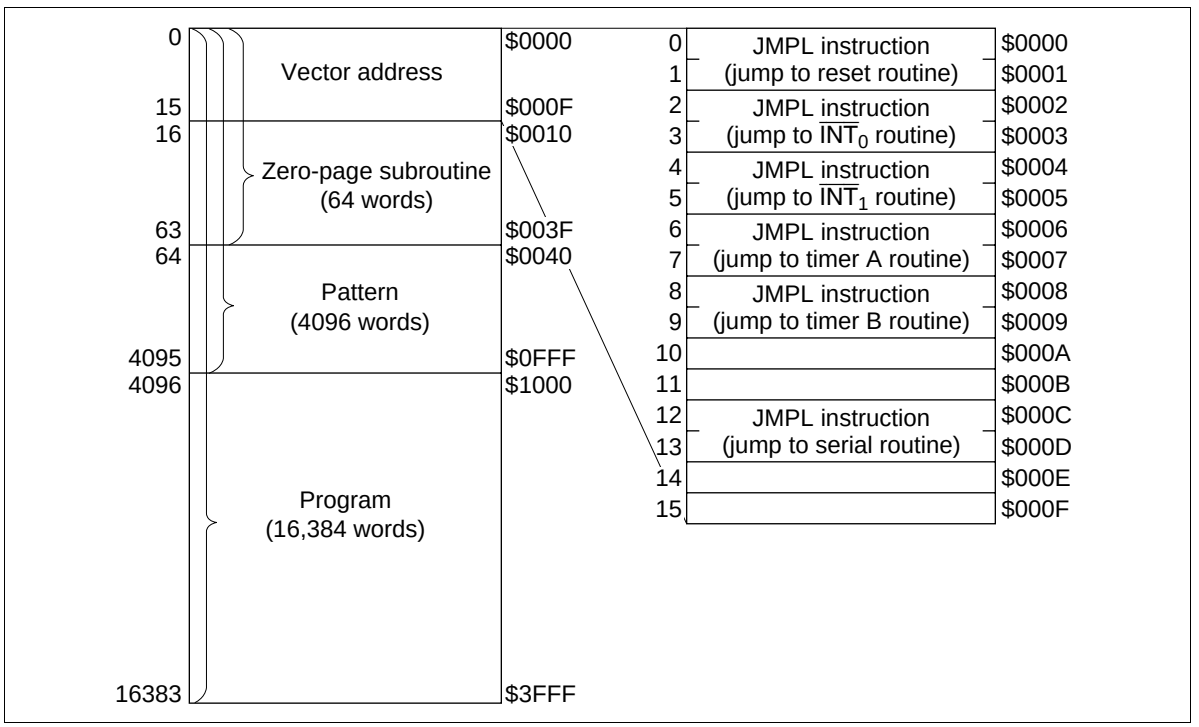


Figure 1 ROM Memory Map

RAM Memory Map

The MCU also contains a 992-digit × 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bits Area ($000 to $003): The interrupt control bits area (figure 3) is used for interrupt control. It is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($004 to $00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counters. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

Data Area ($020 to $3BF): The 16 digits, $020 through $02F, of the data area are called memory registers (MR) and are accessible by the LAMR and XMRA instructions (figure 4).

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when subroutine calls (CAL instruction, CALL instruction) or interrupts are processed. This area can be used as a 16-level nesting stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored only by the RTNI instruction. This area, when not used as a stack, is available as a data area.

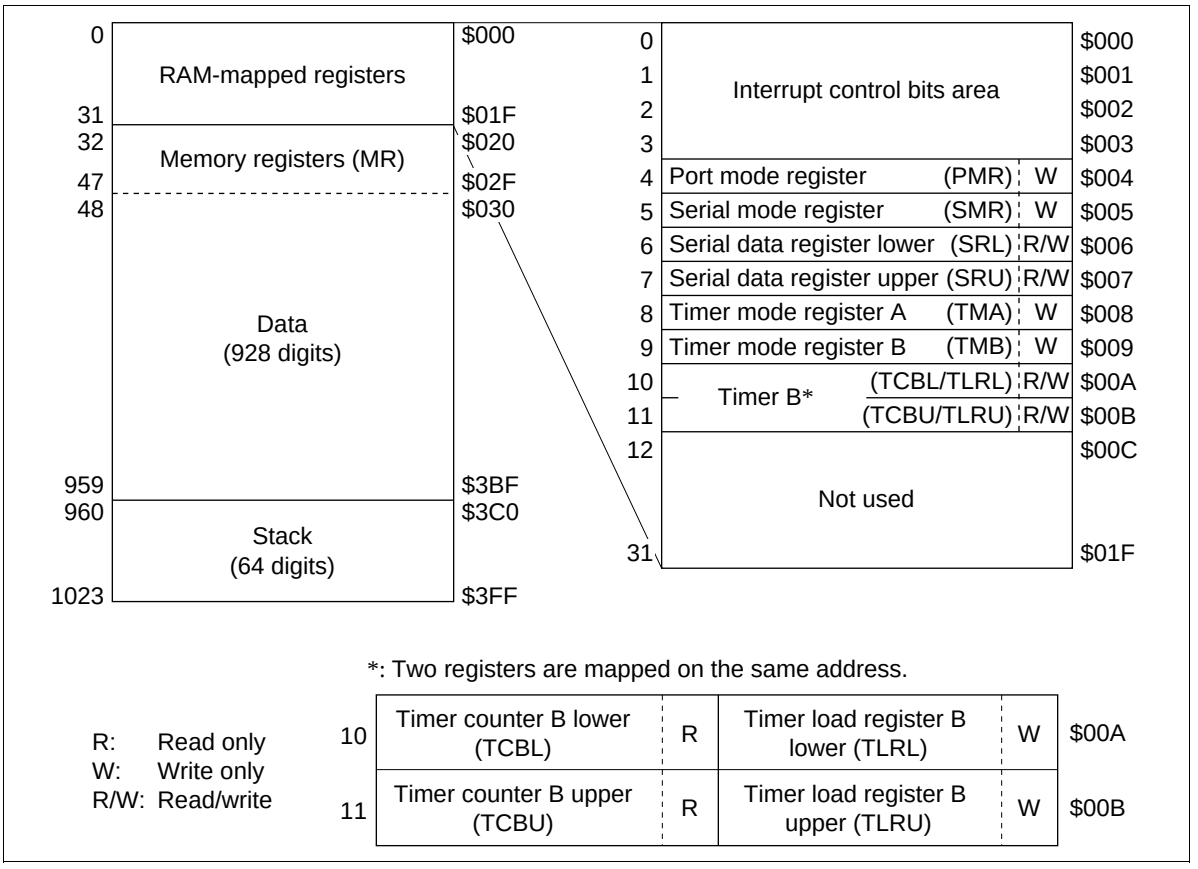


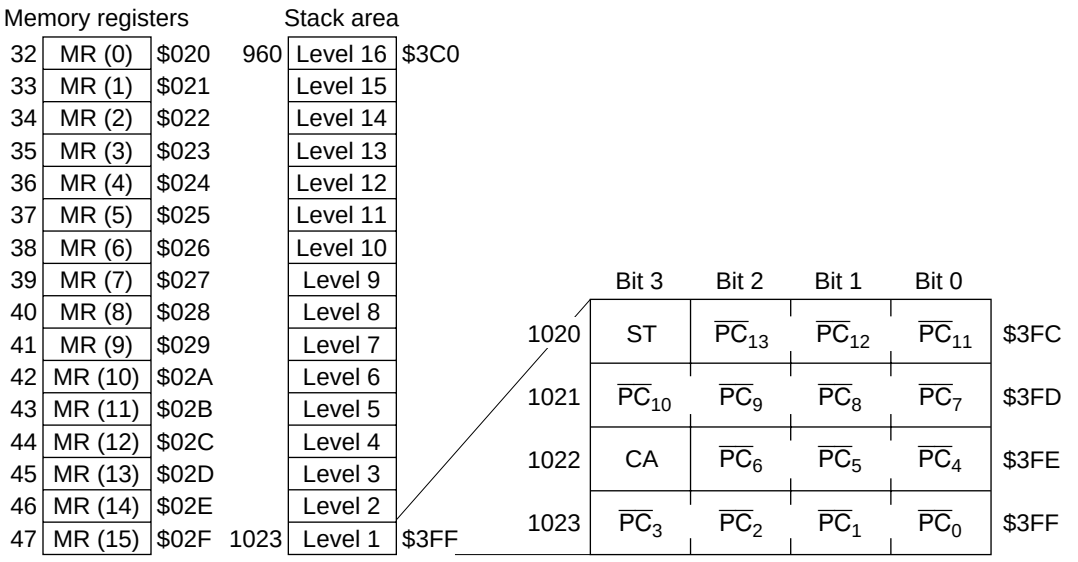
Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not used	Not used	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	Not used	Not used	IMS (IM of serial)	IFS (IF of serial)	$003

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Each bit of the interrupt control bit area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore the interrupt request flag is not affected by the SEM/SEMD instruction. The value of the status flag becomes invalid when the unusable bits are tested.

Figure 3 Interrupt Control Bits Area Configuration



PC_{13} to PC_0: Program counter
ST: Status flag
CA: Carry flag

Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

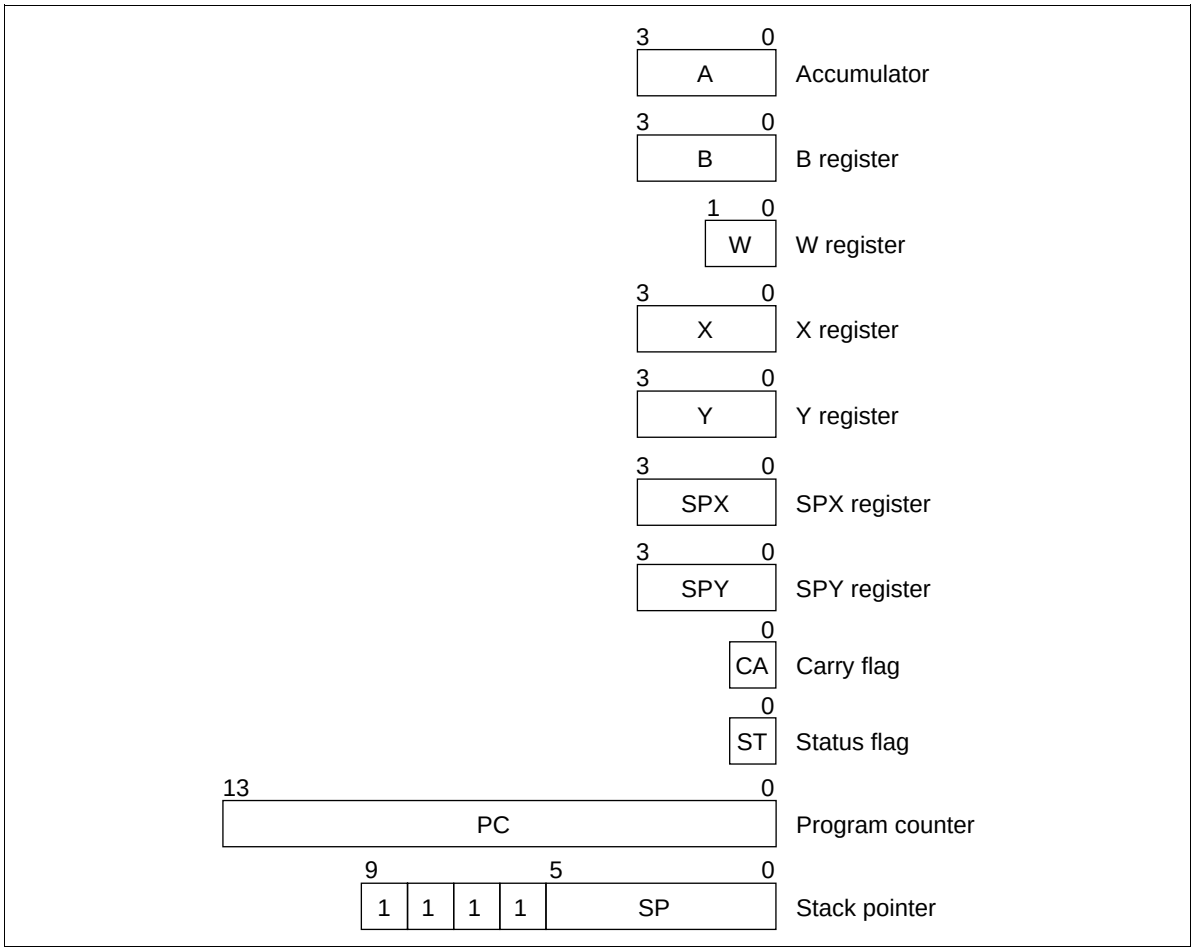


Figure 5 Registers and Flags

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the arithmetic logic unit (ALU), and transfer data to/from memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register, and the 4-bit X and Y registers indirectly address RAM. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY assist the X and Y registers, respectively.

Carry Flag (CA): The carry flag (CA) stores the overflow from the ALU generated by an arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions.

During an interrupt, a carry is pushed onto the stack. It is restored by the RTNI instruction, but not by the RTN instruction.

Status Flag (ST): The status flag (ST) holds the ALU overflow, ALU non-zero, and the results of a bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instruction. The value for the status flag remains unchanged until the next arithmetic, compare, or bit test instruction is executed. The status becomes a 1 after the BR, BRL, CAL, or CALL instruction is either executed or skipped. During an interrupt, the status is pushed onto the stack. It is restored back from the stack by the RTNI instruction, but not by the RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) points to the address of the next stack area (up to 16 levels).

The stack pointer is initialized to RAM address $3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the high-order four bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to $3FF by either MCU reset or by the RSP bit reset from the REM/REMD instruction.

Interrupts

Five interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$), timer/counters (timers A and B), and serial port (serial). For each source, an interrupt request flag (IF) interrupt mask (IM), and interrupt vector addresses control and maintain the interrupt request. The interrupt enable flag (IE) also controls interrupt operations.

Interrupt Control Bits and Interrupt Processing: The interrupt control bits are mapped on $000 through $003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

An interrupt request is generated when IF is set to 1 and IM is 0. If IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt source.

Table 1 Vector Addresses and Interrupt Priority

Reset/Interrupt	Priority	Vector Addresses
RESET	—	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Serial	5	$000C

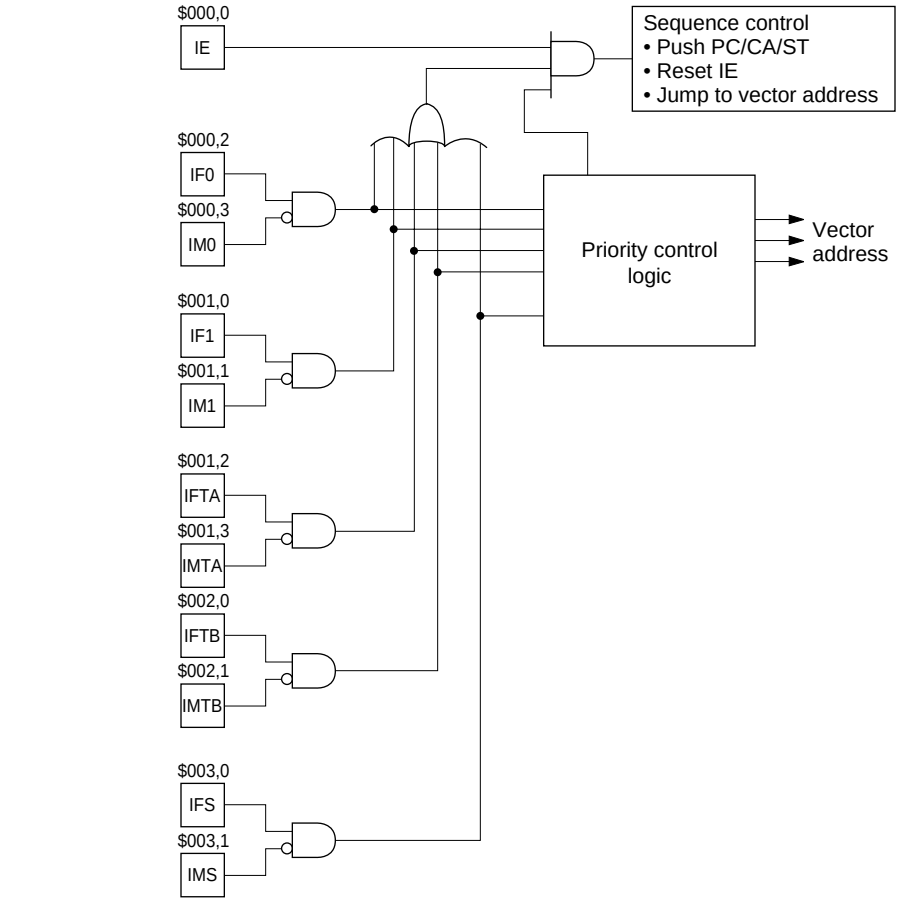
Table 2 Interrupt Conditions

	Interrupt Source				
Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	Serial
IE	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	1

Note: * Indicates don't care

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry flag, status flag, and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

At each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.



Note: $m, n is RAM address $m, bit number n.

Figure 6 Interrupt Control Circuit Block Diagram

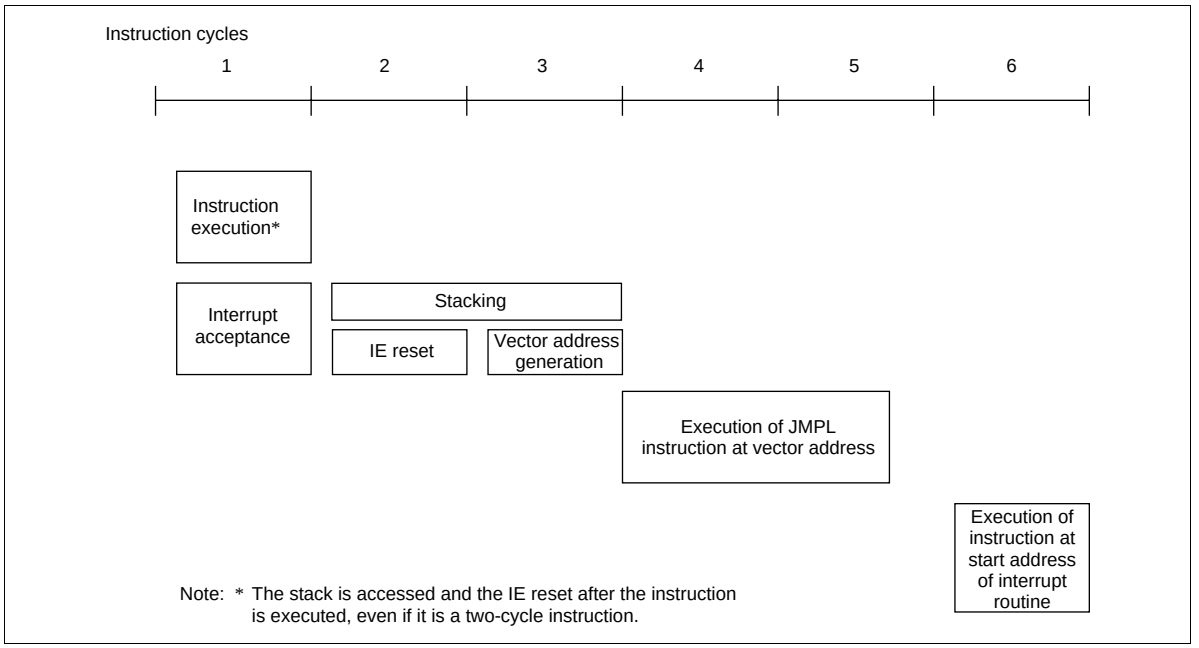


Figure 7 Interrupt Processing Sequence

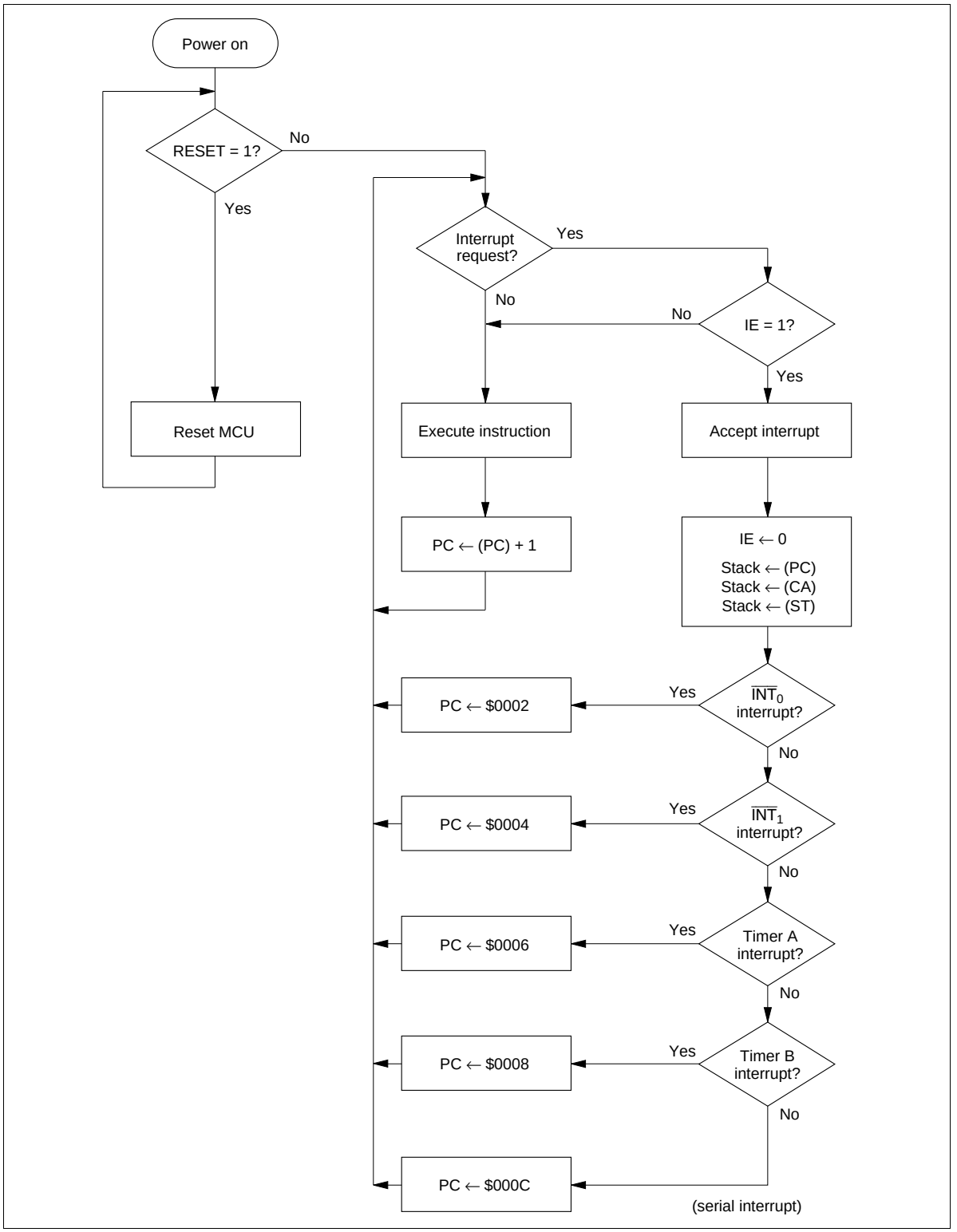


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by an interrupt and set by the RTNI instruction.

Table 3 Interrupt Enable Flag

IE	Interrupt Enable/Disable
0	Disabled
1	Enabled

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by the port mode register (PMR: $004). Setting bit 3 and bit 2 of PMR causes the $R3_3/\overline{INT_1}$ and $R3_2/\overline{INT_0}$ pins to be used as $\overline{INT_1}$ and $\overline{INT_0}$, respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs. (Refer to table 4.)

The $\overline{INT_1}$ input can be used as a clock signal input to timer B in which timer B counts up at each falling edge of the $\overline{INT_1}$ input. When $\overline{INT_1}$ is used as the timer B external event input, the external interrupt mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted. (Refer to table 5.)

Table 4 External Interrupt Request Flags

IF0, IF1	Interrupt Request
0	No
1	Yes

Table 5 External Interrupt Masks

IM0, IM1	Interrupt Request
0	Enabled
1	Disabled (masked)

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs, respectively.

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: $004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT_0}$ pin, $R3_3/\overline{INT_1}$ pin, $R4_1$/SI pin, and $R4_2$/SO pin as shown in table 6. The port mode register will be initialized to $0 by MCU reset. These pins are therefore initially used as ports.

Table 6 Port Mode Register

PMR3	$R3_3/\overline{INT_1}$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR2	$R3_2/\overline{INT_0}$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as $\overline{INT_0}$ input pin

PMR1	$R4_1$/SI Pin
0	Used as $R4_1$ port input/output pin
1	Used as SI input pin

PMR0	$R4_2$/SO Pin
0	Used as $R4_2$ port input/output pin
1	Used as SO output pin

Serial Interface

The serial interface is used to transmit/receive 8-bit data serially. It consists of the serial data register, the serial mode register, the octal counter, and the multiplexer as illustrated in figure 9. Pin $R4_0/\overline{SCK}$ and the transmit clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transmit clock signal.

The STS instruction initiates serial interface operations and resets the octal counter to \$0. The counter starts to count at the falling edge of the transmit clock ($\overline{SCK}$) signal and increments by one at the rising edge of $\overline{SCK}$. When the octal counter is reset to \$0 after eight transmit clock signals, or a transmit/receive operation is discontinued, the serial interrupt request flag will be set.

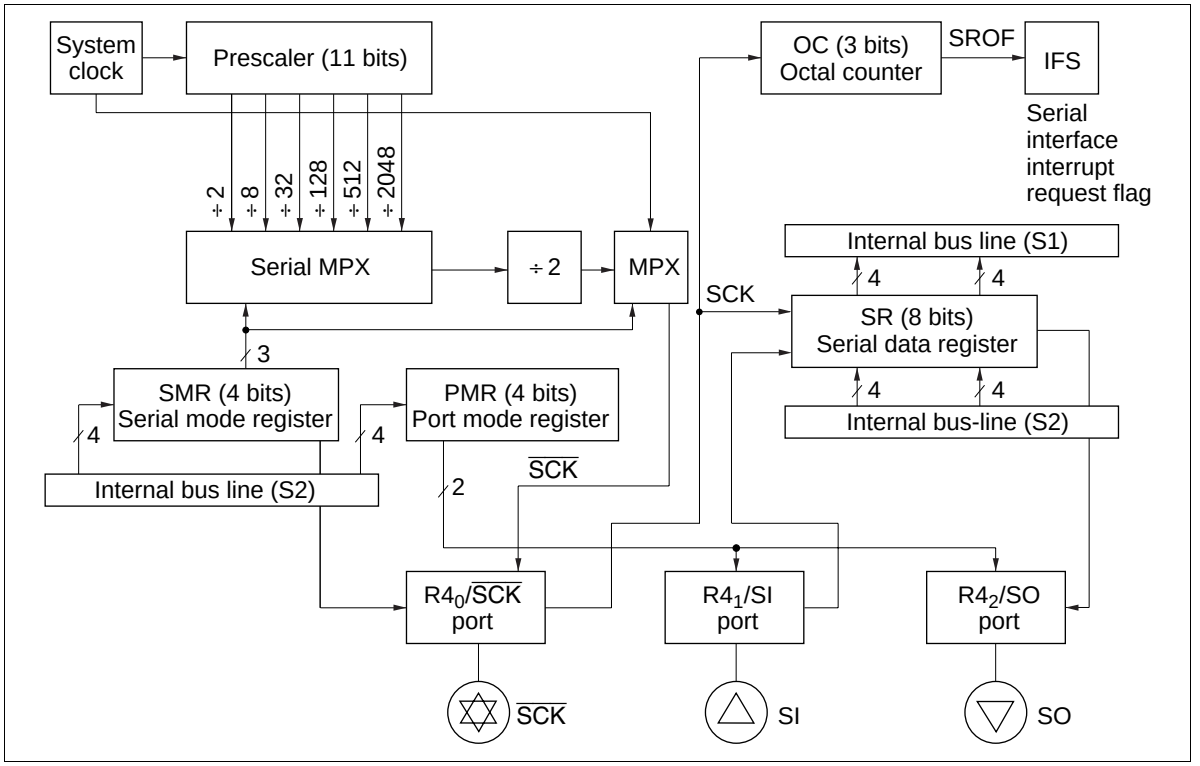


Figure 9 Serial Interface Block Diagram

Serial Mode Register (SMR: \$005): The 4-bit write-only serial mode register controls the $R4_0/\overline{SCK}$ pin, prescaler divide ratio, and transmit clock source as shown in table 7.

The write signal to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from accepting the transmit clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transmit and to set the serial interrupt request flag.

The contents of the serial mode register will be changed on the second instruction cycle after the serial mode register has been written to. Therefore, the STS instruction must be executed after the data in the serial mode register has been changed completely. The serial mode register will be reset to $0 by MCU reset.

Table 7 Serial Mode Register

SMR3	$R4_0/\overline{SCK}$
0	Used as $R4_0$ port input/output pin
1	Used as $\overline{SCK}$ input/output pin

			Transmit Clock			
SMR2	SMR1	SMR0	$R4_0/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ output	Prescaler	÷ 2048	÷ 4096
		1	$\overline{SCK}$ output	Prescaler	÷ 512	÷ 1024
	1	0	$\overline{SCK}$ output	Prescaler	÷ 128	÷ 256
		1	$\overline{SCK}$ output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ output	Prescaler	÷ 8	÷ 16
		1	$\overline{SCK}$ output	Prescaler	÷ 2	÷ 4
	1	0	$\overline{SCK}$ output	System clock	—	÷ 1
		1	$\overline{SCK}$ input	External clock	—	—

Serial Data Register (SRL: $006, SRU: $007): The 8-bit read/write serial data register consists of a low-order digit (SRL: $006) and a high-order digit (SRU: $007).

The data in the serial data register is output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transmit clock signal. At the same time, external data is input from the SI pin to the serial data register, MSB first, synchronously with the rising edge of the transmit clock. Figure 10 shows the I/O timing chart of the transmit clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

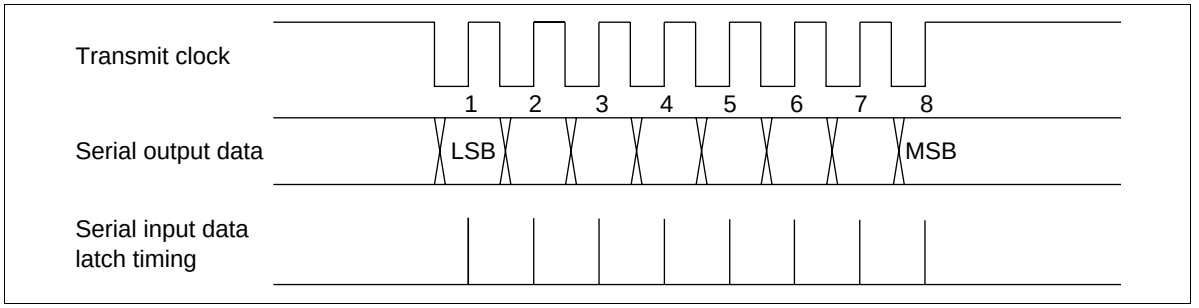


Figure 10 Serial Interface I/O Timing

Serial Interrupt Request Flag (IFS: $003, Bit 0): The serial interrupt request flag will be set when the octal counter counts eight transmit clock signals, or when data transfer is discontinued by resetting the octal counter. Refer to table 8.

Table 8 Serial Interrupt Request Flag

IFS	Interrupt Request
0	No
1	Yes

Serial Interrupt Mask (IMS: $003, Bit 1): The serial interrupt mask masks the interrupt request. Refer to table 9.

Table 9 Serial Interrupt Mask

IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

Selection and Change of the Operation Mode: Table 10 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and in the serial mode register.

Initialize the serial interface by a write signal to the serial mode register when the operation mode has changed.

Table 10 Serial Interface Operation Mode

SMR3	PMR1	PMR0	Serial Interface Operating Mode
1	0	0	Clock continuous output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Operating State of Serial Interface: The serial interface has three operating states: the STS waiting state, transmit clock wait state, and transfer state, as shown in figure 11.

The STS waiting state is the initialization state of the serial interface. The serial interface enters this state in one of two ways: either by the operation mode changing through a change in the data in the port mode register, or by data being written into the serial mode register. In this state, the serial interface does not operate even if the transmit clock is applied. If the STS instruction is executed, the serial interface shifts to the transmit clock wait state.

In the transmit clock wait state the falling edge of the first transmit clock causes the serial interface to shift to the transfer state. The octal counter then counts up and the serial data register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in the transmit clock wait state while the transmit clock outputs continuously.

The octal counter becomes 000 again after 8 transmit clocks or the execution of the STS instruction, so the serial interface returns to the transmit clock wait state and the serial interrupt request flag is set simultaneously.

When the internal transmit clock is selected, the transmit clock output is triggered by the execution of the STS instruction, and stops after 8 clocks.

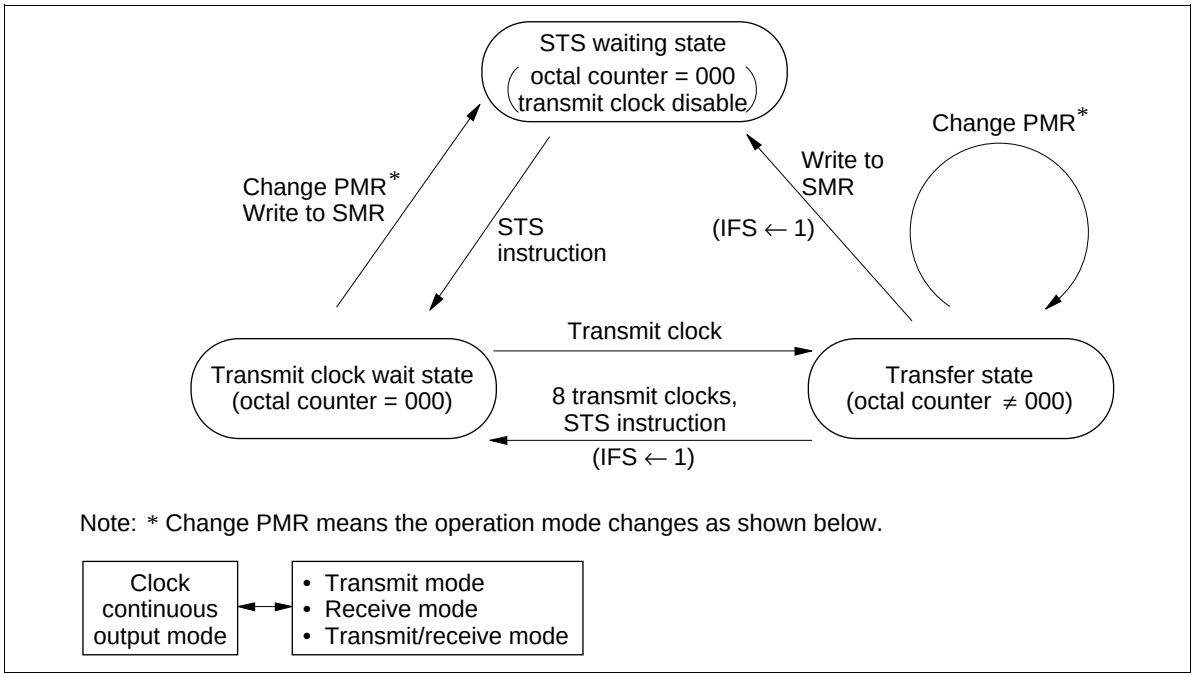


Figure 11 Serial Interface Operation State

Transmit Clock Error Detection Example: The serial interface functions abnormally when the transmit clock is disturbed by external noise. Transmit clock errors can be detected by the procedure shown in figure 12.

If more than 8 transmit clocks occur in the transfer state, the state of the serial interface shifts as follows: transfer state, transmit clock wait state, and transfer state. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure sets the IFS again.

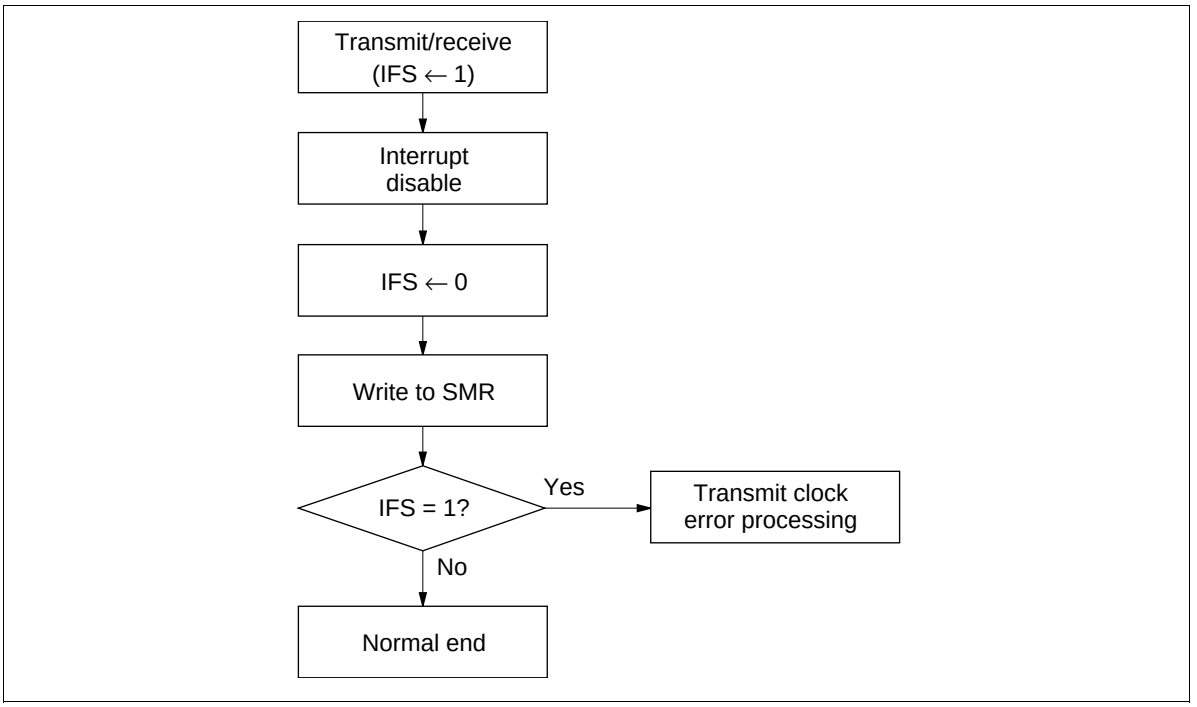


Figure 12 Transmit Clock Error Detection Example

Timers

The MCU contains a prescaler and two timer/counters (timers A and B). See figure 13. The prescaler is an 11-bit binary counter, timer A an 8-bit free-running timer, and timer B is an 8-bit auto-reload timer/event counter.

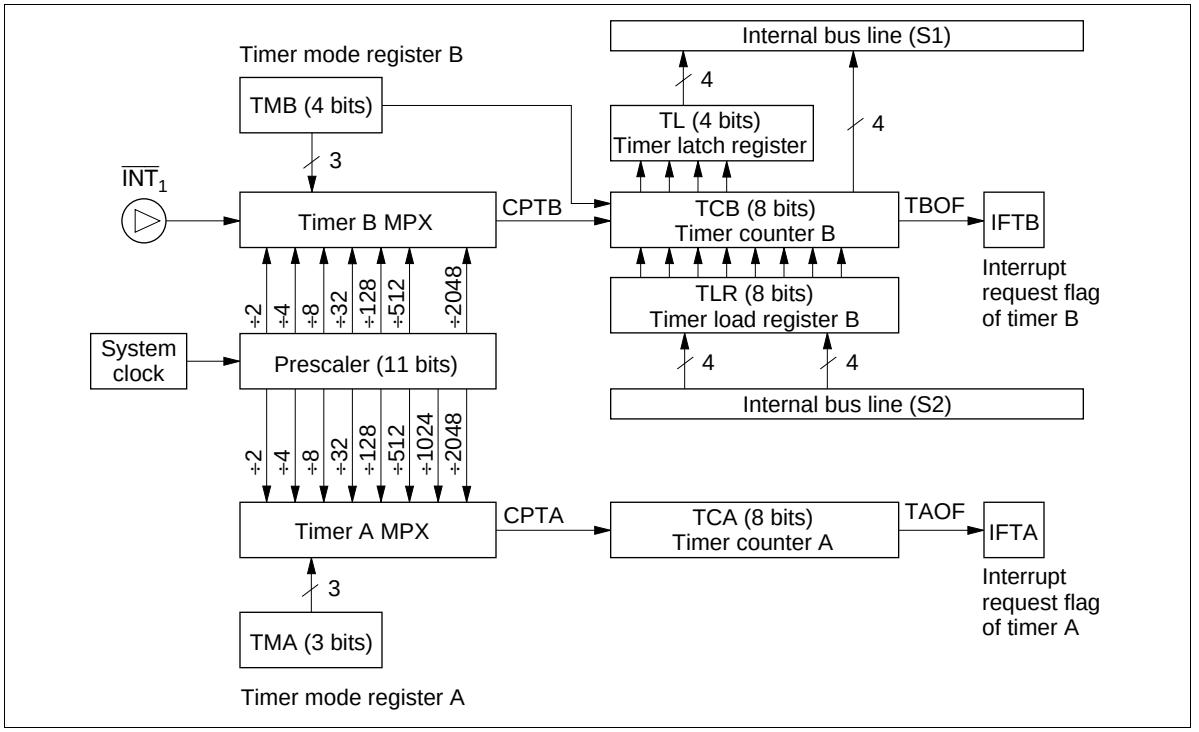


Figure 13 Timer/Counter Block Diagram

Prescaler: The input to the prescaler is the system clock signal. The prescaler is initialized to $0000 by MCU reset, and it starts to count up with the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except at MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface. The prescaler divide ratio is selected by timer mode register A (TMA), timer mode register B (TMB), or the serial mode register (SMR).

Timer A Operation: After timer A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A becomes $FF, it generates an overflow and becomes $00. This overflow causes the timer A interrupt request flag (IFTA: $001, bit 2) to go to 1. This timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to timer A are selected by timer mode register A (TMA: $008).

Timer B Operation: Timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio of timer B. When the external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT}_1$ as $\overline{INT}_1$ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into timer load register B by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to $FF, it will generate an overflow output. In this case, if the autoreload function is selected, timer B is initialized according to the value of timer load register B. If it is not selected, timer B goes to $00. The timer B interrupt request flag (IFTB: $002, bit 0) will be set at this overflow output.

Timer Mode Register A (TMA: $008): Timer mode register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of timer A clock input as shown in table 11. Timer mode register A is initialized to $0 by MCU reset.

Table 11 Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler Divide Ratio
0	0	0	÷ 2048
		1	÷ 1024
	1	0	÷ 512
		1	÷ 128
1	0	0	÷ 32
		1	÷ 8
	1	0	÷ 4
		1	÷ 2

Timer Mode Register B (TMB: $009): Timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 12. Timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after timer mode register B is written to. Timer B should be initialized by writing data into timer load register B after the contents of TMB are changed. The configuration and function of timer mode register B is shown in figure 14.

Table 12 Timer Mode Register B

TMB3	Auto-Reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
		1	÷ 512
	1	0	÷ 128
		1	÷ 32
1	0	0	÷ 8
		1	÷ 4
	1	0	÷ 2
		1	$\overline{INT}_1$ (external event input)

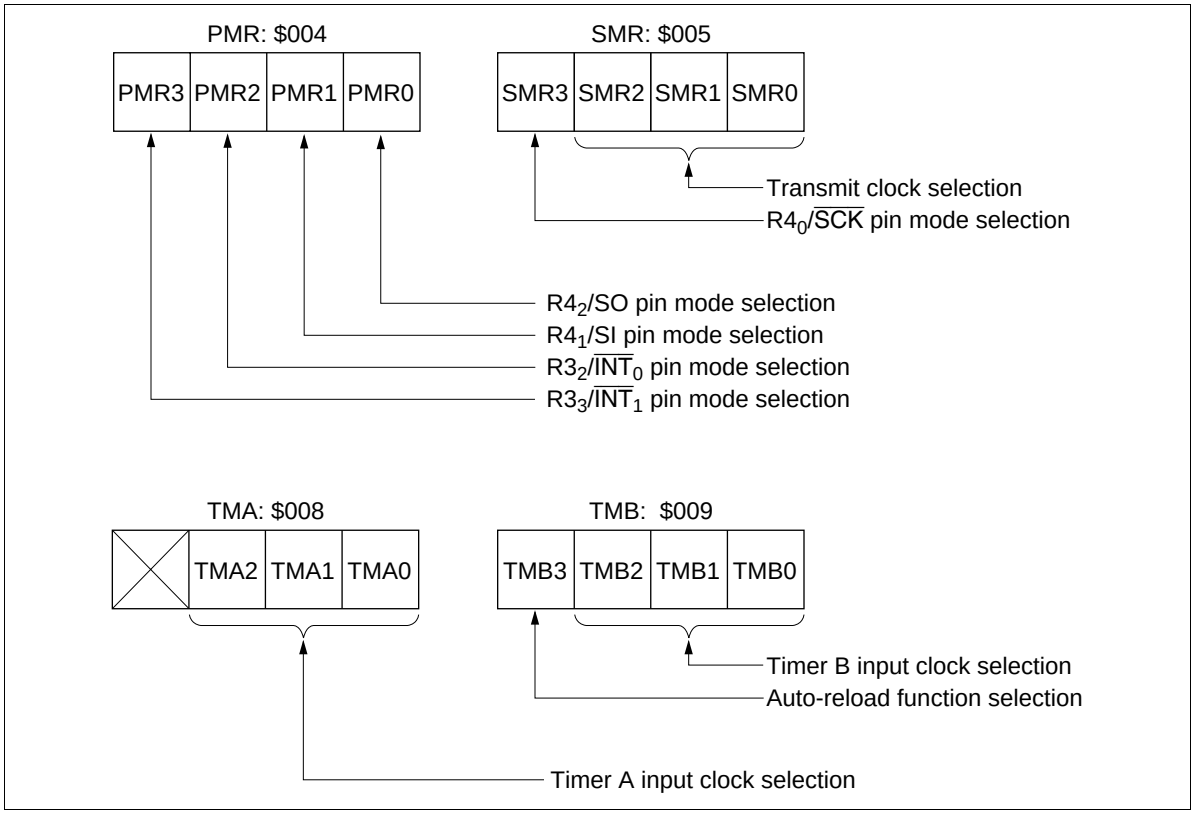


Figure 14 Mode Register Configuration and Function

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B). (Refer to figure 2.)

Timer counter B can be initialized by writing data into timer load register B. Write the low-order digit first, and then the high-order digit. The timer counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by the MCU reset.

The counter value of timer B can be obtained by reading timer counter B. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): The timer A interrupt request flag is set by the overflow output of timer A (table 13).

Table 13 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 3): The timer A interrupt mask prevents an interrupt request from being generated by the timer A interrupt request flag (table 14).

Table 14 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 15).

Table 15 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $002, Bit 1): The timer B interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag (table 16).

Table 16 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Input/Output

The MCU has 58 I/O pins, 32 standard and 26 high voltage. One of three circuit types can be selected by the mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain); and one of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, the RA_1/V_{disp} pin must be selected as V_{disp} via the mask option when the option with pull-down MOS is selected for at least one high-voltage pin. See table 17 for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected in the manner specified in table 18.

Output Circuit Operation of With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in figure 15 is used to shorten the rise time of the output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps the PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{HLT}$ signal becomes 0 in the stop mode, MOS (A), (B), and (C) turn off.

D Port: I/O port D has 16 discrete I/O pins, each of which can be addressed independently. It can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions. See tables 17 and 18 for the classification of standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The eleven R ports are composed of 36 I/O pins and 6 input-only pins. Data is input through the LAR and LBR instructions and output through the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read when the output-only and/or non-existing ports are read.

The $R3_2$, $R3_3$, $R4_0$, $R4_1$, and $R4_2$ pins are multiplexed with the $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI, and SO pins, respectively. See tables 17 and 18 for the classification of standard pins, high-voltage pins and selectable circuit types of these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent malfunction.

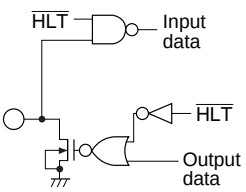
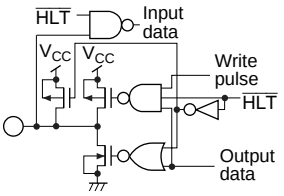
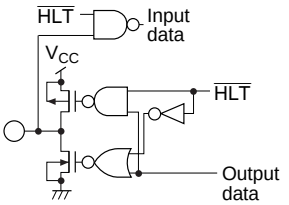
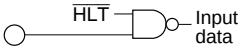
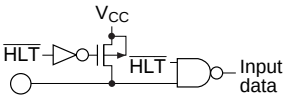
High-voltage pins: Select without pull-down MOS (PMOS open drain) via the mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select without pull-up MOS (NMOS open drain) via the mask option and connect to GND on the printed circuit board.

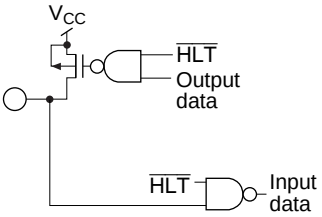
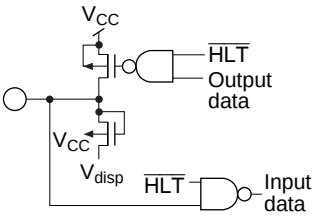
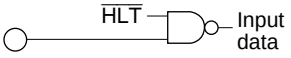
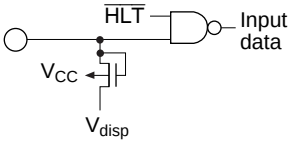
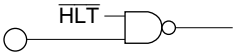
$R4_0/\overline{SCK}$ and $R4_2$/SO should be used as $R4_0$ and $R4_2$ by the serial mode register and port mode register, respectively.

Table 17 I/O Pin Circuit Types

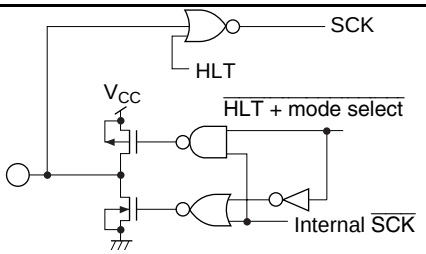
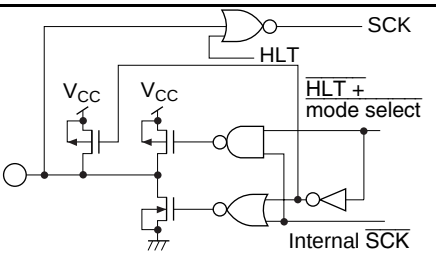
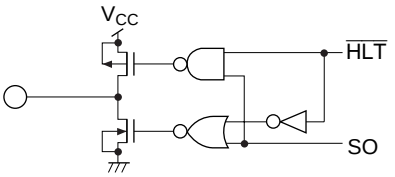
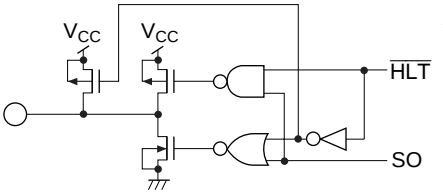
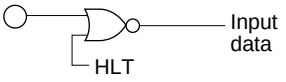
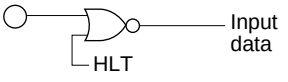
Standard Pins

	Without Pull-Up MOS (NMOS Open Drain) (A)	With Pull-Up MOS (B)	CMOS (C)	Applicable Pins
I/O common pins				D_0–D_3, $R3_0$–$R3_3$, $R4_0$–$R4_3$, $R5_0$–$R5_3$, $R6_0$–$R6_3$, $R7_0$–$R7_3$, $R8_0$–$R8_3$
Input pins			—	$R9_0$–$R9_3$

High Voltage Pins

	Without Pull-Down MOS (PMOS Open Drain) (D)	With Pull-Up MOS (E)	Applicable Pins
I/O common pins			D_4–D_{15}, $R0_0$–$R0_3$, $R1_0$–$R1_3$, $R2_0$–$R2_3$
Input pins			RA_0
Input pins		—	RA_1

Standard Pins

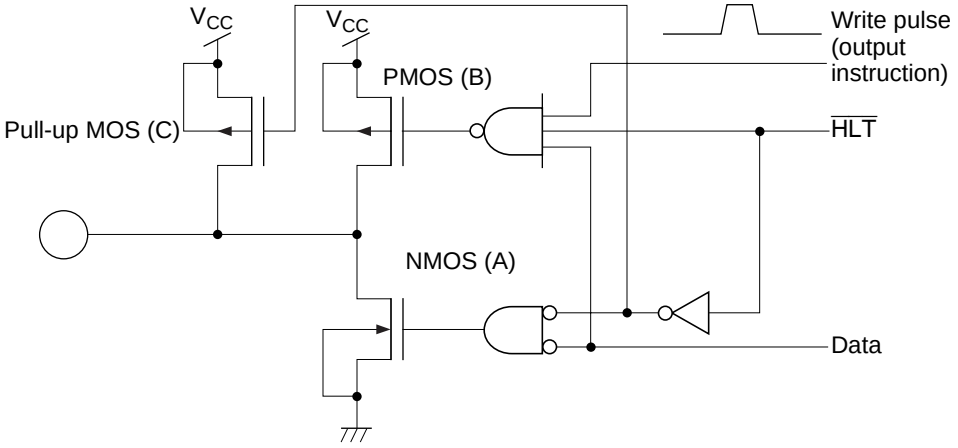
	Without Pull-Up MOS (NMOS Open Drain) or CMOS (A or C)	With Pull-Up MOS (B)	Applicable Pins
I/O common pins			SCK* (output mode)
Output pins			SO
Input pins			$\overline{INT}_0$, $\overline{INT}_1$ SI, SCK (input mode)

Notes: In the stop mode, HLT is 0, HLT is 1 and I/O pins are in high impedance.

* If the MCU is interrupted by the serial interface in the external clock input mode, the SCK terminal becomes input only.

Table 18 Data Input from Common Input/Output Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High voltage pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0



MOS Buffer	On-Resistance Value
A	Approximately 250 Ω
B	Approximately 1 kΩ
C	Approximately 30 kΩ to 160 kΩ (V_{CC} = 5 V)

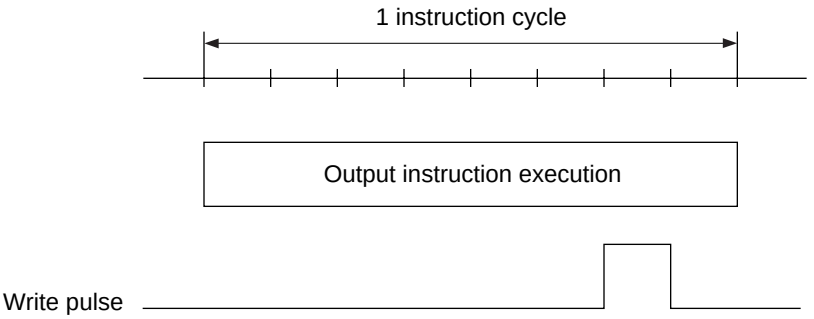


Figure 15 Output Circuit Operation of With Pull-Up MOS Standard Pins

Reset

Pulling the RESET pin high resets the MCU. At power-on or when cancelling the stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instruction cycles are required for the MCU to be reset.

Table 19 shows the components initialized by MCU reset, and the status of each.

Table 19 Initial Values After MCU Reset

Item			Initial Value by MCU Reset	Contents
Program counter (PC)			$0000	Execute program from the top of ROM address
Status flag (ST)			1	Enable branching with conditional branch instructions
Stack pointer (SP)			$3FF	Stack level is 0
I/O pins, output register	Standard pins	(A) Without pull-up MOS	1	Enable to input
		(B) With pull-up MOS	1	Enable to input
		(C) CMOS	1	—
	High-voltage pins	(D) Without pull-down MOS	0	Enable to input
		(E) With pull- down MOS	0	Enable to input
Interrupt flags	Interrupt enable flag (IE)		0	Inhibit all interrupts
	Interrupt request flag (IF)		0	No interrupt request
	Interrupt mask (IM)		1	Mask interrupt request
Mode registers	Port mode register (PMR)		0000	See Port Mode Register section
	Serial mode register (SMR)		0000	See Serial Mode Register section
	Timer mode register A (TMA)		000	See Timer Mode Register A section
	Timer mode register B (TMB)		0000	See Timer Mode Register B section
Timer/counters	Prescaler		$000	—
	Timer counter A (TCA)		$00	—
	Timer counter B (TCB)		$00	—
	Timer load register (TLR)		$00	—
	Octal counter		000	—

Item		After MCU Reset to Recover from Stop Mode	After MCU Reset to Recover from Other Modes
Carry flag	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial data register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained	Same as above for RAM

Internal Oscillator Circuit

Figure 16 outlines the internal oscillator circuit. A crystal oscillator or ceramic oscillator can be selected as the oscillator type. Refer to table 20 to select the oscillator type. In addition, see figure 17 for the layout of the crystal or ceramic oscillator.

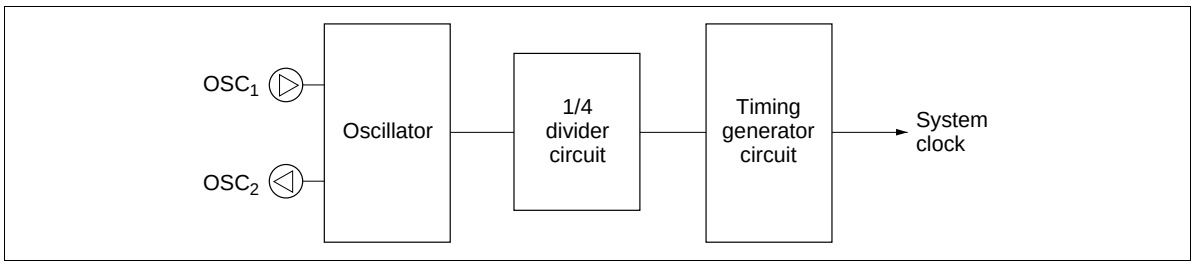


Figure 16 Internal Oscillator Circuit

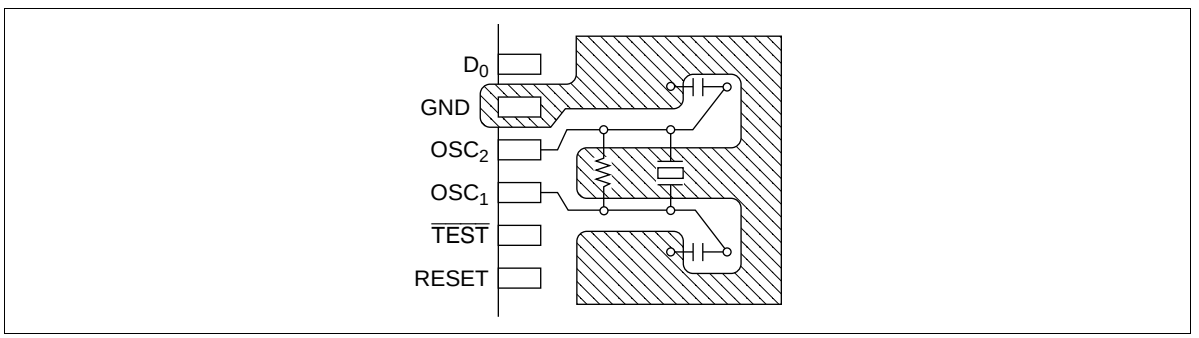
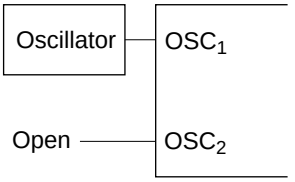
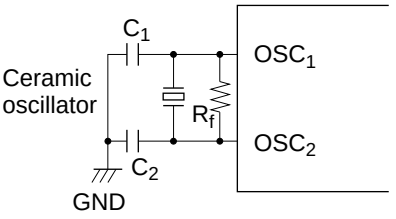
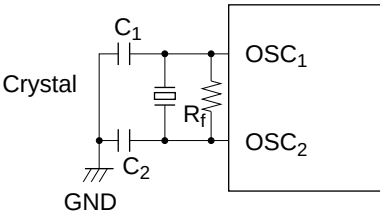
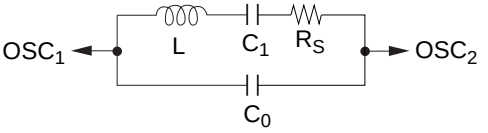


Figure 17 Layout of Crystal or Ceramic Oscillator

Table 20 Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
External clock operation (OSC_1, OSC_2)		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator CSA4.00MG (Murata) R_f: 1 MΩ ±20% C_1: 30 pF ±20% C_2: 30 pF ±20%
Crystal oscillator (OSC_1, OSC_2)	 AT-cut parallel resonance crystal 	R_f: 1 MΩ ±20% C_1: 10 pF to 22 pF ±20% C_2: 10 pF to 22 pF ±20% Crystal: Equivalent circuit shown at bottom left C_o: 7 pF max. R_s: 100 Ω max. f: 1.0 MHz to 4.5 MHz

Notes: 1. The circuit parameters written above are recommended by the crystal or ceramic oscillator manufacturer. The circuit parameters are affected by the crystal, ceramic resonator, and the floating capacitance when designing the board.

When using the resonator, consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic oscillator. Refer to figure 17.

Operating Modes

The MCU has two low-power dissipation modes, standby mode and stop mode (table 21). Figure 18 is a mode transition diagram for these modes.

Standby Mode: Executing the SBY instruction puts the MCU into standby mode. In standby mode, the oscillator circuit is active, and the interrupts, timer/counters, and serial interface remain working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 21 Low-Power Dissipation Modes

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Registers, flags	Retained	Reset*[1]
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained*[2]	High impedance
Timer/counters, serial interface	Active	Stopped
Cancellation method	RESET input, interrupt request	RESET input

Notes: 1. The MCU recovers from the stop mode by RESET input. Refer to table 19 for the contents of flags and registers.
2. When I/O circuits are active, an I/O current may flow in the standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

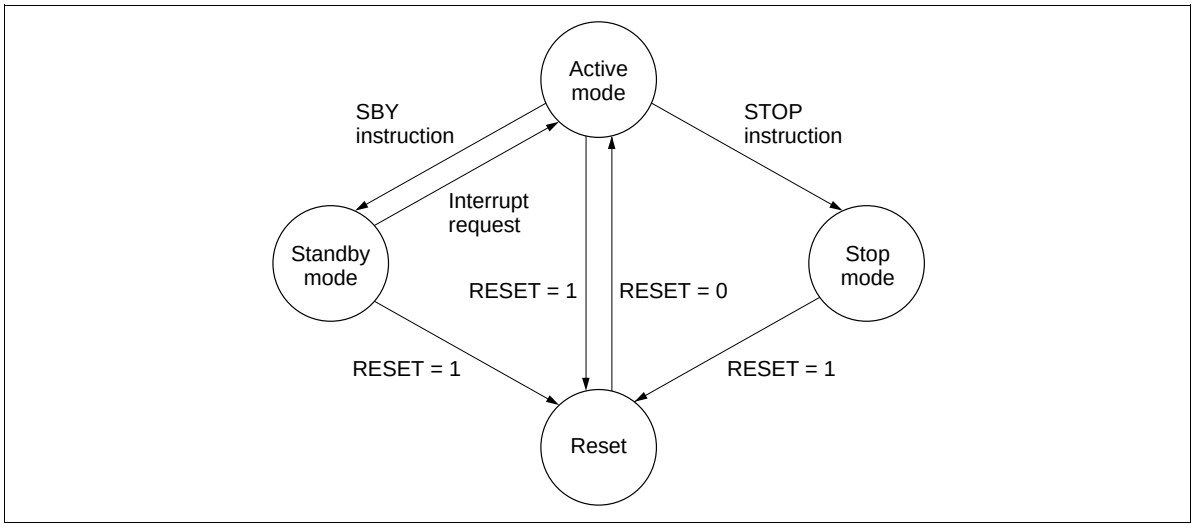


Figure 18 MCU Operating Mode Transition

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction. If the interrupt enable flag is 1 when an interrupt request is asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues.

Figure 19 shows the flowchart of the standby mode.

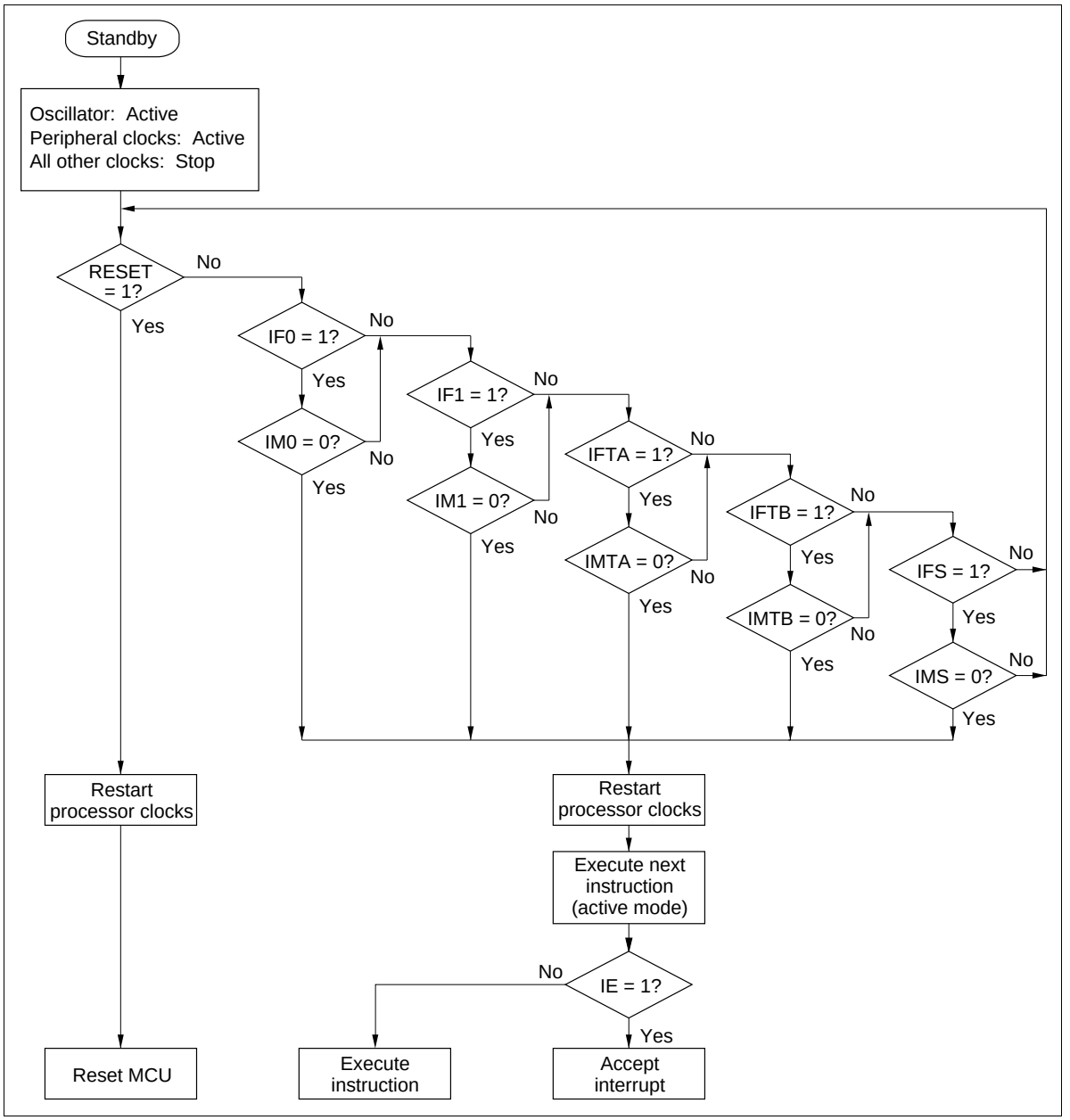


Figure 19 MCU Operating Flowchart in Standby Mode

Stop Mode: Executing the STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

The stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 20, reset input must be applied for at least t_{RC} for oscillation to be stabilized. (Refer to the AC Characteristics table.) After the stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, X/SPX registers, Y/SPY registers, carry flag, and serial data register will not retain their contents.

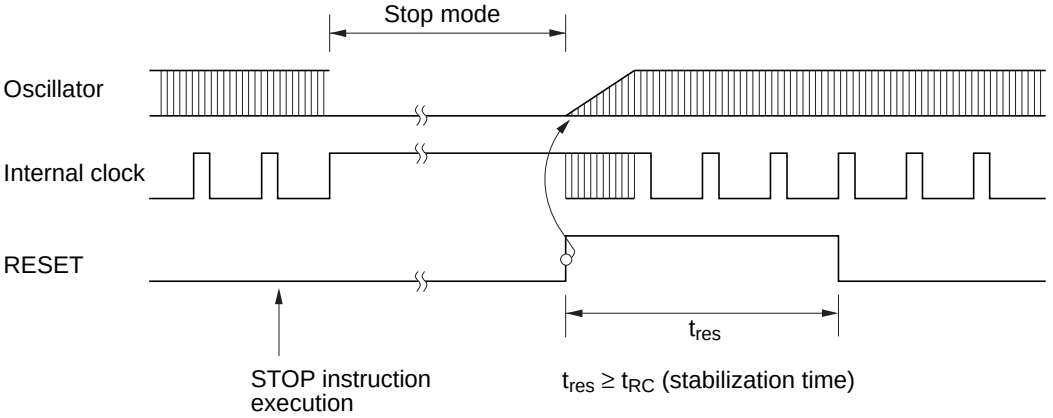


Figure 20 Timing of Stop Mode Cancellation

PROM Mode Pin Description

Table 22 describes the pin functions in PROM mode.

Table 22 PROM Mode Signals

Pin Number			MCU Mode		PROM Mode	
DC-64S, DP-64S	FP-64B	FP-64A	Symbol	I/O	Symbol	I/O
1	59	57	D_{11}	I/O	V_{CC}	
2	60	58	D_{12}	I/O		
3	61	59	D_{13}	I/O		
4	62	60	D_{14}	I/O		
5	63	61	D_{15}	I/O		
6	64	62	$R0_0$	I/O	A_1	I
7	1	63	$R0_1$	I/O	A_2	I
8	2	64	$R0_2$	I/O	A_3	I
9	3	1	$R0_3$	I/O	A_4	I
10	4	2	$R1_0$	I/O	A_5	I
11	5	3	$R1_1$	I/O	A_6	I
12	6	4	$R1_2$	I/O	A_7	I
13	7	5	$R1_3$	I/O	A_8	I
14	8	6	$R2_0$	I/O	A_0	I
15	9	7	$R2_1$	I/O	A_{10}	I
16	10	8	$R2_2$	I/O	A_{11}	I
17	11	9	$R2_3$	I/O	A_{12}	I
18	12	10	RA_0	I	V_{CC}	
19	13	11	RA_1/V_{disp}	I		
20	14	12	$R3_0$	I/O	A_{13}	I
21	15	13	$R3_1$	I/O	A_{14}	I
22	16	14	$R3_2/\overline{INT}_0$	I/O		
23	17	15	$R3_3/\overline{INT}_1$	I/O		
24	18	16	$R5_0$	I/O		
25	19	17	$R5_1$	I/O		
26	20	18	$R5_2$	I/O		
27	21	19	$R5_3$	I/O		
28	22	20	$R6_0$	I/O		
29	23	21	$R6_1$	I/O		

Pin Number			MCU Mode		PROM Mode	
DC-64S, DP-64S	FP-64B	FP-64A	Symbol	I/O	Symbol	I/O
30	24	22	$R6_2$	I/O		
31	25	23	$R6_3$	I/O		
32	26	24	V_{CC}		V_{CC}	
33	27	25	$R4_0/\overline{SCK}$	I/O	O_4	I/O
34	28	26	$R4_1$/SI	I/O	O_5	I/O
35	29	27	$R4_2$/SO	I/O	O_6	I/O
36	30	28	$R4_3$	I/O	O_7	I/O
37	31	29	$R7_0$	I/O	$\overline{CE}$	I
38	32	30	$R7_1$	I/O	$\overline{OE}$	I
39	33	31	$R7_2$	I/O		
40	34	32	$R7_3$	I/O	O_4	I/O
41	35	33	$R8_0$	I/O	O_3	I/O
42	36	34	$R8_1$	I/O	O_2	I/O
43	37	35	$R8_2$	I/O	O_1	I/O
44	38	36	$R8_3$	I/O	O_0	I/O
45	39	37	$R9_0$	I	V_{PP}	
46	40	38	$R9_1$	I	A_9	I
47	41	39	$R9_2$	I	$\overline{M}_0$	I
48	42	40	$R9_3$	I	$\overline{M}_1$	I
49	43	41	RESET	I	RESET	I
50	44	42	$\overline{TEST}$	I	$\overline{TEST}$	I
51	45	43	OSC_1	I		
52	46	44	OSC_2			
53	47	45	GND		GND	
54	48	46	D_0	I/O	O_0	I/O
55	49	47	D_1	I/O	O_1	I/O
56	50	48	D_2	I/O	O_2	I/O
57	51	49	D_3	I/O	O_3	I/O
58	52	50	D_4	I/O		
59	53	51	D_5	I/O		

Pin Number			MCU Mode		PROM Mode	
DC-64S, DP-64S	FP-64B	FP-64A	Symbol	I/O	Symbol	I/O
60	54	52	D_6	I/O		
61	55	53	D_7	I/O		
62	56	54	D_8	I/O		
63	57	55	D_9	I/O		
64	58	56	D_{10}	I/O	V_{CC}	

Notes: 1. I/O: Input/output pins
I: Input pins
O: Output pins
2. Connect each pair of O_4, O_3, O_2, O_1, and O_0. Hitachi supplies the socket adapter on which these pairs are internally connected.

Programmable ROM Operation

The on-chip PROM of HD4074019 and HD407L4019 are programmed in PROM mode. The PROM mode is set by pulling $\overline{TEST}$, $\overline{M}_0$, and $\overline{M}_1$ low, and RESET high as shown in figure 21. In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 64-to-28-pin socket adapter. Table 24 lists the recommended PROM programmers and socket adapters.

Since the instruction of the HMCS400 series consists of 10 bits, the HMCS400-series microcom puter incorporates a conversion circuit used as a general-purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, the low-order 5 bits and the high-order 5 bits. For example, if 8 kwords of an on-chip PROM are programmed by a general purpose PROM programmer, 16 kbytes of addresses ($0000 to $3FFF) should be specified.

Programming and Verification

The HD4074019 and HD407L4019 can be programmed at high-speed without causing voltage stress or affecting data reliability.

Table 23 shows how programming and verification modes are selected.

Erasing

PROMs with ceramic window packages can be erased by ultraviolet light. All erased bits become 1s.

The erasing specifications are as follows: ultraviolet (UV) light with wavelength 2537 Å with a minimum irradiation of 15 W sec/cm^2. These conditions are satisfied by exposing the LSI to a 12,000-μW/cm^2 UV source for 15 to 20 minutes at a distance of 1 inch.

Precautions

1. Addresses $0000 to $7FFF should be specified if the PROM is programmed by a PROM programmer. Note that the plastic package type cannot be erased and reprogrammed.
   (Only ceramic window packages can be erased and reprogrammed.)

2. Make sure that the PROM programmer, socket adapter, and LSI match properly. Using the wrong programmer for the socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed to the programmer.

3. The PROM should be programmed with V_{PP} = 12.5 V. Other PROMs use 21 V. If 21 V is applied to the HD4074019 and HD407L4019, the LSI may be permanently damaged. 12.5 V is the voltage for V_{PP} of Intel's 27256.

Table 23 PROM Modes Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0 to O_7**
Programming	Low	High	V_{PP}	Data input
Verify	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 24 Recommended PROM Programmers and Socket Adapters

PROM Programmer*			**Socket Adapter**	
Maker	**Type Name**	**Package Type**	**Type Name**	**Maker**
DATA I/O	280	DP-64S	HS409ESS11H	Hitachi
	201	DC-64S		
	29B + UniPak2B	FP-64B	HS409ESF01H	
	S22	FP-64A	HS409ESH01H	
AVAL DATA Corp.	PKW-1000	DP-64S	HS409ESS21H	Hitachi
	PKW-1100	DC-64S		
	PKW-1600	FP-64B	HS409ESF01H	
	PKW-3100	FP-64A	HS409ESH01H	

Note: * Since the address pins of the HD4074019 and HD407L4019 are high voltage pins, errors may occur in device insertion tests if a PROM programmer other than those listed above is used.

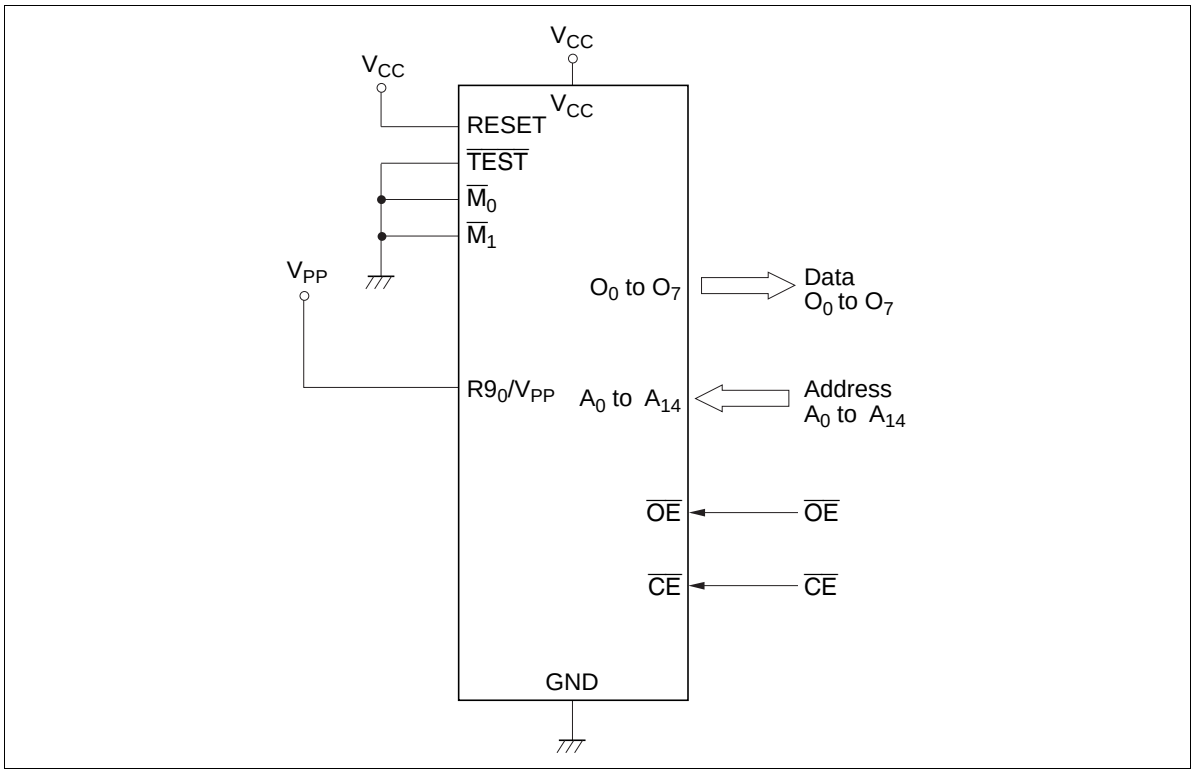


Figure 21 PROM Mode Function Diagram

Addressing Modes

RAM Addressing Modes

As shown in figure 22, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

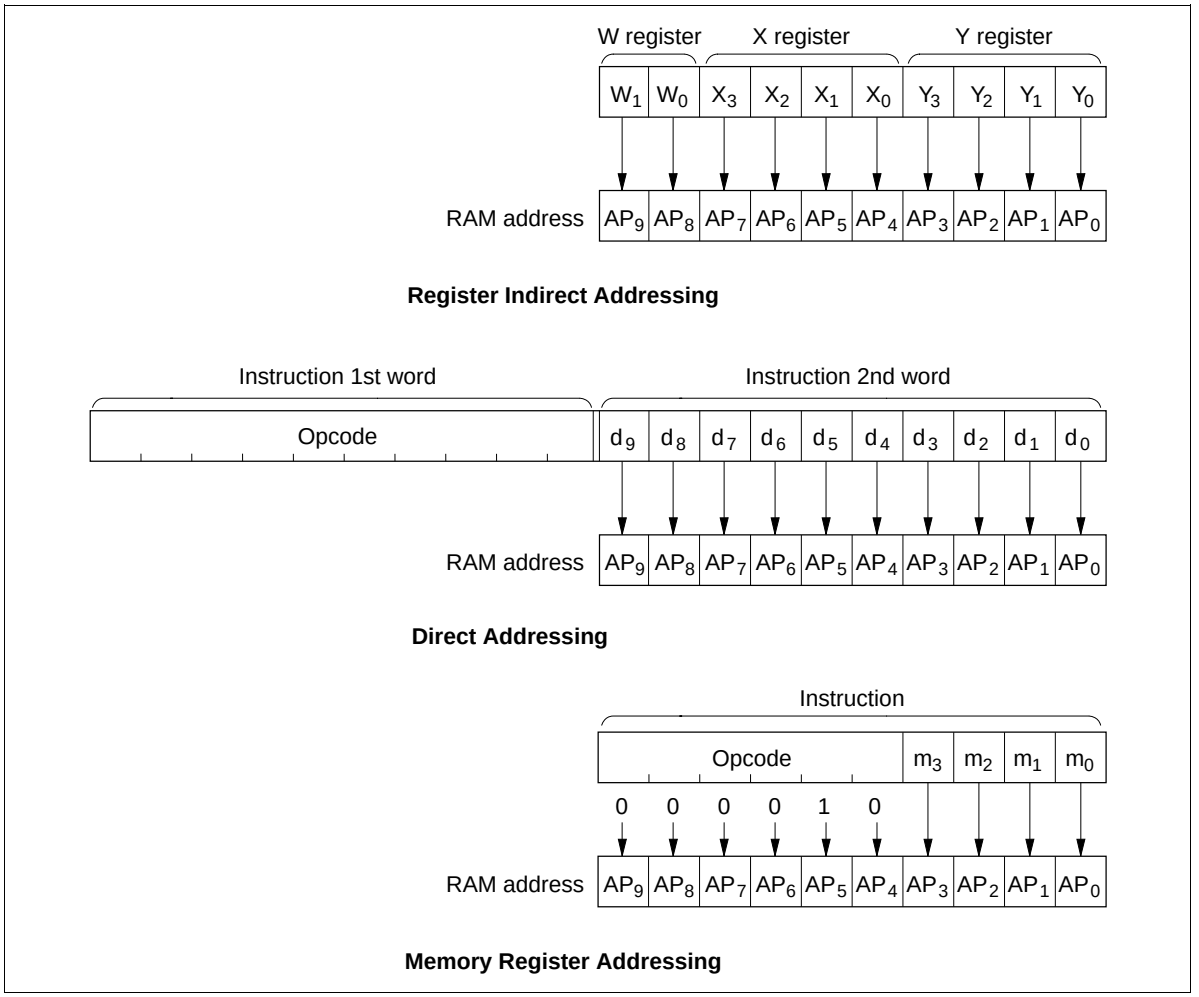


Figure 22 RAM Addressing Modes

Register Indirect Addressing Mode: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing Mode: The memory registers (16 digits from $020 to $02F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four kinds of ROM addressing modes as shown in figure 23.

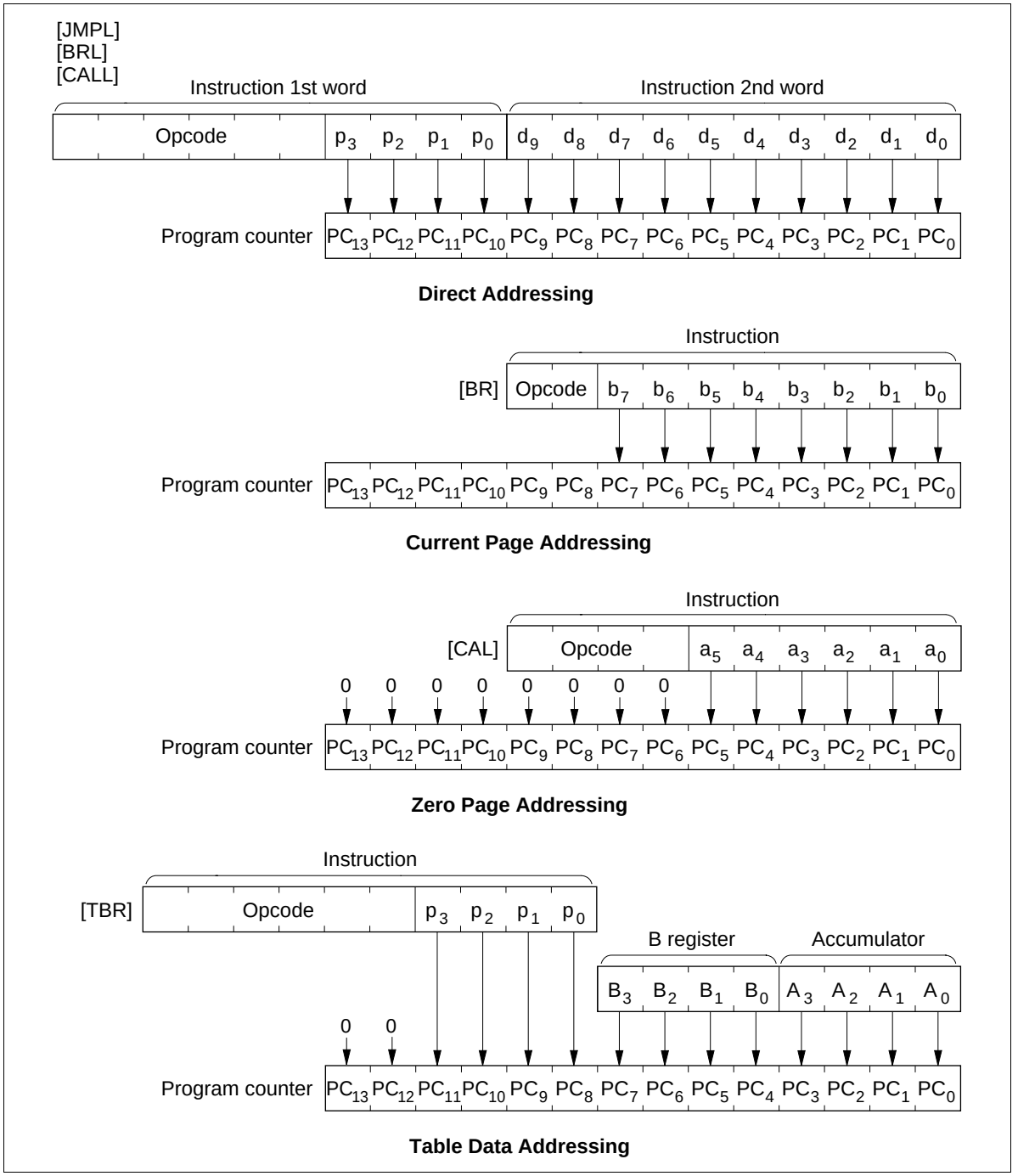


Figure 23 ROM Addressing Modes

Direct Addressing Mode: The program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 8 pages of ROM with 256 words per page. By executing the BR instruction, the program can branch to an address on the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

When the BR instruction is on a page boundary (256n + 255) (figure 24), executing it transfers the PC contents to the next page, due to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400-series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000 to $003F. When the CAL instruction is executed, 6 bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing Mode: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referenced by the P instruction (figure 25). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

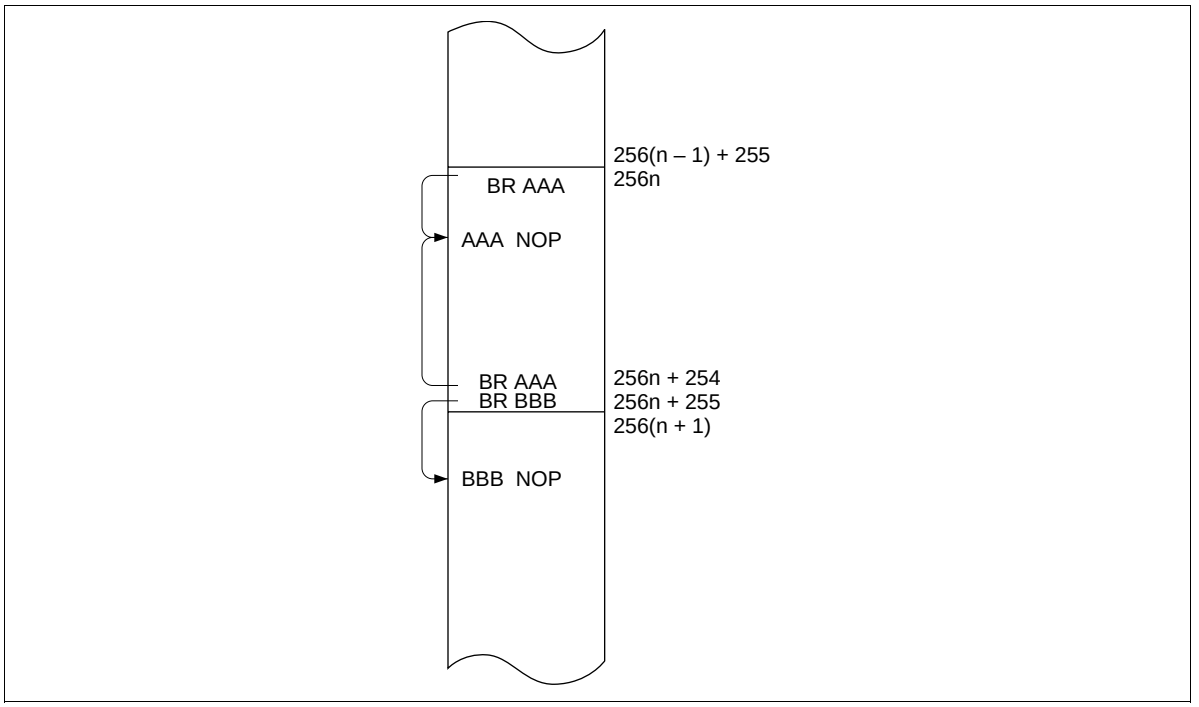


Figure 24 BR Instruction Branch Destination on a Page Boundary

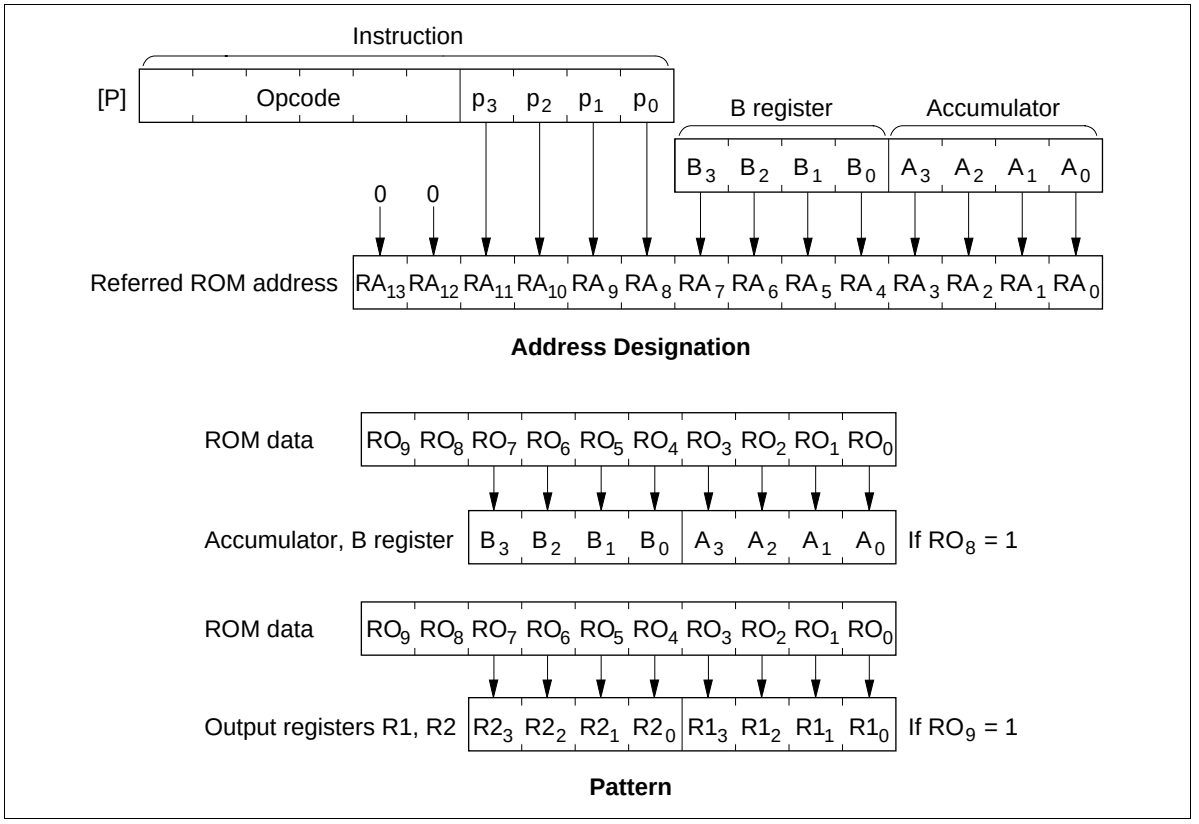


Figure 25 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14	V	10
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
		V_{CC} – 45 to V_{CC} + 0.3	V	2
Total permissible input current	$\sum I_o$	50	mA	3
Maximum input current	I_o	15	mA	5, 6
Maximum output current	$-I_o$	4	mA	6, 7
		6	mA	7, 8
		30	mA	7, 9
Total permissible output current	$-\sum I_o$	150	mA	4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation should be under the conditions of the electrical characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of the LSI.

All voltages are with respect to GND.

1. Standard pins.
2. High voltage pins.
3. Total permissible input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
4. Total permissible output current is the total sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
5. Maximum input current is the maximum amount of input current from each I/O pin to GND.
6. D_0 to D_3 and R3 to R8.
7. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
8. R0 to R2.
9. D_4 to D_{15}.
10. Applied to HD4074019 and HD407L4019.

Electrical Characteristics

DC Characteristics

(HD404019R: V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD40L4019R: V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD4074019: V_{CC} = 4.5 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD407L4019: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	0.8 V_{CC}	—	V_{CC} + 0.3	V	HD404019R, HD4074019	
			0.9 V_{CC}	—	V_{CC} + 0.3	V	HD40L4019R	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			0.9 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019	
		SI	0.7 V_{CC}	—	V_{CC} + 0.3	V	HD404019R, HD4074019	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD40L4019R	
			0.7 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			0.9 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019	
		OSC_1	V_{CC} –0.5	—	V_{CC} + 0.3	V	HD404019R, HD4074019, HD407L4019	
			V_{CC} –0.3	—	V_{CC} + 0.3	V	HD40L4019R	
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	0.2 V_{CC}	V	HD404019R, HD4074019	
			–0.3	—	0.1 V_{CC}	V	HD40L4019R	
			–0.3	—	0.2 V_{CC}	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			–0.3	—	0.1 V_{CC}	V	HD407L4019	
		SI	–0.3	—	0.3 V_{CC}	V	HD404019R, HD4074019	
			–0.3	—	0.2 V_{CC}	V	HD40L4019R	
			–0.3	—	0.3 V_{CC}	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			–0.3	—	0.1 V_{CC}	V	HD407L4019	
Input low voltage	V_{IL}	OSC_1	–0.3	—	0.5	V	HD404019R, HD4074019, HD407L4019	
			–0.3	—	0.3	V	HD40L4019R	
Output high voltage	V_{OH}	$\overline{SCK}$, SO	V_{CC} –1.0	—	—	V	$–I_{OH}$ = 1.0 mA	
			V_{CC} –0.5	—	—	V	$–I_{OH}$ = 0.5 mA	

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Output low voltage	V_{OL}	$\overline{SCK}$, SO	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	| IIL |	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	8.0	mA	HD404019R, HD4074019: V_{CC} = 5 V, f_{OSC} = 4 MHz, divide by 4	2
			—	—	8.0	mA	HD40L4019R, HD407L4019: V_{CC} = 5 V, f_{OSC} = 4 MHz, divide by 4	2
			—	—	3.0	mA	HD40L4019R, HD407L4019: V_{CC} = 3 V, f_{OSC} = 3.58 MHz, divide by 4	2
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, divide by 4	3
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	HD404019R, HD40L4019R: V_{in} ($\overline{TEST}$, $R9_0$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 V to 0.3 V	4
			—	—	10	µA	HD4074019, HD407L4019: V_{in} ($\overline{TEST}$, $R9_0$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 V to 0.3 V	
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Excluding pull-up MOS current and output buffer current (HD404019R, HD40L4019R) Excluding output buffer current (HD4074019, HD407L4019)

2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state, operation mode
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

3. The timer/counter operates with the fastest clock. Input/output current does not flow.
   - MCU in standby mode
   - Input/output in reset state
   - Serial interface: stop
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0 to D_3, R3 to R9: V_{CC}
   - D_4 to D_{15}, R0 to R2, RA_0, RA_1: V_{disp}

4. Excluding pull-down MOS current.

Input/Output Characteristics for Standard Pins

(HD404019R: V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD40L4019R: V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD4074019: V_{CC} = 4.5 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD407L4019: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	D_0 to D_3, R3 to R9	0.7 V_{CC}	—	V_{CC} + 0.3	V	HD404019R, HD4074019	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD40L4019R	
			0.7 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019	
Input low voltage	V_{IL}	D_0 to D_3, R3 to R9	–0.3	—	0.3 V_{CC}	V	HD404019R, HD4074019	
			–0.3	—	0.2 V_{CC}	V	HD40L4019R	
			–0.3	—	0.3 V_{CC}	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			–0.3	—	0.2 V_{CC}	V	HD407L4019	
Output high voltage	V_{OH}	D_0 to D_3, R3 to R8	V_{CC} – 1.0	—	—	V	HD404019R, HD40L4019R: $–I_{OH}$ = 1.0 mA	1
			V_{CC} – 0.5	—	—	V	HD404019R, HD40L4019R: $–I_{OH}$ = 0.5 mA	1
Output low voltage	V_{OL}	D_0 to D_3, R3 to R8	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_3, R3 to R9	—	—	1	µA	HD404019R, HD40L4019R: V_{in} = 0 V to V_{CC}	2
		D_0 to D_3, R3 to R8, $R9_1$ to $R9_3$	—	—	1	µA	HD4074019, HD407L4019: V_{in} = 0 V to V_{CC}	3
		$R9_0$	—	—	20	µA		
Pull-up MOS current	$–I_{PU}$	D_0 to D_3, R3 to R9	30	—	150	µA	HD404019R, HD40L4019R: V_{CC} = 5 V, V_{in} = 0 V	4

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Excluding pull-up MOS current and output buffer current.
3. Excluding output buffer current.
4. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins

(HD404019R: V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD40L4019R: V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD4074019: V_{CC} = 4.5 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD407L4019: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input high voltage	V_{IH}	D_4 to D_{15}, R0 to R2, RA_0, RA_1	0.7 V_{CC}	—	V_{CC} + 0.3	V	HD404019R, HD4074019	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	
			0.7 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			0.8 V_{CC}	—	V_{CC} + 0.3	V	HD407L4019	
Input low voltage	V_{IL}	D_4 to D_{15}, R0 to R2, RA_0, RA_1	V_{CC} – 40	—	0.3 V_{CC}	V	HD404019R, HD4074019	
			V_{CC} – 40	—	0.2 V_{CC}	V	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	
			V_{CC} – 40	—	0.3 V_{CC}	V	HD407L4019: V_{CC} = 4.5 V to 5.5 V	
			V_{CC} – 40	—	0.2 V_{CC}	V	HD407L4019	
Output high voltage	V_{OH}	D4 to D15	V_{CC} – 3.0	—	—	V	HD404019R, HD40L4019R: $-I_{OH}$ = 15 mA, V_{CC} = 5 V ± 20%	
			V_{CC} – 2.0	—	—	V	HD404019R, HD40L4019R: $-I_{OH}$ = 10 mA, V_{CC} = 5 V ± 20%	
			V_{CC} – 1.0	—	—	V	HD404019R, HD40L4019R: $-I_{OH}$ = 4 mA	
			V_{CC} – 3.0	—	—	V	HD4074019: $-I_{OH}$ = 15 mA	
			V_{CC} – 2.0	—	—	V	HD4074019: $-I_{OH}$ = 10 mA	
			V_{CC} – 1.0	—	—	V	HD4074019: $-I_{OH}$ = 4 mA	
			V_{CC} – 3.0	—	—	V	HD407L4019: $-I_{OH}$ = 15 mA, V_{CC} = 4.5 V to 5.5 V	
			V_{CC} – 2.0	—	—	V	HD407L4019: $-I_{OH}$ = 10 mA	
			V_{CC} – 1.0	—	—	V	HD407L4019: $-I_{OH}$ = 4 mA	

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Output high voltage	V_{OH}	R0 to R2	V_{CC} – 3.0	—	—	V	HD404019R, HD40L4019R: $-I_{OH}$ = 3 mA, V_{CC} = 5 V ± 20%	
			V_{CC} – 2.0	—	—	V	HD404019R, HD40L4019R: $-I_{OH}$ = 2 mA, V_{CC} = 5 V ± 20%	
			V_{CC} – 1.0	—	—	V	HD404019R, HD40L4019R: $-I_{OH}$ = 0.8 mA	
			V_{CC} – 3.0	—	—	V	HD4074019: $-I_{OH}$ = 3 mA	
			V_{CC} – 2.0	—	—	V	HD4074019: $-I_{OH}$ = 2 mA	
			V_{CC} – 1.0	—	—	V	HD4074019: $-I_{OH}$ = 0.8 mA	
			V_{CC} – 3.0	—	—	V	HD407L4019: $-I_{OH}$ = 3 mA, V_{CC} = 4.5 V to 5.5 V	
			V_{CC} – 2.0	—	—	V	HD407L4019: $-I_{OH}$ = 2 mA	
			V_{CC} – 1.0	—	—	V	HD407L4019: $-I_{OH}$ = 0.8 mA	
Output low voltage	V_{OL}	D_4 to D_{15}, R0 to R2	—	—	V_{CC} – 37	V	HD404019R, HD40L4019R: V_{disp} = V_{CC} – 40 V	1
			—	—	V_{CC} – 37	V	HD404019R, HD40L4019R: 150 kΩ at V_{CC} – 40 V	2
			—	—	V_{CC} – 37	V	HD4074019, HD407L4019: 150 kΩ at V_{CC} – 40 V	
Input/output leakage current	$\lvert I_{IL} \rvert$	D_4 to D_{15}, R0 to R2, RA_0, RA_1	—	—	20	µA	HD404019R, HD40L4019R: V_{in} = V_{CC} – 40 V to V_{CC}	3
			—	—	20	µA	HD4074019, HD407L4019: V_{in} = V_{CC} – 40 V to V_{CC}	4
Pull-down MOS current	I_{PD}	D_4 to D_{15}, R0 to R2, RA_0, RA_1	125	—	900	µA	HD404019R, HD40L4019R: V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-up MOS by mask option.
2. Applied to I/O pins selected as with pull-up MOS (PMOS open drain) by mask option.
3. Excluding pull-down MOS current and output buffer current.
4. Excluding output buffer current.

AC Characteristics

(HD404019R: V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD40L4019R: V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD4074019: V_{CC} = 4.5 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD407L4019: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	HD404019R: divide by 4	
			0.4	4	4.5	MHz	HD40L4019R: V_{CC} = 3.5 V to 6.0 V, divide by 4	
			0.4	—	3.58	MHz	HD40L4019R: divide by 4	
			0.2	4	4.5	MHz	HD4074019: divide by 4	
			0.2	4	4.5	MHz	HD407L4019: V_{CC} = 4.5 V to 5.5 V, divide by 4	
			0.2	—	3.58	MHz	HD407L4019	
Instruction cycle time	t_{cyc}		0.89	1	20	µs	HD404019R	
			0.89	1	10	µs	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	
			1.12	—	10	µs	HD40L4019R	
			0.89	1	20	µs	HD4074019: divide by 4	
			0.89	1	20	µs	HD407L4019: V_{CC} = 4.5 V to 5.5 V, divide by 4	
			1.12	—	20	µs	HD407L4019	
Oscillation stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms	HD404019R, HD4074019	1
			—	—	20	ms	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1
			—	—	40	ms	HD40L4019R	1
			—	—	20	ms	HD407L4019: V_{CC} = 4.5 V to 5.5 V	1
			—	—	40	ms	HD407L4019	1

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage (HD404019R/HD40L4019R: 3.5 V, HD4074019: 4.5 V, HD407L4019: 3.0 V (3.5 V when V_{CC} = 3.5 V to 6.0 V)) at power-on until when the oscillator stabilizes, or after RESET goes high by MCU reset to quit stop mode. At power-on or when recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. When using a crystal or ceramic oscillator, consult with the crystal oscillator manufacturer since the oscillator stabilization time depends on the circuit constants and stray capacitance. (See figure 26.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
External clock high width	t_{CPH}	OSC_1	92	—	—	ns	HD404019R, HD4074019: divide by 4	1
			92	—	—	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V, divide by 4	1
			120	—	—	ns	HD40L4019R: divide by 4	1
			92	—	—	ns	HD407L4019: V_{CC} = 4.5 V to 5.5 V, divide by 4	1
			115	—	—	ns	HD407L4019	1
External clock low width	t_{CPL}	OSC_1	92	—	—	ns	HD404019R, HD4074019: divide by 4	1
			92	—	—	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V, divide by 4	1
			120	—	—	ns	HD40L4019R: divide by 4	1
			92	—	—	ns	HD407L4019: V_{CC} = 4.5 V to 5.5 V, divide by 4	1
			115	—	—	ns	HD407L4019	1
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		1
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		1
$\overline{INT}_0$ high width	t_{IH}	$\overline{INT}_0$	2	—	—	t_{cyc}		2
$\overline{INT}_0$ low width	t_{IL}	$\overline{INT}_0$	2	—	—	t_{cyc}		2
$\overline{INT}_1$ high width	t_{IH}	$\overline{INT}_1$	2	—	—	t_{cyc}		2
$\overline{INT}_1$ low width	t_{IL}	$\overline{INT}_1$	2	—	—	t_{cyc}		2
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		3
Input capacitance	C_{in}	All pins	—	—	30	pF	HD404019R, HD40L4019R: f = 1 MHz, V_{in} = 0 V	
		All pins except $R9_0$	—	—	30	pF	HD4074019, HD407L4019: f = 1 MHz, V_{in} = 0 V	
		$R9_0$	—	—	180	pF		
RESET fall time	t_{RSTf}		—	—	20	ms		3

Notes: 1. See figure 26.
2. See figure 27.
3. See figure 28.

Serial Interface Timing Characteristics

(HD404019R: V_{CC} = 3.5 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD40L4019R: V_{CC} = 2.7 V to 6 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD4074019: V_{CC} = 4.5 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
HD407L4019: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, Ta = –20°C to +75°C
unless otherwise specified)

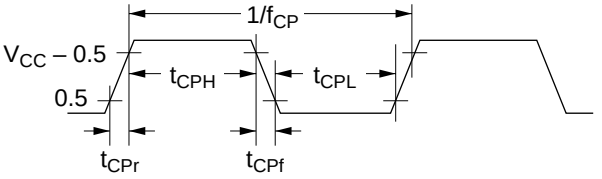
Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$ output	1	—	—	t_{cyc}	Load shown in figure 30	1, 2
Transmit clock high widths	t_{SCKH}	$\overline{SCK}$ output	0.4	—	—	t_{cyc}		1, 2
Transmit clock low widths	t_{SCKL}	$\overline{SCK}$ output	0.4	—	—	t_{cyc}		1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$ output	—	—	40	ns	HD404019R, HD4074019, HD407L4019	1, 2
			—	—	40	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1, 2
			—	—	200	ns	HD40L4019R	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$ output	—	—	40	ns	HD404019R, HD4074019, HD407L4019	1, 2
			—	—	40	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1, 2
			—	—	200	ns	HD40L4019R	1, 2
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$ input	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$ input	0.4	—	—	t_{cyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$ input	0.4	—	—	t_{cyc}		1
Transmit clock completion detect time	t_{SCKHD}	$\overline{SCK}$ input	1	—	—	t_{cyc}		3
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$ input	—	—	40	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$ input	—	—	40	ns		1

Notes: 1. See figure 29.
2. See figure 30.
3. Transmit clock completion detect time is the high level period after 8 pulses of transmit clock are input. The serial interrupt request flag is not set when the next transmit clock is input before the transmit clock completion detect time has passed.

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Notes
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	HD404019R	1, 2
			—	—	300	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1, 2
			—	—	500	ns	HD40L4019R	1, 2
			—	—	200	ns	HD4074019	1, 2
			—	—	200	ns	HD407L4019: V_{CC} = 4.5 V to 5.5 V	1, 2
			—	—	400	ns	HD407L4019	1, 2
Serial input data setup time	t_{SSI}	SI	100	—	—	ns	HD404019R	1
			100	—	—	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1
Serial input data setup time	t_{SSI}	SI	300	—	—	ns	HD40L4019R	1
			200	—	—	ns	HD4074019, HD407L4019	1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns	HD404019R	1
			200	—	—	ns	HD40L4019R: V_{CC} = 3.5 V to 6.0 V	1
			400	—	—	ns	HD40L4019R	1
			100	—	—	ns	HD4074019	1
			100	—	—	ns	HD407L4019: V_{CC} = 4.5 V to 5.5 V	1
			200	—	—	ns	HD407L4019	1

Notes: 1. See figure 29.
2. See figure 30.

HD404019R
HD4074019
HD407L4019



HD40L4019R

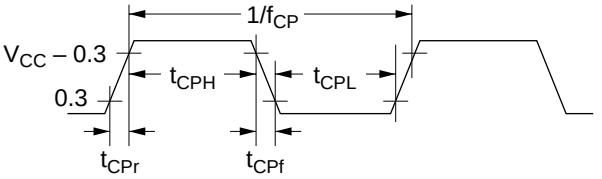
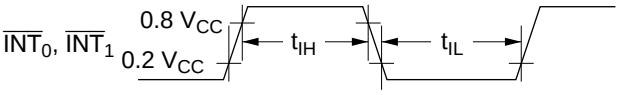


Figure 26 Oscillator Timing

HD404019R
HD4074019
HD407L4019 (V_{CC} = 4.5 V to 5.5 V)



HD40L4019R
HD407L4019 (V_{CC} = 3.0 V to 4.5 V)

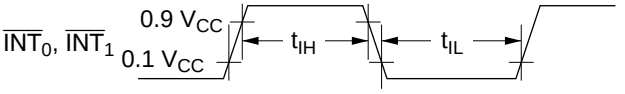
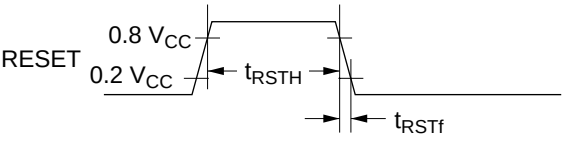


Figure 27 Interrupt Timing

HD404019R
HD4074019
HD407L4019 (V_{CC} = 4.5 V to 5.5 V)



HD40L4019R
HD407L4019 (V_{CC} = 3.0 V to 4.5 V)

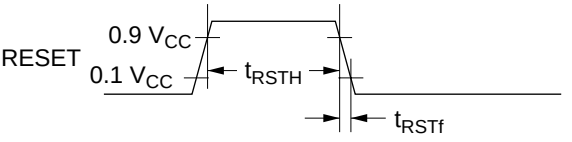
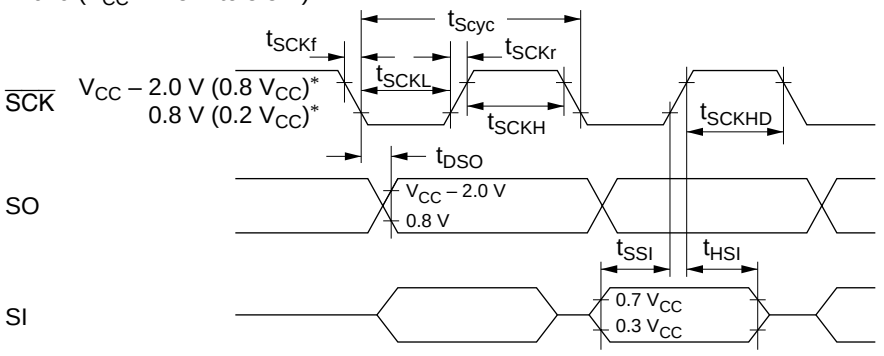


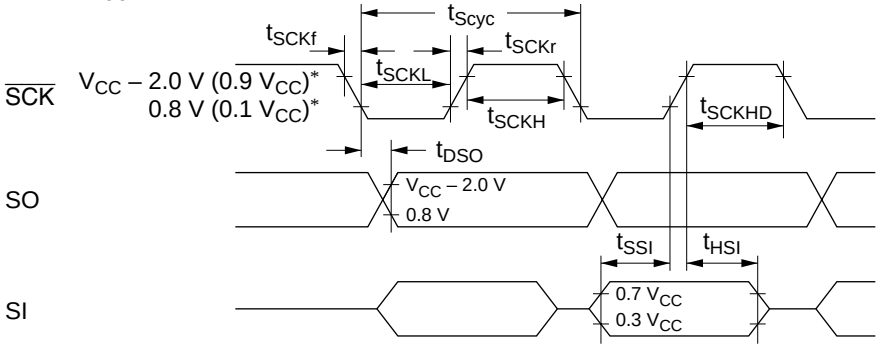
Figure 28 Reset Timing

HD404019R
HD4074019
HD407L4019 (V_{CC} = 4.5 V to 5.5 V)



Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
0.8 V_{CC} and 0.2 V_{CC} are the threshold voltages for transmit clock input.

HD40L4019R
HD407L4019 (V_{CC} = 3.0 V to 4.5 V)



Note: * V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
0.9 V_{CC} and 0.1 V_{CC} are the threshold voltages for transmit clock input.

Figure 29 Timing of Serial Interface

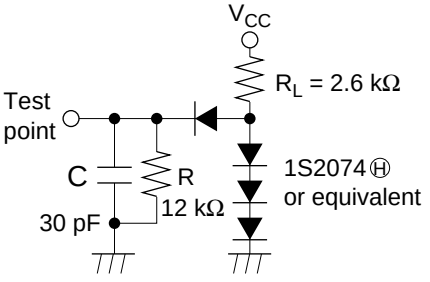


Figure 30 Timing Load Circuit

HD404019R Option List

Date of order	
Customer	
Dept.	
Name	
ROM code name	
LSI type number (Hitachi's entry)	

Please check off the appropriate applications and enter the necessary information.

☐ 5 V operation: HD404019R
☐ Low-voltage operation: HD40L4019R

1. I/O option

Note: I/O options masked by ▒ are not available.

Pin		I/O		I/O option					Pin		I/O		I/O option				
				A	B	C	D	E					A	B	C	D	E
D0		Standard pins	I/O				▒	▒	R3	R30	Standard pins	I/O				▒	▒
D1			I/O				▒	▒		R31		I/O				▒	▒
D2			I/O				▒	▒		R32		I/O				▒	▒
D3			I/O				▒	▒		R33		I/O				▒	▒
D4		High voltage pins	I/O	▒	▒	▒			R4	R40		I/O				▒	▒
D5			I/O	▒	▒	▒				R41		I/O				▒	▒
D6			I/O	▒	▒	▒				R42		I/O				▒	▒
D7			I/O	▒	▒	▒				R43		I/O				▒	▒
D8			I/O	▒	▒	▒			R5	R50		I/O				▒	▒
D9			I/O	▒	▒	▒				R51		I/O				▒	▒
D10			I/O	▒	▒	▒				R52		I/O				▒	▒
D11			I/O	▒	▒	▒				R53		I/O				▒	▒
D12			I/O	▒	▒	▒			R6	R60		I/O				▒	▒
D13			I/O	▒	▒	▒				R61		I/O				▒	▒
D14			I/O	▒	▒	▒				R62		I/O				▒	▒
D15			I/O	▒	▒	▒				R63		I/O				▒	▒
									R7	R70		I/O				▒	▒
										R71		I/O				▒	▒
R0	R00	High voltage pins	I/O	▒	▒	▒				R72		I/O				▒	▒
	R01		I/O	▒	▒	▒				R73		I/O				▒	▒
	R02		I/O	▒	▒	▒			R8	R80		I/O				▒	▒
	R03		I/O	▒	▒	▒				R81		I/O				▒	▒
R1	R10		I/O	▒	▒	▒				R82		I/O				▒	▒
	R11		I/O	▒	▒	▒				R83		I/O				▒	▒
	R12		I/O	▒	▒	▒			R9	R90		I			▒	▒	▒
	R13		I/O	▒	▒	▒				R91		I			▒	▒	▒
R2	R20		I/O	▒	▒	▒				R92		I			▒	▒	▒
	R21		I/O	▒	▒	▒				R93		I			▒	▒	▒
	R22		I/O	▒	▒	▒			RA	RA0	High voltage pins	I	▒	▒	▒		
	R23		I/O	▒	▒	▒				RA1		I	Please mark on RA1/Vdisp				

A: Without pull-up MOS (NMOS open drain)
B: With pull-up MOS
C: CMOS (not be used as input)
D: Without pull-down MOS (PMOS open drain)
E: With pull-down MOS

HD404019R Option List

2. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

3. Divider (DIV)

■ Divide by 4

4. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. System oscillator (OSC1 and OSC2)

☐ Ceramic oscillator
☐ Crystal oscillator
☐ External clock

6. Stop mode

☐ Used
☐ Not used

7. Package

HD404019R	HD40L4019R
☐ DP-64S	☐ DP-64S
☐ FP-64A	☐ FP-64A
☐ FP-64B	

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Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia (Singapore) : http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
Asia (HongKong) : http://www.hitachi.com.hk/eng/bo/grp3/index.htm
Japan : http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX