

# 2SK2728

Silicon N Channel MOS FET  
High Speed Power Switching

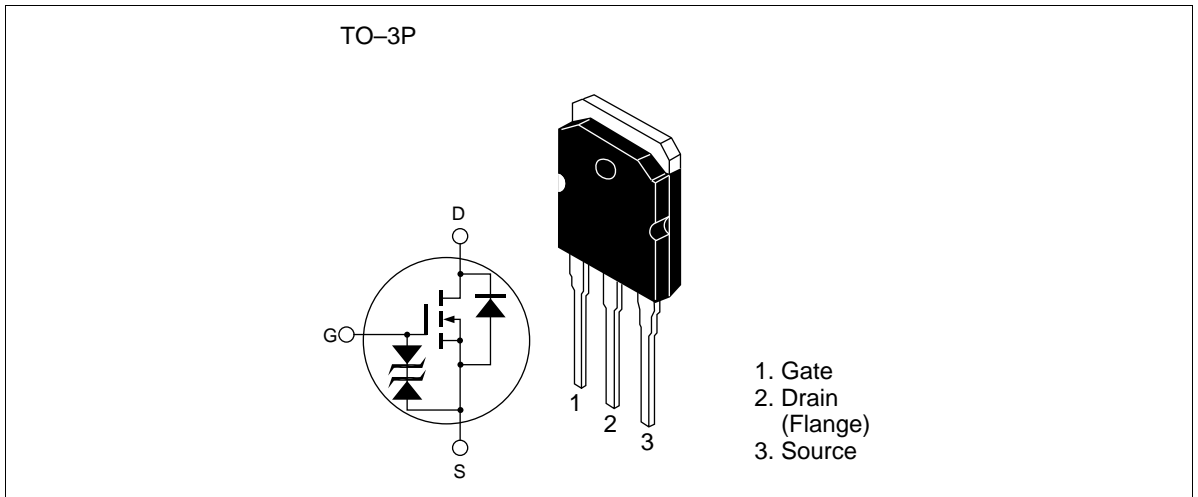
# HITACHI

ADE-208-454 B  
3rd. Edition

## Features

- Low on-resistance
- High speed switching
- Low drive current
- Avalanche ratings

## Outline



**Absolute Maximum Ratings** ( $T_a = 25^\circ\text{C}$ )

<b>Item</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>
Drain to source voltage	$V_{DSS}$	500	V
Gate to source voltage	$V_{GSS}$	$\pm 30$	V
Drain current	$I_D$	18	A
Drain peak current	$I_{D(pulse)}^{*1}$	72	A
Body to drain diode reverse drain current	$I_{DR}$	18	A
Avalanche current	$I_{AP}^{*3}$	18	A
Avalanche energy	$E_{AR}^{*3}$	18	mJ
Channel dissipation	$Pch^{*2}$	150	W
Channel temperature	Tch	150	$^\circ\text{C}$
Storage temperature	Tstg	-55 to +150	$^\circ\text{C}$

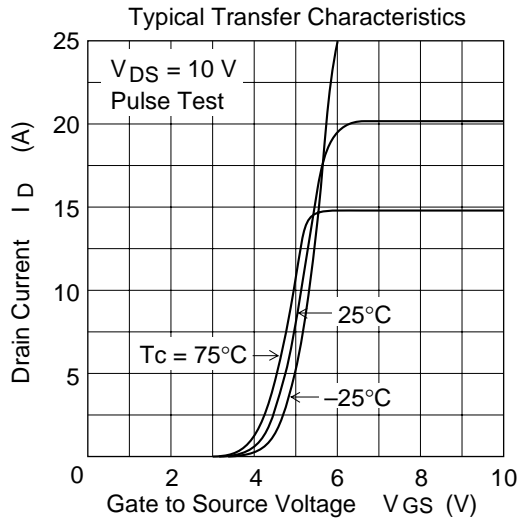
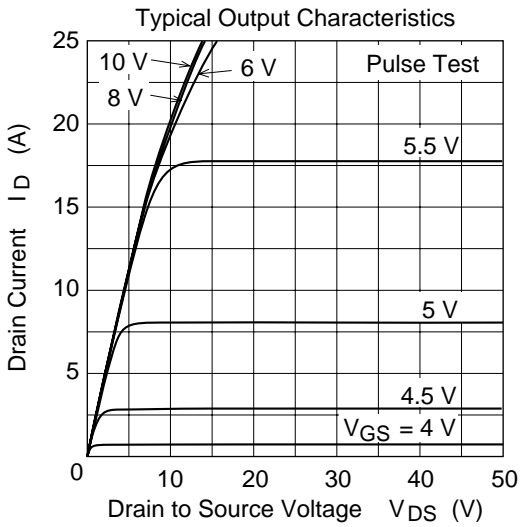
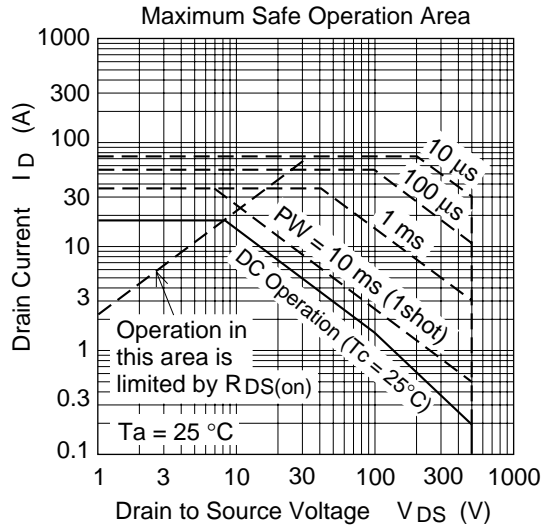
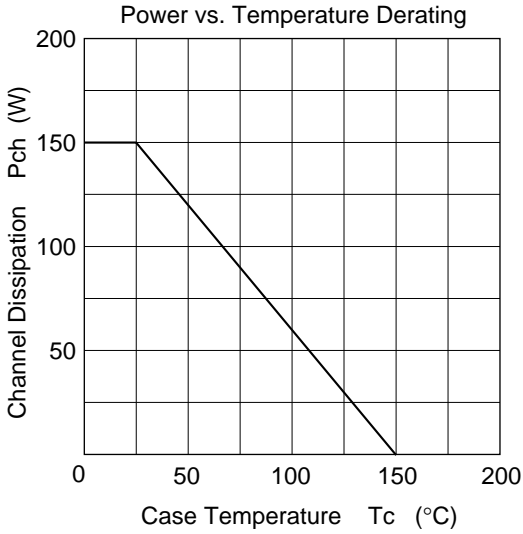
- Notes: 1.  $PW \leq 10\mu\text{s}$ , duty cycle  $\leq 1\%$   
2. Value at  $T_c = 25^\circ\text{C}$   
3. Value at  $Tch = 25^\circ\text{C}$ ,  $R_g \geq 50\Omega$

## Electrical Characteristics (Ta = 25°C)

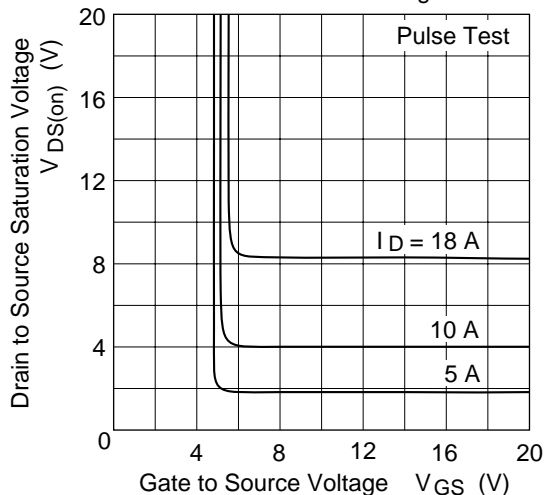
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10\text{mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 30$	—	—	V	$I_G = \pm 100\mu\text{A}, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 25\text{V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 500\text{V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.5	—	3.5	V	$I_D = 1\text{mA}, V_{DS} = 10\text{V}^{*1}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.38	0.45	$\Omega$	$I_D = 9\text{A}, V_{GS} = 10\text{V}^{*1}$
Forward transfer admittance	$ y_{fs} $	8	13	—	S	$I_D = 9\text{A}, V_{DS} = 10\text{V}^{*1}$
Input capacitance	$C_{iss}$	—	2150	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	$C_{oss}$	—	630	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	100	—	pF	$f = 1\text{MHz}$
Total gate charge	$Q_g$	—	38	—	nc	$V_{DD} = 400\text{V}$
Gate to source charge	$Q_{gs}$	—	10	—	nc	$V_{GS} = 10\text{V}$
Gate to drain charge	$Q_{gd}$	—	13	—	nc	$I_D = 18\text{A}$
Turn-on delay time	$t_{d(on)}$	—	35	—	ns	$V_{GS} = 10\text{V}, I_D = 9\text{A}$
Rise time	$t_r$	—	120	—	ns	$R_L = 3.3\Omega$
Turn-off delay time	$t_{d(off)}$	—	100	—	ns	
Fall time	$t_f$	—	65	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	1.0	—	V	$I_D = 18\text{A}, V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	380	—	ns	$I_F = 18\text{A}, V_{GS} = 0$ $di_F/dt = 100\text{A}/\mu\text{s}$

Note: 1. Pulse test

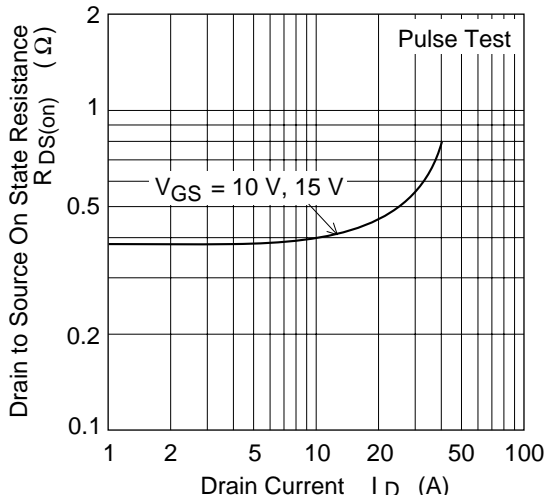
Main Characteristics



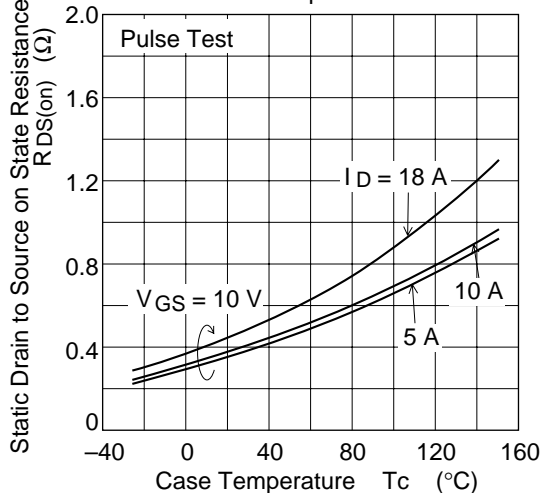
Drain to Source Saturation Voltage vs. Gate to Source Voltage



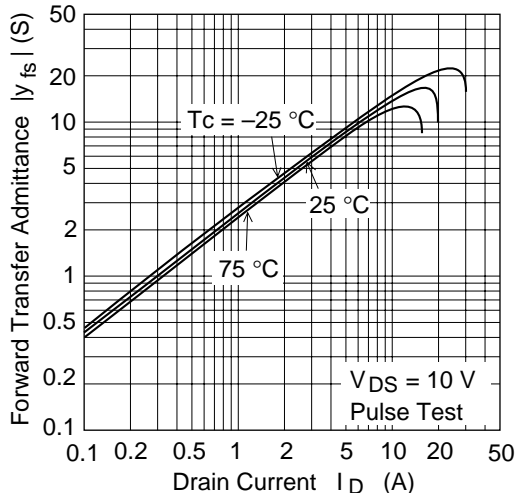
Static Drain to Source on State Resistance vs. Drain Current



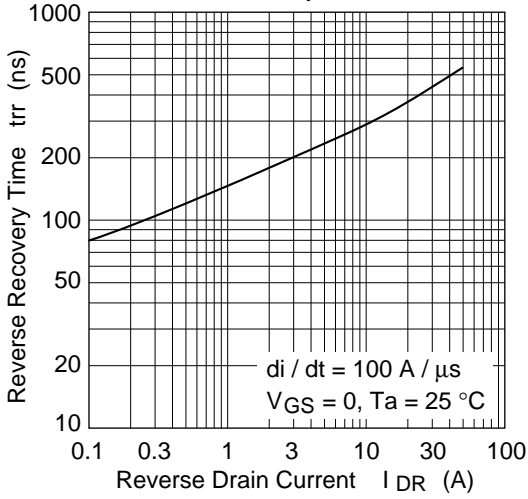
Static Drain to Source on State Resistance vs. Temperature



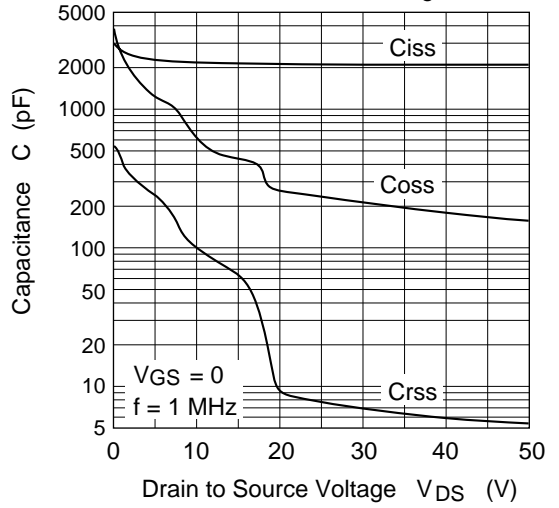
Forward Transfer Admittance vs. Drain Current



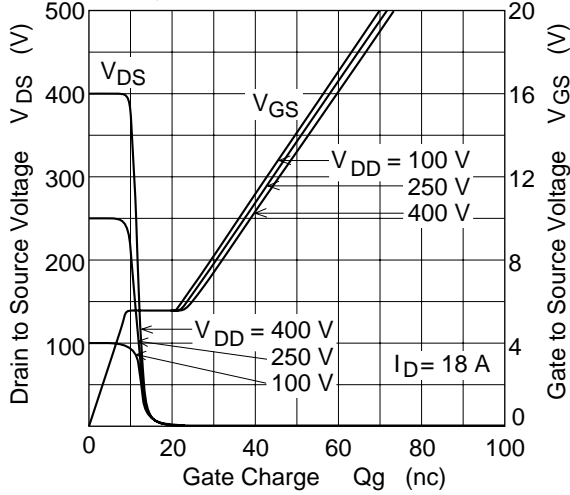
Body to Drain Diode Reverse Recovery Time



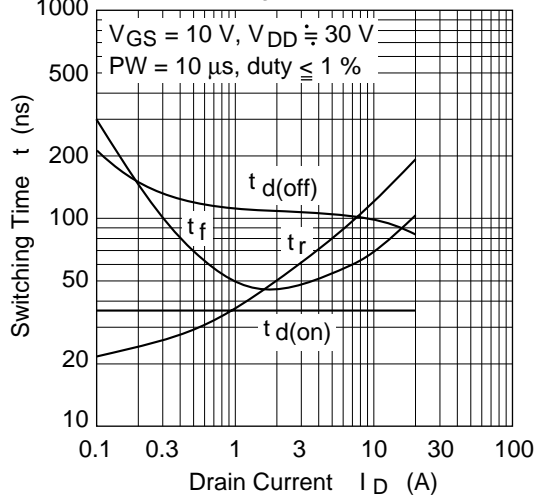
Typical Capacitance vs. Drain to Source Voltage



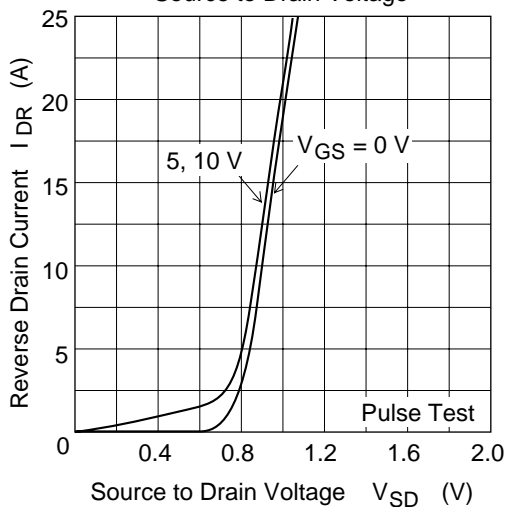
Dynamic Input Characteristics



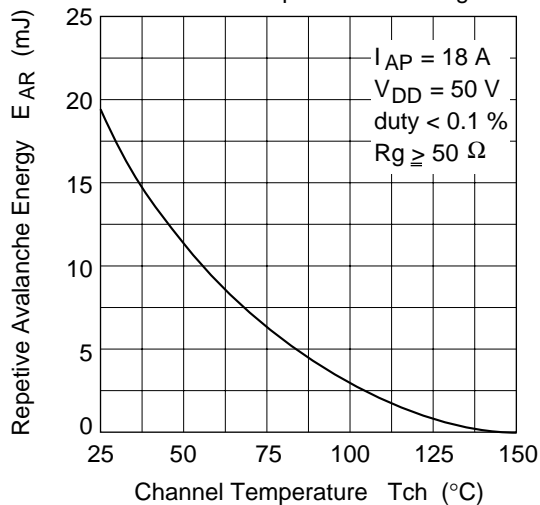
Switching Characteristics



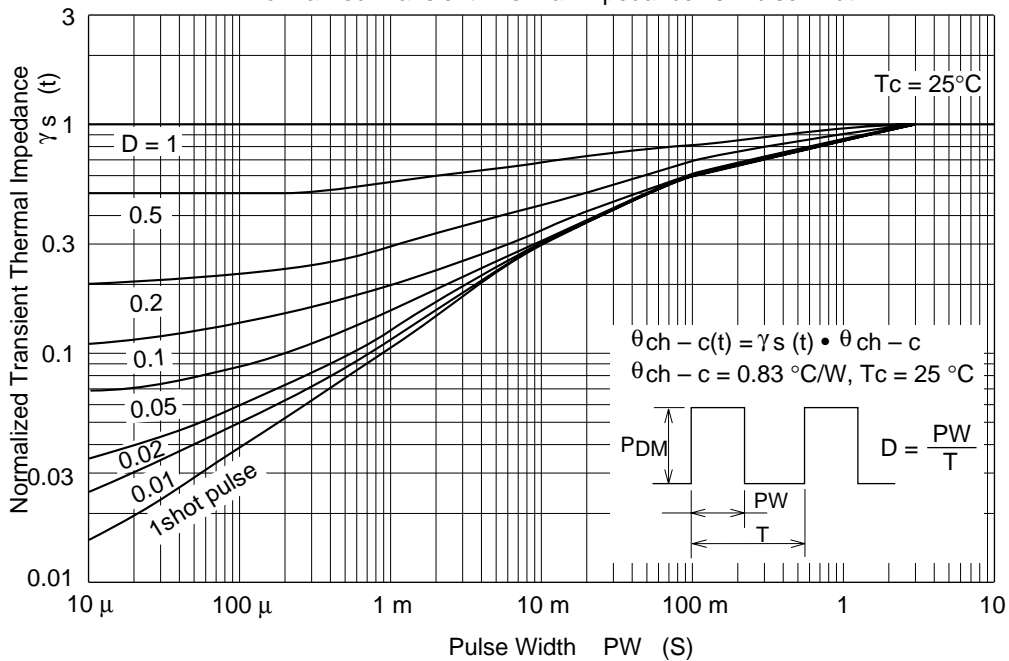
Reverse Drain Current vs. Source to Drain Voltage



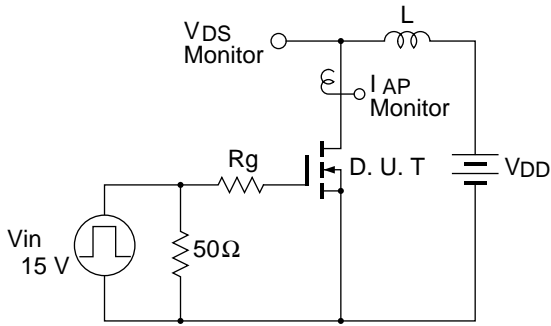
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

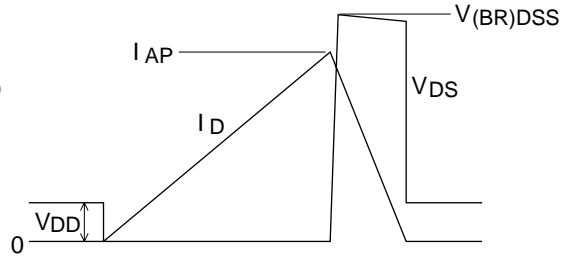


Avalanche Test Circuit

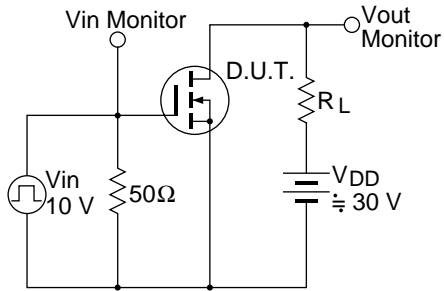


Avalanche Waveform

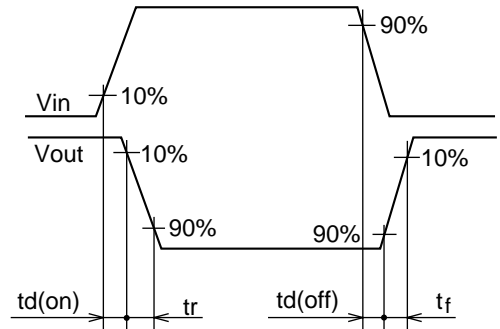
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



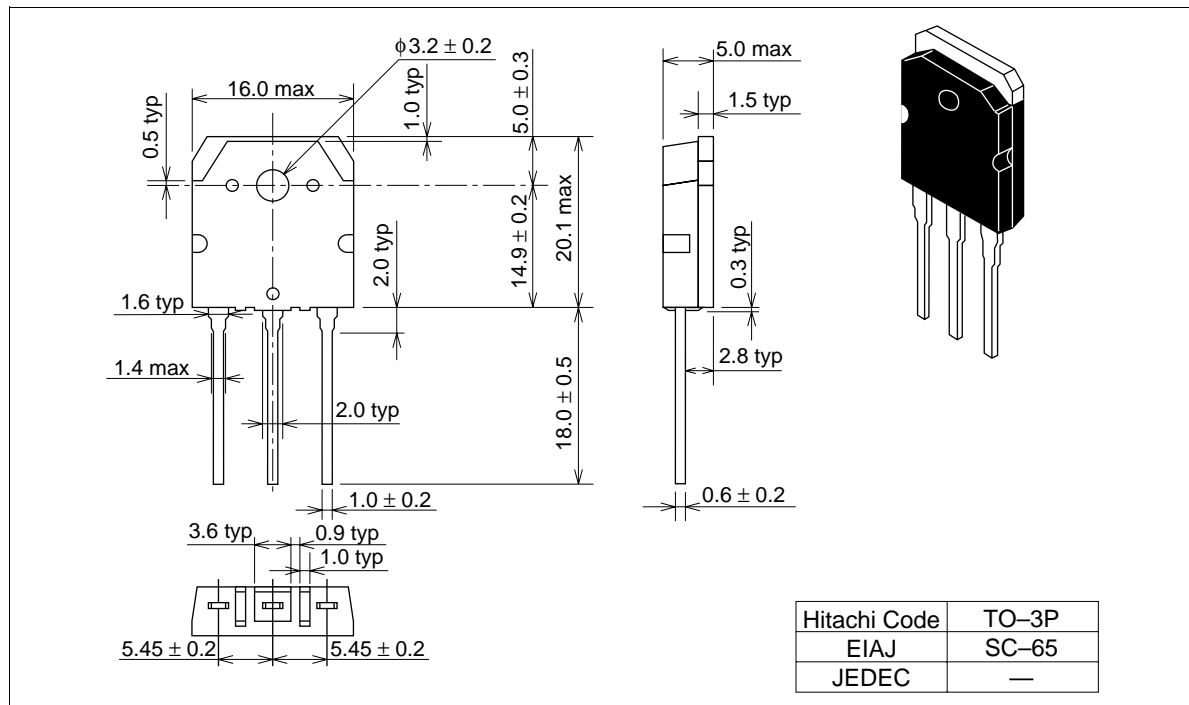
Switching Time Waveform





## Package Dimensions

Unit: mm



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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL North America : <http://semiconductor.hitachi.com/>  
Europe : <http://www.hitachi-eu.com/hel/ecg>  
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## For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic components Group  
Dornacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 049318  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia Ltd.  
Taipei Branch Office  
3F, Hung Kuo Building, No.167,  
Tun-Hwa North Road, Taipei (105)  
Tel: <886> (2) 2718-3666  
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower, World Finance Centre,  
Harbour City, Canton Road, Tsim Sha Tsui,  
Kowloon, Hong Kong  
Tel: <852> (2) 735 9218  
Fax: <852> (2) 730 0281  
Telex: 40815 HITEC HX

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