M37920S4CGP

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37920S4CGP is a single-chip microcomputers designed with high-performance CMOS silicon gate technology. These are housed in 100-pin plastic molded QFP. This microcomputer supports the 7900 Series instruction set, which are enhanced and expanded instruction set and are upper-compatible with the 7700/7751 Series instruction set.

The CPU of this microcomputer is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. Also, the bus interface unit of this microcomputer enhance the memory access efficiency to execute instructions fast. This microcomputer include the 4-channel DMA controller and the DRAM controller with enhanced fast page mode. Therefore, this microcomputer are suitable for office, business, and industrial equipment controller that require fast processing of large data.

DISTINCTIVE FEATURES

<Microcomputer mode>

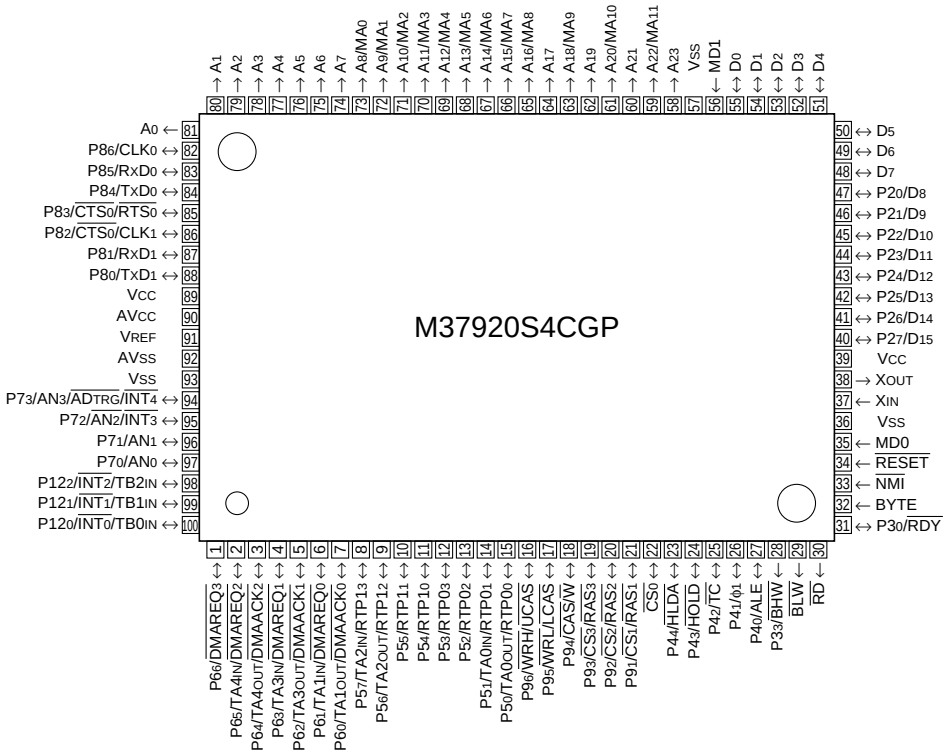
- Number of basic machine instructions 203
- Memory
  RAM .....2048 bytes
  ROM ..... External
- Instruction execution time
  The fastest instruction at 20 MHz frequency ..... 50 ns
- Single power supply ..... 5 V ± 0.5 V
- Interrupts ..... 6 external sources, 17 internal sources, 7 levels
- Multi-functional 16-bit timer ..... 5 + 3
- Serial I/O (UART or Clock synchronous) 2
- 10-bit A-D converter ..... 4-channel inputs
- DMA controller 4-channels
- DRAM controller
- Real-time output
  .... 4 bits × 2 channels, or 6 bits × 1 channel + 2 bits × 1 channel
- 12-bit watchdog timer
- Programmable input/output (ports P2–P9, P12) 49

APPLICATION

Telecommunications equipment such as copiers, printers, typewriters, facsimiles, optical disk drives, HDD, mobile radio communication equipment, ISDN terminals

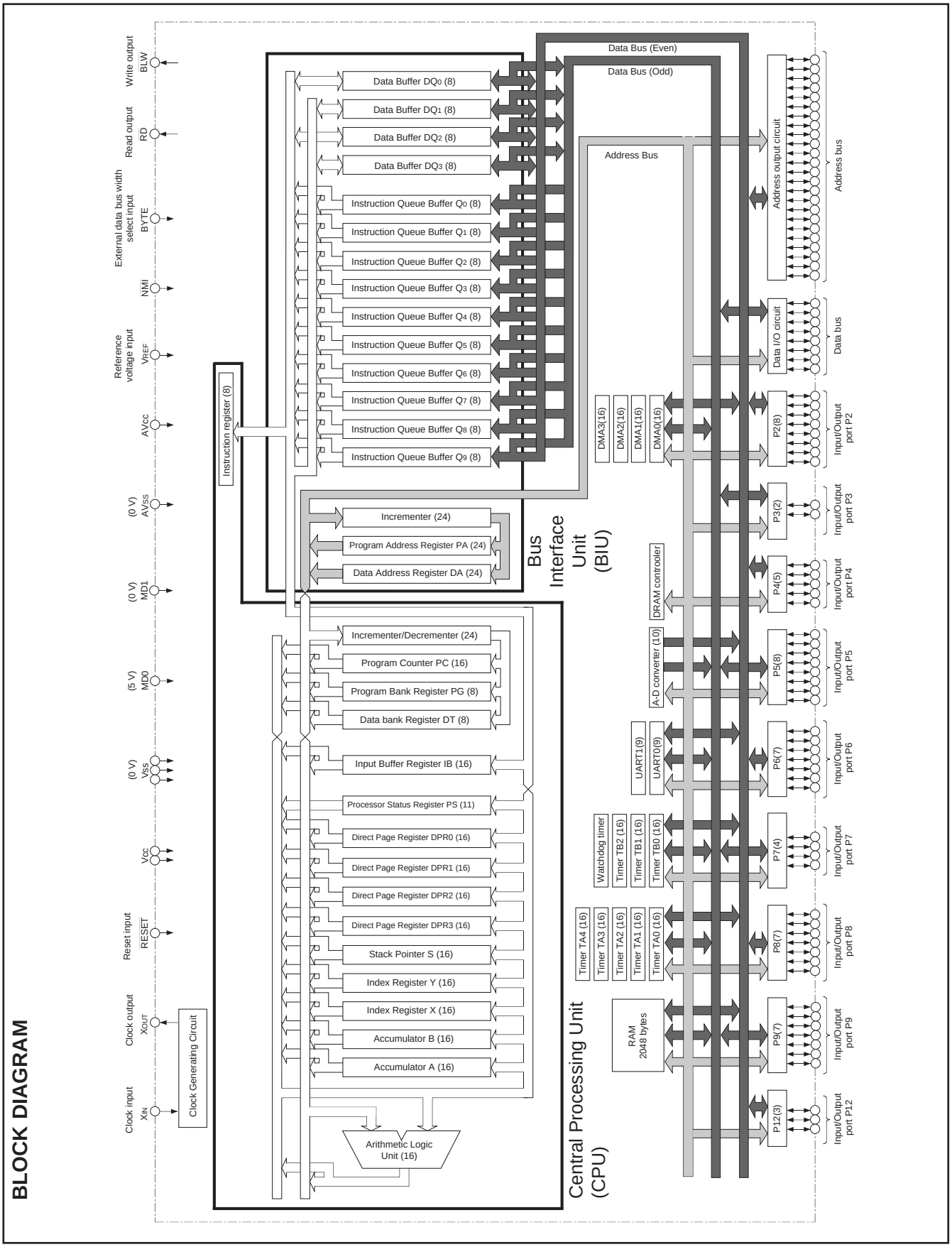
Control devices for office automation equipment such as personal computers

M37920S4CGP PIN CONFIGURATION (TOP VIEW)



Outline 100P6S-A

BLOCK DIAGRAM



FUNCTIONS (Microcomputer mode)

Parameter		Functions
Number of basic machine instructions		203
Instruction execution time		50 ns (the fastest instruction at f(XIN) = 20 MHz)
External clock input frequency f(XIN)		20 MHz (Max.)
Memory size	ROM	External
	RAM	2048 bytes
Programmable input/output ports	P2, P5	8-bit × 2
	P3	2-bit × 1
	P4	5-bit × 1
	P6, P8	7-bit × 2
	P7	4-bit × 1
	P9	6-bit × 1
	P12	3-bit × 1
Multi-functional timers	TA0–TA4	16-bit × 5
	TB0–TB2	16-bit × 3
Serial I/O	UART0 and UART1	(UART or Clock synchronous serial I/O) × 2
A-D converter		10-bit successive approximation method × 1 (4 channels)
Watchdog timer		12-bit × 1
DMA controller		4 channels Maximum transfer rate 20 Mbytes/sec. (at f(XIN) = 20 MHz, 0 wait, 1-bus cycle transfer) 10 Mbytes/sec. (at f(XIN) = 20 MHz, 0 wait, 2-bus cycles transfer)
DRAM controller		1 channel Supports fast page access mode. Incorporates 8-bit refresh timer. Supports $\overline{CAS}$ before $\overline{RAS}$ refresh method or self refresh method.
Chip-select wait control		Chip select area × 4 ($\overline{CS0}$–$\overline{CS3}$). A wait number and bus width can be set for each chip select area.
Real-time output		4 bits × 2 channels; or 6 bits × 1 channel + 2 bits × 1 channel
Interrupts		6 external types, 17 internal types. Each interrupt except $\overline{NMI}$ can be set to a priority level within the range of 0–7 by software.
Clock generating circuit		Built-in (externally connected to a ceramic resonator or quartz crystal resonator).
Power supply voltage		5 V±10 %
Power dissipation		135 mW (at f(XIN) = 20 MHz, typ.)
Ports' input/output characteristics	Input/Output withstand voltage	5 V
	Output current	5 mA
Memory expansion		Up to 16 Mbytes. Note that bank FF16 is a reserved area.
Operating temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		100-pin plastic molded QFP

PIN DESCRIPTION (Microcomputer mode)

Pin	Name	Input/ Output	Functions
Vcc, Vss	Power supply input	—	Apply 5 V±10 % to Vcc, and 0 V to Vss.
MD0	MD0	Input	This pin controls the processor mode. Connect this pin to VCC.
MD1	MD1	Input	Connect this pin to Vss.
$\overline{\text{RESET}}$	Reset input	Input	The microcomputer is reset when “L” level is applies to this pin.
XIN	Clock input	Input	These are input and output pins of the internal clock generating circuit. Connect a ceramic or quartz- crystal resonator between the XIN and XOUT pins. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
BYTE	External data bus width select input	Input	This pin determines whether the external data bus has an 8-bit width or 16-bit width for the memory expansion mode or microprocessor mode. The width is 16 bits when “L” signal is input, and 8 bits when “H” signal is input.
AVcc, AVss	Analog power supply input	—	Power supply input pin for the A-D converter. Connect AVcc to Vcc, and AVss to Vss externally.
VREF	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
A_0–A_7	Low-order address	Output	The low-order 8 bits of address (A_0–A_7) are output.
A_8–A_{15}/ MA_0–MA_7	Middle-order address/ DRAM address	Output	The middle-order 8 bits of address (A_8–A_{15}) are input/output. While DRAM space is accessed, multiplexed address (MA_0–MA_7) is output.
A_{16}–A_{23}/ MA_8–MA_{11}	High-order address/ DRAM address	Output	The high-order 8 bits of address (A_{16}–A_{23}) are output. While DRAM space is accessed, multiplexed address (MA_8–MA_{11}) is output.
D_0–D_7	Low-order data	I/O	The low-order 8 bits of data (D_0–D_7) are input/output.
$P2_0/D_8$– $P2_7/D_{15}$	I/O port P2/ High-order data	I/O	■ When 8-bit external data bus is used (BYTE = “H” level) Port P2 is an 8-bit I/O port. ■ When 16-bit external data bus is used (BYTE = “L” level) The high-order 8 bits (D_8–D_{15}) are input/output.
$P3_0/\overline{\text{RDY}}$, $\overline{\text{RD}}$, $\overline{\text{BLW}}$, $P3_3/\overline{\text{BHW}}$	Memory control signal I/O	Input Output Output Output	While the input level at pin $\overline{\text{RDY}}$ is “L”, the microcomputer is placed in the ready state. While pin $\overline{\text{RD}}$ is at “L” level, the microcomputer reads out data and instruction codes. Also, pin $\overline{\text{RDY}}$ can function as a programmable I/O port pin ($P3_0$) by software. ■ When 8-bit external data bus is used (BYTE = “H” level) While pin $\overline{\text{BLW}}$ is at “L” level, the microcomputer writes data. ■ When 16-bit external data bus is used (BYTE = “L” level) While pin $\overline{\text{BLW}}$ is at “L” level, the microcomputer writes data into an even-numbered address. While pin $\overline{\text{BHW}}$ is at “L” level, the microcomputer writes data into an odd-numbered address.
$P4_0$/ALE, $P4_1/\phi_1$, $P4_2/\overline{\text{TC}}$, $P4_3/\overline{\text{HOLD}}$, $P4_4/\overline{\text{HLDA}}$	I/O port P4	Output Output I/O Input Output	Signal ALE is used to latch an address. ϕ_1 has the same period as internal clock ϕ. Pin $P4_2$ functions as a programmable I/O port pin. While the input level at pin $\overline{\text{HOLD}}$ is at “L” level, the microcomputer is placed in the hold state. Signal $\overline{\text{HLDA}}$ is used to inform the external that the microcomputer enters the hold state. By software, pin ALE, clock ϕ_1 output pin, and pins $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ function as programmable I/O port pins ($P4_0$, $P4_1$, $P4_3$, $P4_4$). Pin $P4_2$ also functions as pin $\overline{\text{TC}}$.
$P5_0$–$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port. These pins also function as I/O pins for timers A0, A2, and pulse output pins for the real-time output.
$P6_0$–$P6_6$	I/O port P6	I/O	Port P6 is a 7-bit I/O port. These pins also function as I/O pins for timers A1, A3, A4, input pins for DMA requests, and output pins for DMA acknowledge signals.

Pin	Name	Input/ Output	Functions
$P7_0$–$P7_3$	I/O port P7	I/O	Port P7 is a 4-bit I/O port. $P7_2$ and $P7_3$ also function as input pins for $\overline{INT_3}$ and $\overline{INT_4}$. According to the software setting, these pins also function as input pins for the A-D converter.
$P8_0$–$P8_6$	I/O port P8	I/O	Port P8 is a 7-bit I/O port. These pins also function as I/O pins for UART0, UART1.
$\overline{CS_0}$	Chip-select output	Output	This is an output pin for $\overline{CS_0}$.
$P9_1$–$P9_6$	I/O port P9	I/O	Port P9 is a 6-bit I/O port. According to the software setting, $P9_1$–$P9_3$ also funtion as chip select output pins. While DRAM space is selected, $P9_4$–$P9_6$ function as output pins for DRAM control signals.
$P12_0$–$P12_2$	I/O port P12	I/O	Port P12 is a 3-bit I/O port. These pins also functions as input pins for $\overline{INT_0}$, $\overline{INT_1}$, $\overline{INT_2}$. According to software setting, these pins also function as input pins for timers B0–B2.
$\overline{NMI}$	Non-maskable interrupt	Input	This pin is for a non-maskable interrupt.

BASIC FUNCTION BLOCKS

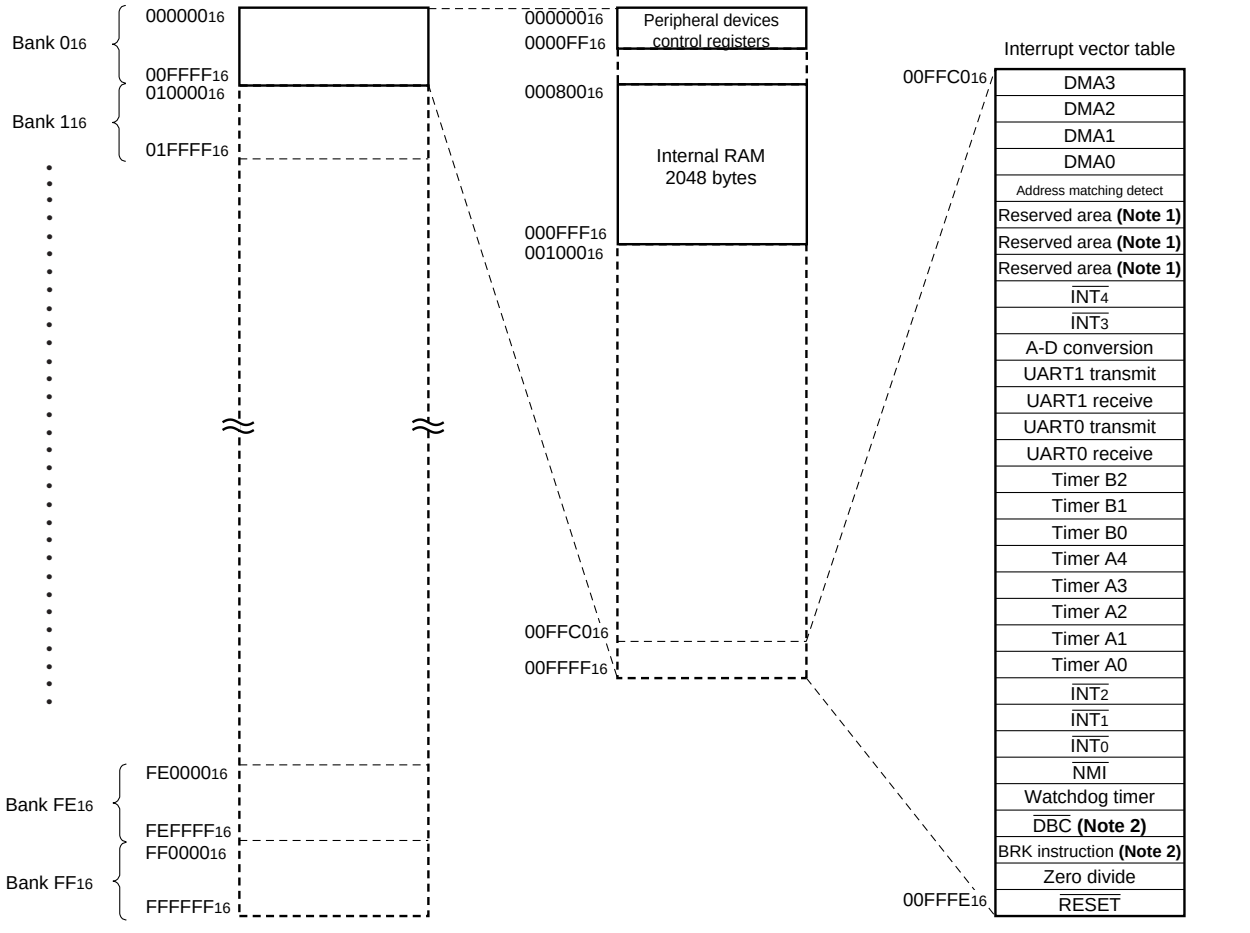
The M37920S4CGP is the same functions as the M37920F8CGP except for the following.

Therefore, refer to the datasheet of the M37920F8CGP.

- The M37920S4CGP does not include the internal flash memory.
- The M37920S4CGP operates only in the microprocessor mode.
- The M37920S4CGP does not have the flash memory control register (address $9E_{16}$).
- Some of programmable I/O ports of the M37920S4CGP differ from those of the M37920FGCGP.

MEMORY

Figure 1 shows the memory map.



Notes 1: Do not write to this address.
2: These are interrupts used only for debugging. Do not use these interrupts.

Fig. 1 Memory map

Address (Hexadecimal notation)	
000000₁₆	Reserved area **(Note 1)**
000001₁₆	Reserved area **(Note 1)**
000002₁₆	[Port P0 register] **(Note 2)**
000003₁₆	[Port P1 register] **(Note 2)**
000004₁₆	[Port P0 direction register] **(Note 2)**
000005₁₆	[Port P1 direction register] **(Note 2)**
000006₁₆	Port P2 register
000007₁₆	Port P3 register
000008₁₆	Port P2 direction register
000009₁₆	Port P3 direction register
00000A₁₆	Port P4 register
00000B₁₆	Port P5 register
00000C₁₆	Port P4 direction register
00000D₁₆	Port P5 direction register
00000E₁₆	Port P6 register
00000F₁₆	Port P7 register
000010₁₆	Port P6 direction register
000011₁₆	Port P7 direction register
000012₁₆	Port P8 register
000013₁₆	Port P9 register
000014₁₆	Port P8 direction register
000015₁₆	Port P9 direction register
000016₁₆	[Port P10 register] **(Note 2)**
000017₁₆	[Port P11 register] **(Note 2)**
000018₁₆	[Port P10 direction register] **(Note 2)**
000019₁₆	[Port P11 direction register] **(Note 2)**
00001A₁₆	Port P12 register
00001B₁₆	
00001C₁₆	Port P12 direction register
00001D₁₆	
00001E₁₆	A-D control register 0
00001F₁₆	A-D control register 1
000020₁₆ 000021₁₆	A-D register 0
000022₁₆ 000023₁₆	A-D register 1
000024₁₆ 000025₁₆	A-D register 2
000026₁₆ 000027₁₆	A-D register 3
000028₁₆ 000029₁₆	
00002A₁₆ 00002B₁₆	
00002C₁₆ 00002D₁₆	
00002E₁₆ 00002F₁₆	
000030₁₆	UART0 transmit/receive mode register
000031₁₆	UART0 baud rate register (BRG0)
000032₁₆ 000033₁₆	UART0 transmit buffer register
000034₁₆	UART0 transmit/receive control register 0
000035₁₆	UART0 transmit/receive control register 1
000036₁₆ 000037₁₆	UART0 receive buffer register
000038₁₆	UART1 transmit/receive mode register
000039₁₆	UART1 baud rate register (BRG1)
00003A₁₆ 00003B₁₆	UART1 transmit buffer register
00003C₁₆	UART1 transmit/receive control register 0
00003D₁₆	UART1 transmit/receive control register 1
00003E₁₆ 00003F₁₆	UART1 receive buffer register

Address (Hexadecimal notation)	
000040₁₆	Count start register
000041₁₆	
000042₁₆	One-shot start register
000043₁₆	
000044₁₆	Up-down register
000045₁₆	Timer A clock division select register
000046₁₆ 000047₁₆	Timer A0 register
000048₁₆ 000049₁₆	Timer A1 register
00004A₁₆ 00004B₁₆	Timer A2 register
00004C₁₆ 00004D₁₆	Timer A3 register
00004E₁₆ 00004F₁₆	Timer A4 register
000050₁₆ 000051₁₆	Timer B0 register
000052₁₆ 000053₁₆	Timer B1 register
000054₁₆ 000055₁₆	Timer B2 register
000056₁₆	Timer A0 mode register
000057₁₆	Timer A1 mode register
000058₁₆	Timer A2 mode register
000059₁₆	Timer A3 mode register
00005A₁₆	Timer A4 mode register
00005B₁₆	Timer B0 mode register
00005C₁₆	Timer B1 mode register
00005D₁₆	Timer B2 mode register
00005E₁₆	Processor mode register 0
00005F₁₆	Processor mode register 1
000060₁₆	Watchdog timer register
000061₁₆	Watchdog timer frequency select register
000062₁₆	Particular function select register 0
000063₁₆	Particular function select register 1
000064₁₆	Particular function select register 2
000065₁₆	Reserved area **(Note 1)**
000066₁₆	Debug control register 0
000067₁₆	Debug control register 1
000068₁₆ 000069₁₆ 00006A₁₆	Address comparison register 0
00006B₁₆ 00006C₁₆ 00006D₁₆	Address comparison register 1
00006E₁₆	$\overline{INT_3}$ interrupt control register
00006F₁₆	$\overline{INT_4}$ interrupt control register
000070₁₆	A-D conversion interrupt control register
000071₁₆	UART0 transmit interrupt control register
000072₁₆	UART0 receive interrupt control register
000073₁₆	UART1 transmit interrupt control register
000074₁₆	UART1 receive interrupt control register
000075₁₆	Timer A0 interrupt control register
000076₁₆	Timer A1 interrupt control register
000077₁₆	Timer A2 interrupt control register
000078₁₆	Timer A3 interrupt control register
000079₁₆	Timer A4 interrupt control register
00007A₁₆	Timer B0 interrupt control register
00007B₁₆	Timer B1 interrupt control register
00007C₁₆	Timer B2 interrupt control register
00007D₁₆	$\overline{INT_0}$ interrupt control register
00007E₁₆	$\overline{INT_1}$ interrupt control register
00007F₁₆	$\overline{INT_2}$ interrupt control register

Notes 1: Do not read/write to this address.
2: These registers are used in the bus fixation of the power saving function. For details, refer to the section on the power saving function of the M37920F8CGP datasheet.

Fig. 2 Location of peripheral devices' control registers (1)

Address (Hexadecimal notation)	
000080₁₆	$\overline{CS_0}$ control register L
000081₁₆	$\overline{CS_0}$ control register H
000082₁₆	$\overline{CS_1}$ control register L
000083₁₆	$\overline{CS_1}$ control register H
000084₁₆	$\overline{CS_2}$ control register L
000085₁₆	$\overline{CS_2}$ control register H
000086₁₆	$\overline{CS_3}$ control register L
000087₁₆	$\overline{CS_3}$ control register H
000088₁₆	
000089₁₆	
00008A₁₆	Area $\overline{CS_0}$ start address register
00008B₁₆	
00008C₁₆	Area $\overline{CS_1}$ start address register
00008D₁₆	
00008E₁₆	Area $\overline{CS_2}$ start address register
00008F₁₆	
000090₁₆	Area $\overline{CS_3}$ start address register
000091₁₆	
000092₁₆	
000093₁₆	
000094₁₆	
000095₁₆	
000096₁₆	
000097₁₆	
000098₁₆	
000099₁₆	
00009A₁₆	
00009B₁₆	
00009C₁₆	Reserved area **(Note 1)**
00009D₁₆	Reserved area **(Note 1)**
00009E₁₆	Reserved area **(Note 1)**
00009F₁₆	
0000A0₁₆	Real-time output control register
0000A1₁₆	
0000A2₁₆	Pulse output data register 0
0000A3₁₆	
0000A4₁₆	Pulse output data register 1
0000A5₁₆	
0000A6₁₆	Reserved area **(Note 1)**
0000A7₁₆	
0000A8₁₆	DRAM control register
0000A9₁₆	Refresh timer
0000AA₁₆	
0000AB₁₆	
0000AC₁₆	$\overline{CTS}/\overline{RTS}$ separate select register
0000AD₁₆	
0000AE₁₆	
0000AF₁₆	
0000B0₁₆	DMAC control register L
0000B1₁₆	DMAC control register H
0000B2₁₆	DMA0 interruput control register
0000B3₁₆	DMA1 interruput control register
0000B4₁₆	DMA2 interruput control register
0000B5₁₆	DMA3 interruput control register
0000B6₁₆	
0000B7₁₆	
0000B8₁₆	
0000B9₁₆	
0000BA₁₆	
0000BB₁₆	
0000BC₁₆	Reserved area **(Note 1)**
0000BD₁₆	Reserved area **(Note 1)**
0000BE₁₆	Reserved area **(Note 1)**
0000BF₁₆	Reserved area **(Note 1)**

Address (Hexadecimal notation)	
0000C0₁₆	Source address register 0 L
0000C1₁₆	Source address register 0 M
0000C2₁₆	Source address register 0 H
0000C3₁₆	
0000C4₁₆	Destination address register 0 L
0000C5₁₆	Destination address register 0 M
0000C6₁₆	Destination address register 0 H
0000C7₁₆	
0000C8₁₆	Transfer counter register 0 L
0000C9₁₆	Transfer counter register 0 M
0000CA₁₆	Transfer counter register 0 H
0000CB₁₆	
0000CC₁₆	DMA0 mode register L
0000CD₁₆	DMA0 mode register H
0000CE₁₆	DMA0 control register
0000CF₁₆	
0000D0₁₆	Source address register 1 L
0000D1₁₆	Source address register 1 M
0000D2₁₆	Source address register 1 H
0000D3₁₆	
0000D4₁₆	Destination address register 1 L
0000D5₁₆	Destination address register 1 M
0000D6₁₆	Destination address register 1 H
0000D7₁₆	
0000D8₁₆	Transfer counter register 1 L
0000D9₁₆	Transfer counter register 1 M
0000DA₁₆	Transfer counter register 1 H
0000DB₁₆	
0000DC₁₆	DMA1 mode register L
0000DD₁₆	DMA1 mode register H
0000DE₁₆	DMA1 control register
0000DF₁₆	
0000E0₁₆	Source address register 2 L
0000E1₁₆	Source address register 2 M
0000E2₁₆	Source address register 2 H
0000E3₁₆	
0000E4₁₆	Destination address register 2 L
0000E5₁₆	Destination address register 2 M
0000E6₁₆	Destination address register 2 H
0000E7₁₆	
0000E8₁₆	Transfer counter register 2 L
0000E9₁₆	Transfer counter register 2 M
0000EA₁₆	Transfer counter register 2 H
0000EB₁₆	
0000EC₁₆	DMA2 mode register L
0000ED₁₆	DMA2 mode register H
0000EE₁₆	DMA2 control register
0000EF₁₆	
0000F0₁₆	Source address register 3 L
0000F1₁₆	Source address register 3 M
0000F2₁₆	Source address register 3 H
0000F3₁₆	
0000F4₁₆	Destination address register 3 L
0000F5₁₆	Destination address register 3 M
0000F6₁₆	Destination address register 3 H
0000F7₁₆	
0000F8₁₆	Transfer counter register 3 L
0000F9₁₆	Transfer counter register 3 M
0000FA₁₆	Transfer counter register 3 H
0000FB₁₆	
0000FC₁₆	DMA3 mode register L
0000FD₁₆	DMA3 mode register H
0000FE₁₆	DMA3 control register
0000FF₁₆	

Note 1: Do not read/write to this address.

Fig. 3 Location of peripheral devices' control registers (2)

Processor mode

The M37920S4CGP operates only in the microprocessor mode exclusive for the external ROM. Be sure to fix the level at pin MD0 to Vcc and the level at pin MD1 to Vss. Also, be sure to fix bits 1, 0 at address $5E_{16}$ (the processor mode register 0) to “1” and “0”, respectively.

Microprocessor mode

When the microcomputer starts its operation after reset with the level at pin MD0 = Vcc level (5 V), the microcomputer is placed in the microprocessor mode.

Table 1. Relationship between pins MD0, MD1 and processor mode

Pin MD0	Pin MD1	Processor mode
VCC level (5 V)	VSS level (5 V)	After reset, the microcomputer starts its operation in the microprocessor mode. (Be sure to pin MD0 to Vcc level.)

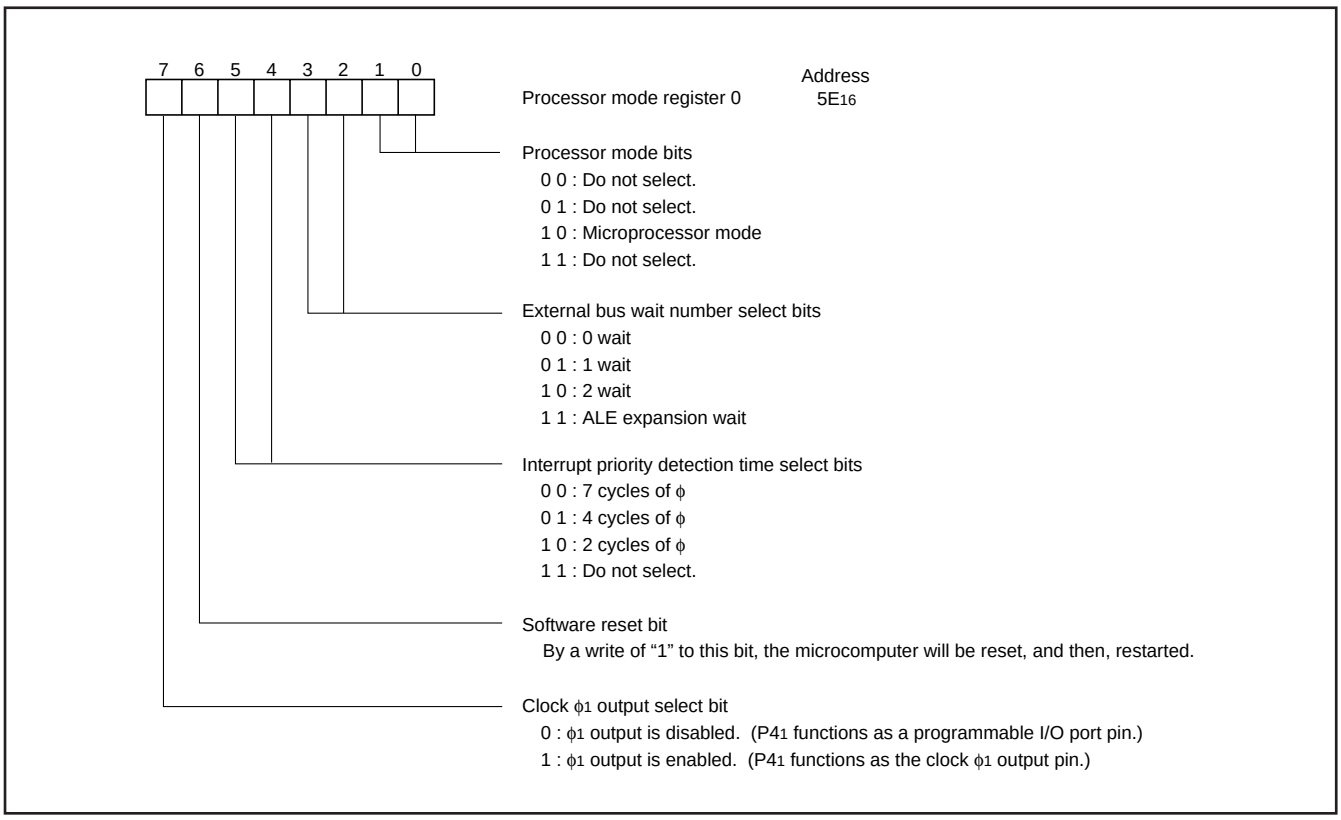


Fig. 4 Processor mode register 0's bit configuration

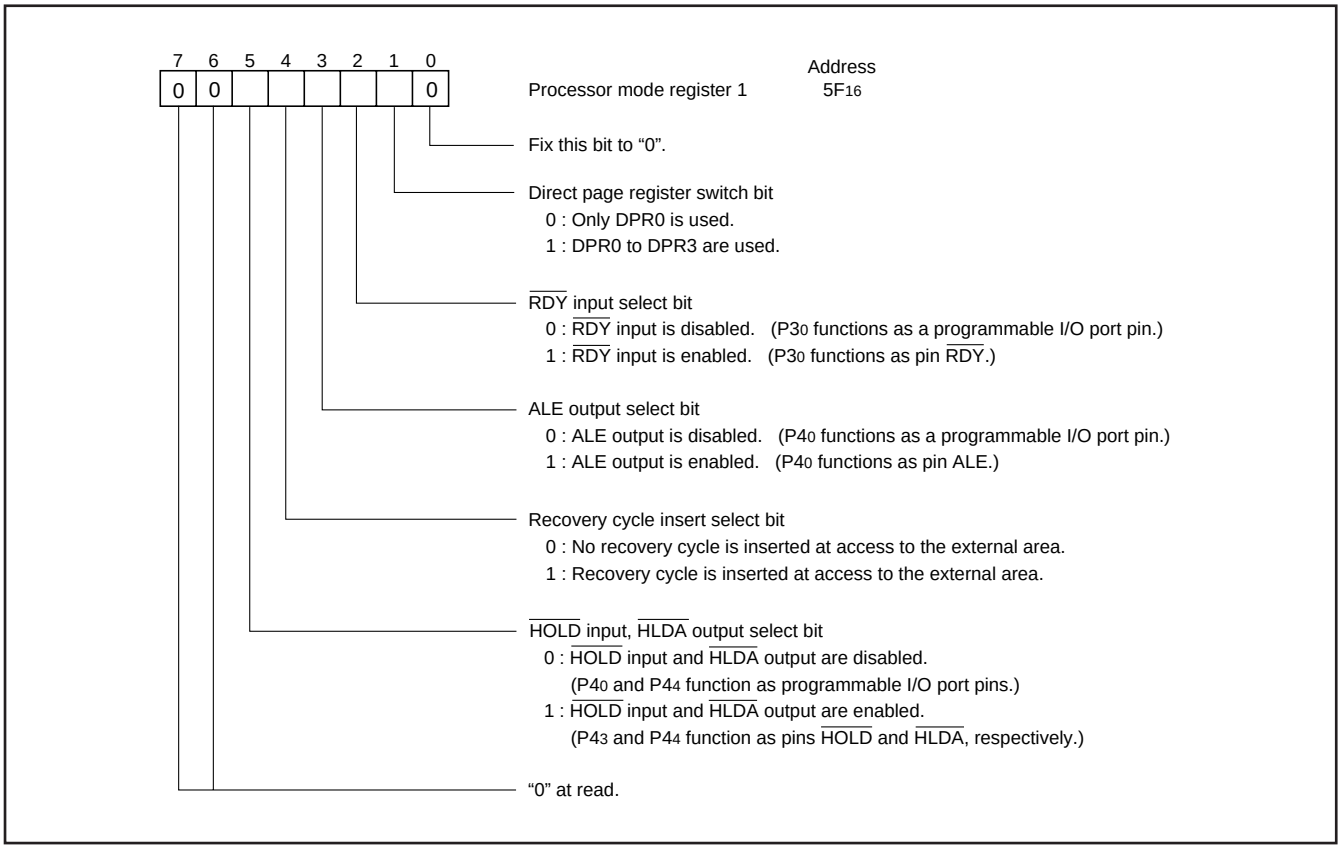


Fig. 5 Processor mode register 1’s bit configuration

	Address	
Port P0 direction register	(04₁₆)···	00₁₆
Port P1 direction register	(05₁₆)···	00₁₆
Port P2 direction register	(08₁₆)···	00₁₆
Port P3 direction register	(09₁₆)···	✕✕✕✕0000
Port P4 direction register	(0C₁₆)···	✕✕✕00000
Port P5 direction register	(0D₁₆)···	00₁₆
Port P6 direction register	(10₁₆)···	✕0000000
Port P7 direction register	(11₁₆)···	✕✕✕✕0000
Port P8 direction register	(14₁₆)···	✕0000000
Port P9 direction register	(15₁₆)···	✕0000000
Port P10 direction register	(18₁₆)···	00₁₆
Port P11 direction register	(19₁₆)···	00₁₆
Port P12 direction register	(1C₁₆)···	✕✕✕✕✕000
A-D control register 0	(1E₁₆)···	00000???
A-D control register 1	(1F₁₆)···	✕0000001
UART 0 Transmit/Receive mode register	(30₁₆)···	00₁₆
UART 1 Transmit/Receive mode register	(38₁₆)···	00₁₆
UART 0 Transmit/Receive control register 0	(34₁₆)···	00001000
UART 1 Transmit/Receive control register 0	(3C₁₆)···	00001000
UART 0 Transmit/Receive control register 1	(35₁₆)···	00000010
UART 1 Transmit/Receive control register 1	(3D₁₆)···	00000010
Count start register	(40₁₆)···	00₁₆
One-shot start register	(42₁₆)···	0✕✕00000
Up-down register	(44₁₆)···	00000000
Timer A clock division select register	(45₁₆)···	✕✕✕✕✕✕00
Timer A0 mode register	(56₁₆)···	00₁₆
Timer A1 mode register	(57₁₆)···	00₁₆
Timer A2 mode register	(58₁₆)···	00₁₆
Timer A3 mode register	(59₁₆)···	00₁₆
Timer A4 mode register	(5A₁₆)···	00₁₆
Timer B0 mode register	(5B₁₆)···	00?✕0000
Timer B1 mode register	(5C₁₆)···	00?✕0000
Timer B2 mode register	(5D₁₆)···	00?✕0000

	Address	
Processor mode register 0	(5E₁₆)···	[Note 2]00010[Note 2]0
Processor mode register 1	(5F₁₆)···	00 **(Note 2)** 00
Watchdog timer	(60₁₆)···	FFF₁₆
Watchdog timer frequency select register	(61₁₆)···	✕✕✕✕✕✕✕0
Particular function select register 0	(62₁₆)···	✕✕✕✕✕✕00
Particular function select register 1	(63₁₆)···	✕✕✕✕00 **(Note 3)**
Debug control register 0	(66₁₆)···	1 **(Note 3)**
Debug control register 1	(67₁₆)···	000[Note 3]000[Note 3]
$\overline{INT_3}$ interrupt control register	(6E₁₆)···	✕✕✕✕0000
$\overline{INT_4}$ interrupt control register	(6F₁₆)···	✕✕✕✕0000
A-D conversion interrupt control register	(70₁₆)···	✕✕✕✕?000
UART 0 transmit interrupt control register	(71₁₆)···	✕✕✕✕0000
UART 0 receive interrupt control register	(72₁₆)···	✕✕✕✕0000
UART 1 transmit interrupt control register	(73₁₆)···	✕✕✕✕0000
UART 1 receive interrupt control register	(74₁₆)···	✕✕✕✕0000
Timer A0 interrupt control register	(75₁₆)···	✕✕✕✕0000
Timer A1 interrupt control register	(76₁₆)···	✕✕✕✕0000
Timer A2 interrupt control register	(77₁₆)···	✕✕✕✕0000
Timer A3 interrupt control register	(78₁₆)···	✕✕✕✕0000
Timer A4 interrupt control register	(79₁₆)···	✕✕✕✕0000
Timer B0 interrupt control register	(7A₁₆)···	✕✕✕✕0000
Timer B1 interrupt control register	(7B₁₆)···	✕✕✕✕0000
Timer B2 interrupt control register	(7C₁₆)···	✕✕✕✕0000
$\overline{INT_0}$ interrupt control register	(7D₁₆)···	✕✕00000
$\overline{INT_1}$ interrupt control register	(7E₁₆)···	✕✕00000
$\overline{INT_2}$ interrupt control register	(7F₁₆)···	✕✕00000
Processor status register PS		000??000???
Program bank register PG		00₁₆
Program counter PC_H		Contents at address FFFF₁₆
Program counter PC_L		Contents at address FFFE₁₆
Direct page registers DPR0 to DPR3		0000₁₆
Data bank register DT		00₁₆
Stack pointer		FFF₁₆

Notes 1: The contents of the other registers and RAM are undefined at reset and must be initialized by software.
2: The status just after reset depends on the voltage level applied to pin MD0.
3: At power-on reset, these bits are clear to "0". At hardware or software reset, on the other hand, these bits retain the state just before reset.

Fig. 6 Microcomputer internal status just after reset (1)

	Address									
$\overline{CS_0}$ control register L	(80_{16})···	(Note 2)	1	0	X	0	(Note 3)	1	0
$\overline{CS_0}$ control register H	(81_{16})···	X	X	X	X	X	0	0	1
$\overline{CS_1}$ control register L	(82_{16})···	0	1	0	0	0	(Note 3)	1	0
$\overline{CS_1}$ control register H	(83_{16})···	0	X	X	X	X	0	0	0
$\overline{CS_2}$ control register L	(84_{16})···	0	1	0	0	0	(Note 3)	1	0
$\overline{CS_2}$ control register H	(85_{16})···	0	X	X	X	X	0	0	0
$\overline{CS_3}$ control register L	(86_{16})···	0	1	0	0	0	(Note 3)	1	0
$\overline{CS_3}$ control register H	(87_{16})···	X	X	X	X	X	0	0	0
Area $\overline{CS_0}$ start address register	($8A_{16}$)···	0	0	0	1	0	0	0	0
Area $\overline{CS_1}$ start address register	($8C_{16}$)···	0	0	0	0	0	0	0	0
Area $\overline{CS_2}$ start address register	($8E_{16}$)···	0	0	0	0	0	0	0	0
Area $\overline{CS_3}$ start address register	(90_{16})···	0	0	0	0	0	0	0	0
Real-time output control register	($A0_{16}$)···	0	0	0	0	0	0	0	0
DRAM control register	($A8_{16}$)···	0	0	0	0	0	0	0	0
$\overline{CTS}$/$\overline{RTS}$ separate select register	(AC_{16})···	0	0	0	0	0	0	0	0
DMAC control register L	($B0_{16}$)···	0	0	0	0	0	0	0	0
DMAC control register H	($B1_{16}$)···	0	0	0	0	0	0	0	0

	Address								
DMA0 interrupt control register	($B2_{16}$)···	X	X	X	X	0	0	0	0
DMA1 interrupt control register	($B3_{16}$)···	X	X	X	X	0	0	0	0
DMA2 interrupt control register	($B4_{16}$)···	X	X	X	X	0	0	0	0
DMA3 interrupt control register	($B5_{16}$)···	X	X	X	X	0	0	0	0
DMA0 mode register L	(CC_{16})···	0	0	0	0	0	0	0	0
DMA0 mode register H	(CD_{16})···	0	0	0	0	0	0	0	0
DMA0 control register	(CE_{16})···	0	0	0	0	0	0	0	0
DMA1 mode register L	(DC_{16})···	0	0	0	0	0	0	0	0
DMA1 mode register H	(DD_{16})···	0	0	0	0	0	0	0	0
DMA1 control register	(DE_{16})···	0	0	0	0	0	0	0	0
DMA2 mode register L	(EC_{16})···	0	0	0	0	0	0	0	0
DMA2 mode register H	(ED_{16})···	0	0	0	0	0	0	0	0
DMA2 control register	(EE_{16})···	0	0	0	0	0	0	0	0
DMA3 mode register L	(FC_{16})···	0	0	0	0	0	0	0	0
DMA3 mode register H	(FD_{16})···	0	0	0	0	0	0	0	0
DMA3 control register	(FE_{16})···	0	0	0	0	0	0	0	0

Notes 1: The contents of the other registers and RAM are undefined at reset and must be initialized by software.
2: The status just after reset depends on the voltage level applied to pin MD0.
3: While Vss level voltage is applied to pin BYTE, these bits are “0”. While Vcc level voltage is applied to pin BYTE, on the other hand, these bits are “1”.

Fig. 7 Microcomputer internal registers’ status just after reset (2)

INPUT/OUTPUT PINS

Each of ports P3 to P9 and P12 has an direction register, and each bit can be programmed for input or output. A pin becomes an output pin when the corresponding bit of direction register is “1”, and an input pin when it is “0”.

When a pin is programmed as an output pin, the data written to its port latch is output to the output pin. When a pin is programmed as an output pin, the contents of the port latch are read out instead of the value of the pin. Accordingly, a previously output value can be read out correctly even when the output “H” voltage is lowered or the output “L” voltage is raised, owing to an external load, etc.

A pin programmed as an input pin is placed in the flooting state, and the value input to the pin can be read out correctly. When a pin is programmed as an input pin, the data can be written only in the port latch, and the pin remains floating.

Each of Figures 8 and 9 shows the block diagram for each port pin.

Table 2. Correspondence between external buses, bus control signals, and programmable I/O port pins

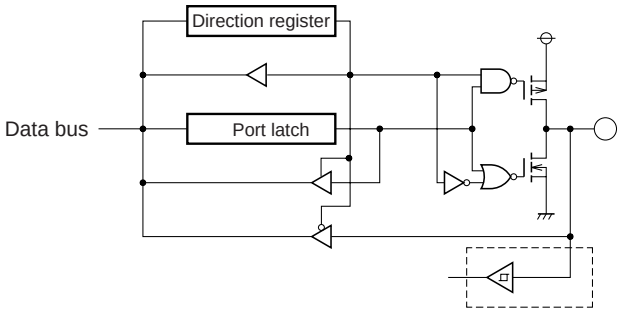
External buses, Bus control signals	Standby state select bit	
	0	1
A_0 to A_7, A_8 to A_{15}, A_{16} to A_{23}	A_0 to A_7, A_8 to A_{15}, A_{16} to A_{23}	$P10_0$ to $P10_7$ **(Note 2)**, $P11_0$ to $P11_7$ **(Note 2)**, $P0_0$ to $P0_7$ **(Note 2)**
D_0 to D_7, D_8 to D_{15}	D_0 to D_7, D_8 to D_{15} **(Note 1)**	$P1_0$ to $P1_7$ **(Note 2)**, $P2_0$ to $P2_7$
$\overline{RD}$, $\overline{BLW}$, $\overline{BHW}$	$\overline{RD}$, $\overline{BLW}$, $\overline{BHW}$ **(Note 1)**	$P3_1$, $P3_2$ **(Note 2)**, $P3_3$
$\overline{CS_0}$	$\overline{CS_0}$	$P9_0$ **(Note 2)**

Notes 1: When the external data bus width = 8 bits (BYTE = V_{CC} level), this becomes a programmable I/O port pin, regardless of the standby state select bit’s contents.

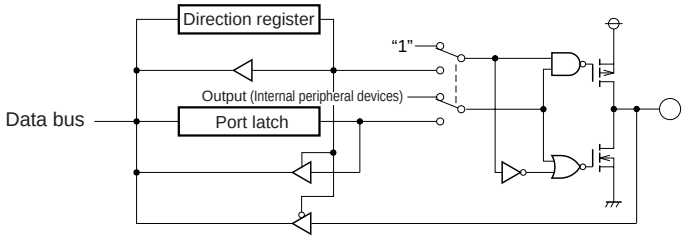
2: Pin functions of port pins P0, P1, $P3_1$, $P3_2$, $P9_0$, P10, P11 are not shown in the pin configuration. However, relationship with corresponding bus signals and ports is listed in Table 2. For the addresses of these port’s registers and direction registers, refer to the location of the perpheral devices’ control registers (Figures 2 and 3).

[Inside dotted-line not included]
P20/D8 to P27/D15, P33/$\overline{BHW}$

[Inside dotted-line included]
P30/$\overline{RDY}$, P43/$\overline{HOLD}$,
P61/TA1IN/$\overline{DMAREQ0}$,
P63/TA3IN/$\overline{DMAREQ1}$,
P65/TA4IN/$\overline{DMAREQ2}$, P66/$\overline{DMAREQ3}$,
P81/RxD1, P85/RxD0, P120/$\overline{INT0}$/TB0IN,
P121/$\overline{INT1}$/TB1IN, P122/$\overline{INT2}$/TB2IN

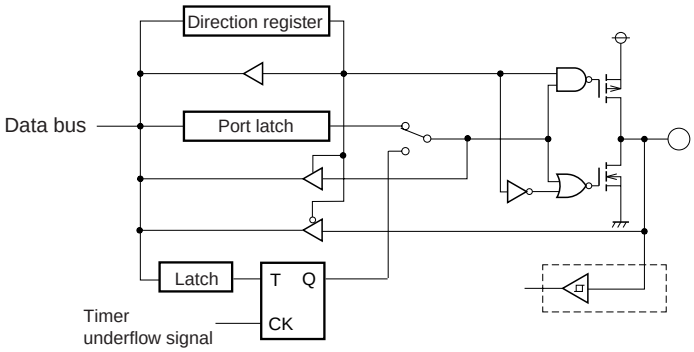


P40/ALE, P41/ϕ1, P44/$\overline{HLDA}$,
P60/TA1OUT/$\overline{DMAACK0}$,
P62/TA3OUT/$\overline{DMAACK1}$,
P64/TA4OUT/$\overline{DMAACK2}$,
P80/TxD1, P84/TxD0,
P91/$\overline{CS1}$/$\overline{RAS1}$, P92/$\overline{CS2}$/$\overline{RAS2}$,
P93/$\overline{CS3}$/$\overline{RAS3}$, P94/$\overline{CAS}$/$\overline{W}$,
P95/$\overline{WRL}$/$\overline{LCAS}$, P96/$\overline{WRH}$/$\overline{UCAS}$



[Inside dotted-line not included]
P52/RTP02, P53/RTP03, P54/RTP10,
P55/RTP11

[Inside dotted-line included]
P51/TA0IN/RTP01, P57/TA2IN/RTP13



P50/TA0OUT/RTP00, P56/TA2OUT/RTP12

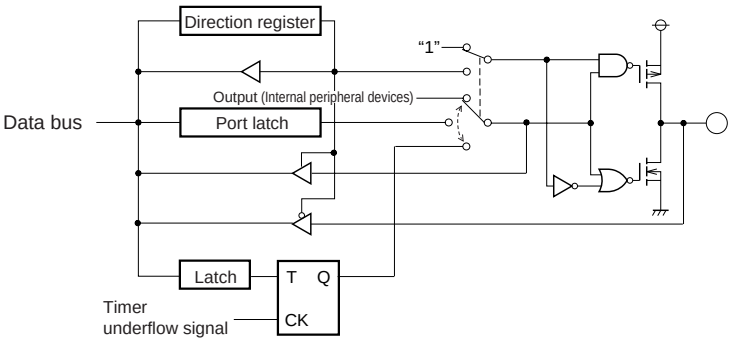
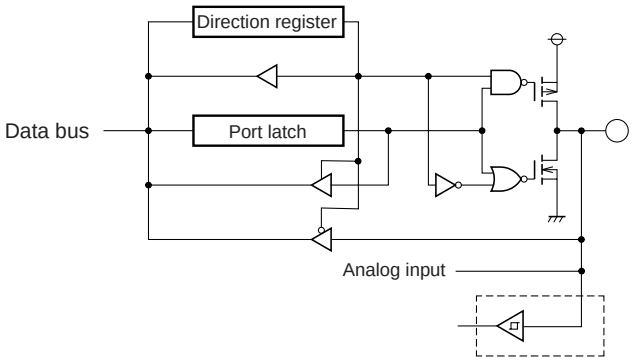


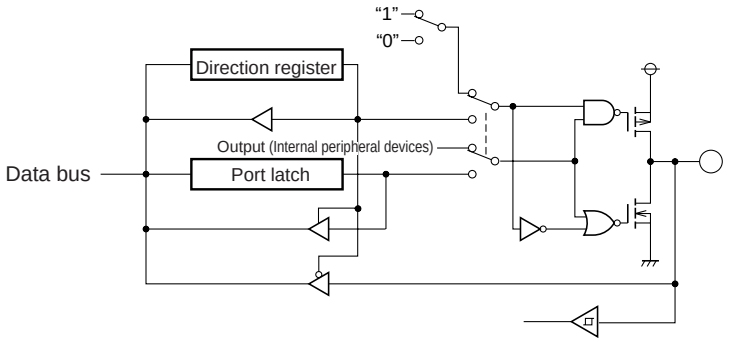
Fig. 8 Block diagram for each port pin (1)

[Inside dotted-line not included]
P7$_0$/AN$_0$, P7$_1$/AN$_1$

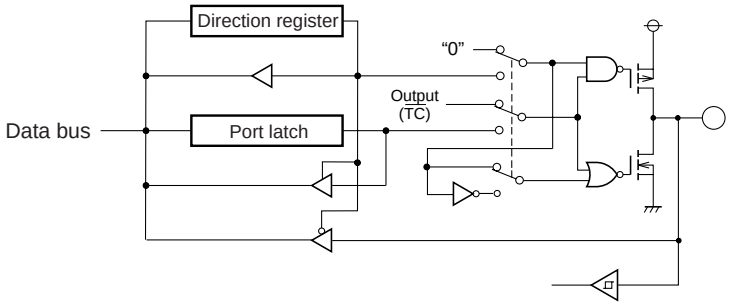
[Inside dotted-line included]
P7$_2$/AN$_2$/$\overline{\text{INT}_3}$, P7$_3$/AN$_3$/$\overline{\text{AD}}$TRG/$\overline{\text{INT}_4}$



P8$_2$/$\overline{\text{CTS}_0}$/CLK$_1$, P8$_3$/$\overline{\text{CTS}_0}$/$\overline{\text{RTS}_0}$,
P8$_6$/CLK$_0$



P4$_2$/$\overline{\text{TC}}$



$\overline{\text{RD}}$, $\overline{\text{BLW}}$, $\overline{\text{CS}_0}$, A$_0$ to A$_{23}$, D$_0$ to D$_7$

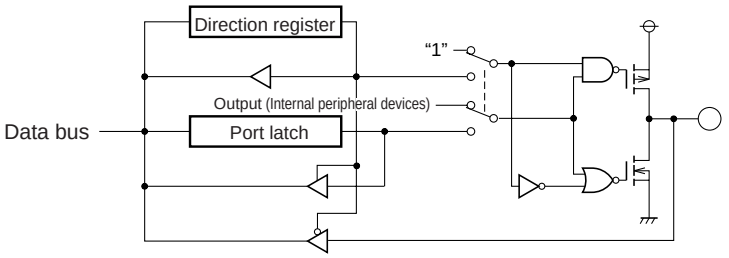


Fig. 9 Block diagram for each port pin (2)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Power source voltage	–0.3 to 6.5	V
AVCC	Analog power source voltage	–0.3 to 6.5	V
V_I	Input voltage D0–D7, D8/P20–D15/P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122, VREF, XIN, RESET, BYTE, MD0, MD1, NMI	–0.3 to VCC+0.3	V
V_O	Output voltage A0–A23, RD, BLW, BHW/P33, CS0, D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122, XOUT	–0.3 to VCC+0.3	V
P_d	Power dissipation	300	mW
T_{opr}	Operating temperature	–20 to 85	°C
T_{stg}	Storage temerature	–40 to 150	°C

RECOMMENDED OPERATING CONDITIONS (Vcc = 5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage		4.5	5	5.5	V
AVCC	Analog power source voltage			VCC		V
V_{SS}	Power source voltage			0		V
AVSS	Analog power source voltage			0		V
V_{IH}	High-level input voltage	P20–P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122, XIN, RESET, BYTE, MD0, MD1, NMI	0.8VCC		VCC	V
V_{IH}	High-level input voltage	D0–D7, D8–D15	0.5VCC		VCC	V
V_{IL}	Low-level input voltage	P20–P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122, XIN, RESET, BYTE, MD0, MD1, NMI	0		0.2VCC	V
V_{IL}	Low-level input voltage	D0–D7, D8–D15	0		0.16VCC	V
$I_{OH\ (peak)}$	High-level peak output current	A0–A23, RD, BLW, BHW/P33, CS0, D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122			–10	mA
$I_{OH\ (avg)}$	High-level average output current	A0–A23, RD, BLW, BHW/P33, CS0, D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122			–5	mA
$I_{OL\ (peak)}$	Low-level peak output current	A0–A23, RD, BLW, BHW/P33, CS0, D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122			10	mA
$I_{OL\ (avg)}$	Low-level average output current	A0–A23, RD, BLW, BHW/P33, CS0, D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122			5	mA
f(XIN)	External clock input frequency				20	MHz

Notes 1: Average output current is the average value of an interval of 100 ms.

2: The sum of $I_{OL(peak)}$ for A0–A23, D0–D7, D8/P20–D15/P27, ports P80–P86 must be 80 mA or less, the sum of $I_{OH(peak)}$ for A0–A23, D0–D7, D8/P20–D15/P27, ports P80–P86 must be 80 mA or less, the sum of $I_{OL(peak)}$ for ports P30, RD, BLW, BHW/P33, CS0, P40–P44, P50–P57, P60–P66, P70–P73, P91–P96, P120–P122 must be 80 mA or less, the sum of $I_{OH(peak)}$ for P30, RD, BLW, BHW/P33, CS0, P40–P44, P50–P57, P60–P66, P70–P73, P91–P96, P120–P122 must be 80 mA or less.

DC ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –20 to 85 °C, f(XIN) = 20 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	High-level output voltage A0–A23, $\overline{CS0}$, D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P93, P1220–P1222	IOH = –10 mA	3			V
VOH	High-level output voltage A0–A23, $\overline{CS0}$, D0–D7, D8/P20–D15/P27, P40, P44, P91–P93	IOH = –400 μA	4.7			V
VOH	High-level output voltage $\overline{RD}$, $\overline{BLW}$, $\overline{BHW}$/P33, P94/$\overline{CAS}$/$\overline{W}$, P95/$\overline{WRL}$/$\overline{LCAS}$, P96/$\overline{WRH}$/$\overline{UCAS}$	IOH = –10 mA	3.4			V
		IOH = –400 μA	4.8			
VOL	Low-level output voltage A0–A23, $\overline{CS0}$, D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P93, P1220–P1222	IOL = 10 mA			2	V
VOL	Low-level output voltage A0–A23, $\overline{CS0}$, D0–D7, D8/P20–D15/P27, P40, P44, P91–P93	IOL = 2 mA			0.45	V
VOL	Low-level output voltage $\overline{RD}$, $\overline{BLW}$, $\overline{BHW}$/P33, P94/$\overline{CAS}$/$\overline{W}$, P95/$\overline{WRL}$/$\overline{LCAS}$, P96/$\overline{WRH}$/$\overline{UCAS}$	IOL = 10 mA			1.6	V
		IOL = 2 mA			0.4	
VT+ —VT–	Hysteresis TA0IN–TA4IN, TB0IN–TB2IN, $\overline{INT0}$–$\overline{INT4}$, $\overline{DMAREQ0}$–$\overline{DMAREQ3}$, $\overline{ADTRG}$, $\overline{CTS0}$, CLK0, CLK1, $\overline{NMI}$, $\overline{RDY}$, $\overline{HOLD}$, RxD0, RxD1		0.4		1	V
VT+ —VT–	Hysteresis $\overline{RESET}$		0.5		1.5	V
VT+ —VT–	Hysteresis XIN		0.1		0.3	V
IIH	High-level input current D0–D7, D8/P20–D15/P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P1220–P1222, XIN, $\overline{RESET}$, BYTE, MD0, MD1, $\overline{NMI}$	VI = 5.0 V			5	μA
IIL	Low-level input current D0–D7, D8/P20–D15/P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P1220–P1222, XIN, $\overline{RESET}$, BYTE, MD0, MD1, $\overline{NMI}$	VI = 0 V			–5	μA
VRAM	RAM hold voltage	When clock is stoped.	2			V
ICC	Power source current	At reset in microprocessor mode, output-only pins are open, and the other pins are connected to Vss. f(XIN) = 20 MHz.		25	50	mA
		Ta = 25 °C when clock is stopped.			1	μA
		Ta = 80 °C when clock is stopped.			20	

A-D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5 V ± 10 %, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
				Min.	Max.	
————	Resolution	V_{REF} = V_{CC}			10	Bits
————	Absolute accuracy	V_{REF} = V_{CC}	10-bit resolution mode		± 3	LSB
			8-bit resolution mode		± 2	LSB
R_{LADDER}	Ladder resistance	V_{REF} = V_{CC}		5		kΩ
t_{CONV}	Conversion time	f(X_{IN}) ≤ 20 MHz	10-bit resolution mode	5.9		μs
			8-bit resolution mode	2.45 **(Note)**		
V_{REF}	Reference voltage	————		2.7	V_{CC}	V
V_{IA}	Analog input voltage	————		0	V_{REF}	V

Note: This is applied when A-D conversion freguency (ϕ_{AD}) = $f_{1(\phi)}$.

PERIPHERAL DEVICE INPUT/OUTPUT TIMING

(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 20 MHz unless otherwise noted)

✻ For limits depending on f(X_{IN}), their calculation formulas are shown below. Also, the values at f(X_{IN}) = 20 MHz are shown in ( ).

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi$_{IN}$ input cycle time	80		ns
$t_{w(TAH)}$	TAi$_{IN}$ input high-level pulse width	40		ns
$t_{w(TAL)}$	TAi$_{IN}$ input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TA)}$	TAi$_{IN}$ input cycle time	f(X_{IN}) ≤ 20 MHz	$\frac{16 \times 10^9}{f(X_{IN})}$ (800)		ns
$t_{w(TAH)}$	TAi$_{IN}$ input high-level pulse width	f(X_{IN}) ≤ 20 MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns
$t_{w(TAL)}$	TAi$_{IN}$ input low-level pulse width	f(X_{IN}) ≤ 20 MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns

Note : The TAi$_{IN}$ input cycle time requires 4 or more cycles of a count source. The TAi$_{IN}$ input high-level pulse width and the TAi$_{IN}$ input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f_2 at f(X_{IN}) ≤ 20 MHz.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TA)}$	TAi$_{IN}$ input cycle time	f(X_{IN}) ≤ 20 MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns
$t_{w(TAH)}$	TAi$_{IN}$ input high-level pulse width		80		ns
$t_{w(TAL)}$	TAi$_{IN}$ input low-level pulse width		80		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi$_{IN}$ input high-level pulse width	80		ns
$t_{w(TAL)}$	TAi$_{IN}$ input low-level pulse width	80		ns

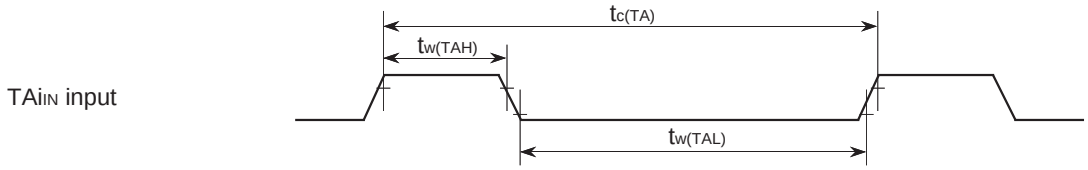
Timer A input (Up-down input and Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi$_{OUT}$ input cycle time	2000		ns
$t_{w(UPH)}$	TAi$_{OUT}$ input high-level pulse width	1000		ns
$t_{w(UPL)}$	TAi$_{OUT}$ input low-level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAi$_{OUT}$ input setup time	400		ns
$t_{h(TIN-UP)}$	TAi$_{OUT}$ input hold time	400		ns

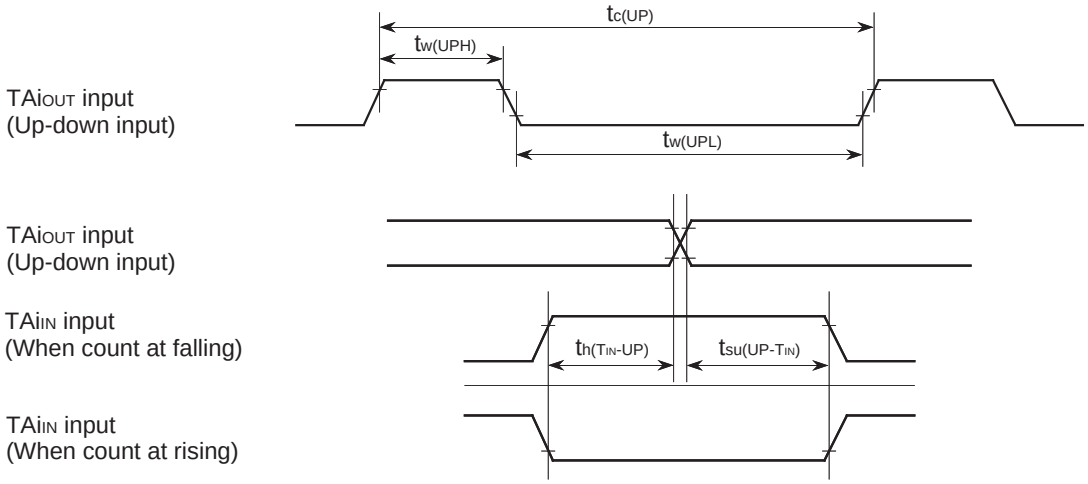
Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi$_{IN}$ input cycle time	800		ns
$t_{su(TAj_{IN}\text{-}TAj_{OUT})}$	TAj$_{IN}$ input setup time	200		ns
$t_{su(TAj_{OUT}\text{-}TAj_{IN})}$	TAj$_{OUT}$ input setup time	200		ns

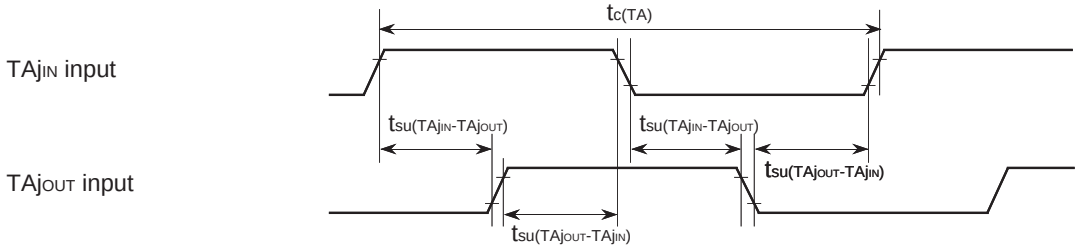
•Gating input in timer mode
•Count input in event counter mode
•External trigger input in one-shot pulse mode
•External trigger input in pulse width modulation mode



•Up-down input and Count input in event counter mode



•Two-phase pulse input in event counter mode



Test conditions
•Vcc = 5 V ± 10 %, Ta = –20 to 85 °C
•Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (one edge count)	80		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (one edge count)	40		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (one edge count)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (both edge count)	160		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (both edge count)	80		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (both edge count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	$f(X_{IN}) \leq 20$ MHz	$\frac{16 \times 10^9}{f(X_{IN})}$ (800)		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width	$f(X_{IN}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width	$f(X_{IN}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns

Note: The TBiIN input cycle time requires 4 or more cycles of a count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f_2 at $f(X_{IN}) \leq 20$ MHz.

Timer B input (Pulse width measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	$f(X_{IN}) \leq 20$ MHz	$\frac{16 \times 10^9}{f(X_{IN})}$ (800)		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width	$f(X_{IN}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width	$f(X_{IN}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns

Note: The TBiIN input cycle time requires 4 or more cycles of a count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f_2 at $f(X_{IN}) \leq 20$ MHz.

A-D trigger input

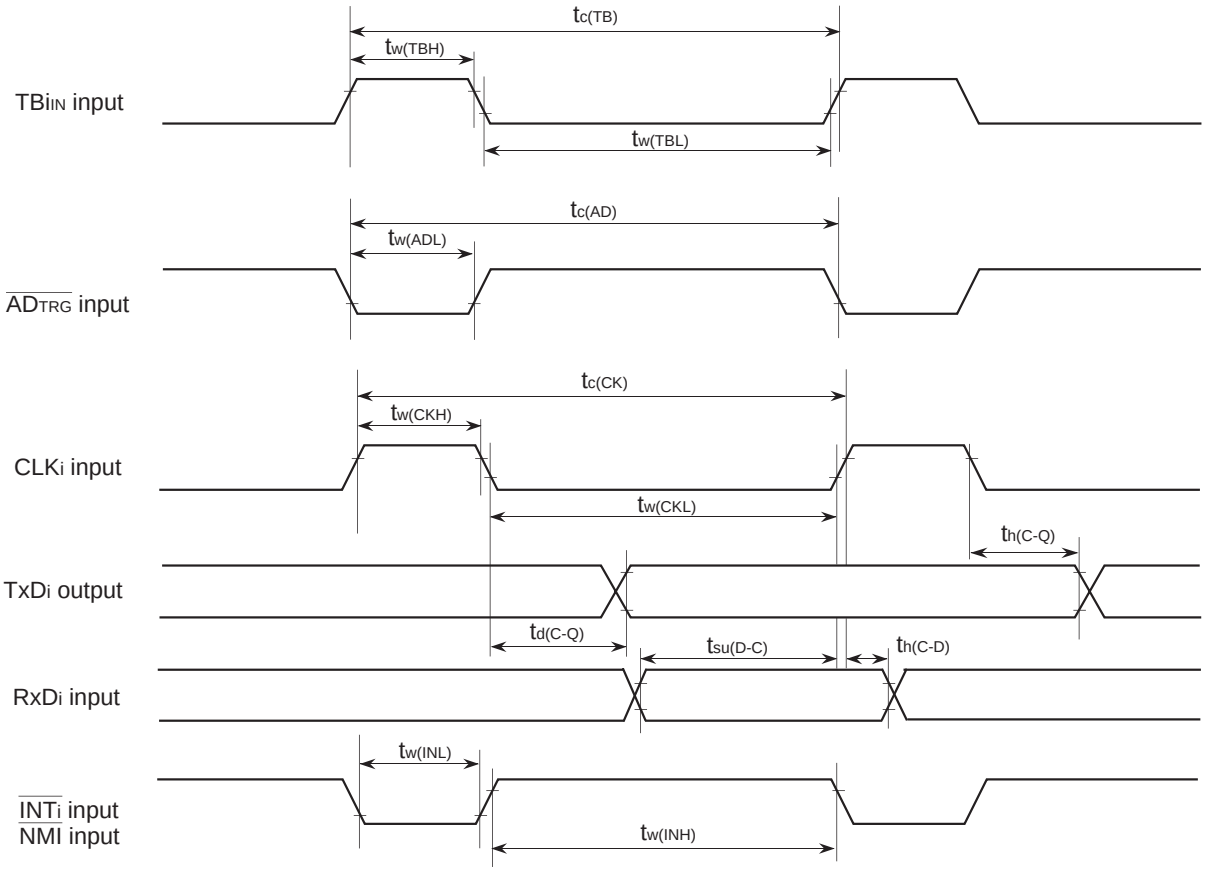
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (minimum allowable trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input low-level pulse width	125		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high-level pulse width	100		ns
$t_{w(CKL)}$	CLKi input low-level pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	20		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

External interrupt ($\overline{INT_i}$) input, $\overline{NMI}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input/$\overline{NMI}$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT_i}$ input/$\overline{NMI}$ input low-level pulse width	250		ns



Test conditions
- Vcc = 5 V ± 10 %, Ta = –20 to 85 °C
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF

READY, HOLD TIMING

Timing requirements (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

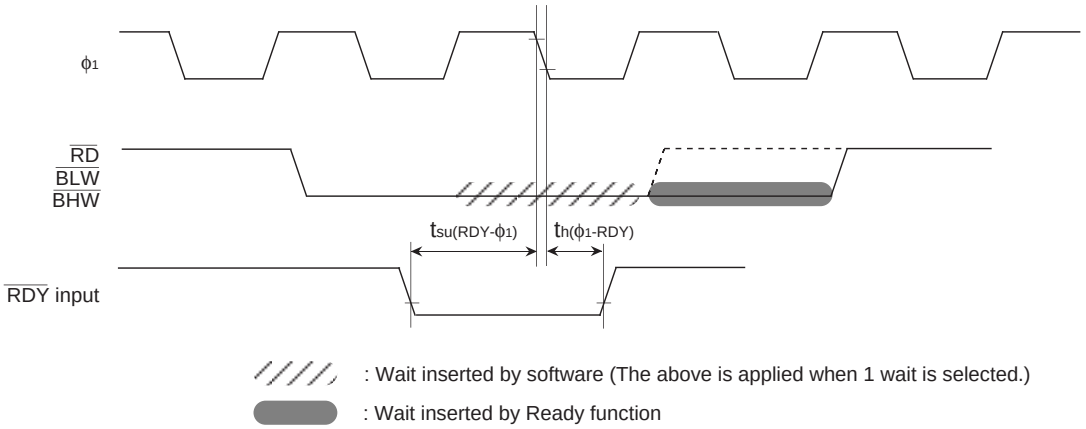
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(RDY-\phi1)}$	$\overline{RDY}$ input setup time	40		ns
$t_{su(HOLD-\phi1)}$	$\overline{HOLD}$ input setup time	40		ns
$t_{h(\phi1-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi1-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

Switching characteristics (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{d(\phi1-HLDAL)}$	$\overline{HLDA}$ output delay time		20	ns
$t_{d(RDH-HLDAL)}$	$\overline{HLDA}$ low-level output delay time after read	tc –15 **(Note)**		ns
$t_{d(BXWH-HLDAL)}$	$\overline{HLDA}$ low-level output delay time after write	tc –15 **(Note)**		ns
$t_{pxz(HLDAL-RDZ)}$	Floating start delay time	–15	10	ns
$t_{pxz(HLDAL-BXWZ)}$	Floating start delay time	–15	10	ns
$t_{pxz(HLDAL-CSiZ)}$	Floating start delay time	–15	10	ns
$t_{pxz(HLDAL-ALEZ)}$	Floating start delay time	–15	10	ns
$t_{pxz(HLDAL-AZ)}$	Floating start delay time	–15	10	ns
$t_{pzx(HLDAL-RDZ)}$	Floating release delay time	0		ns
$t_{pzx(HLDAL-BXWZ)}$	Floating release delay time	0		ns
$t_{pzx(HLDAL-CSiZ)}$	Floating release delay time	0		ns
$t_{pzx(HLDAL-ALEZ)}$	Floating release delay time	0		ns
$t_{pzx(HLDAL-AZ)}$	Floating release delay time	0		ns

Note: tc = 1/f(X_{IN}).

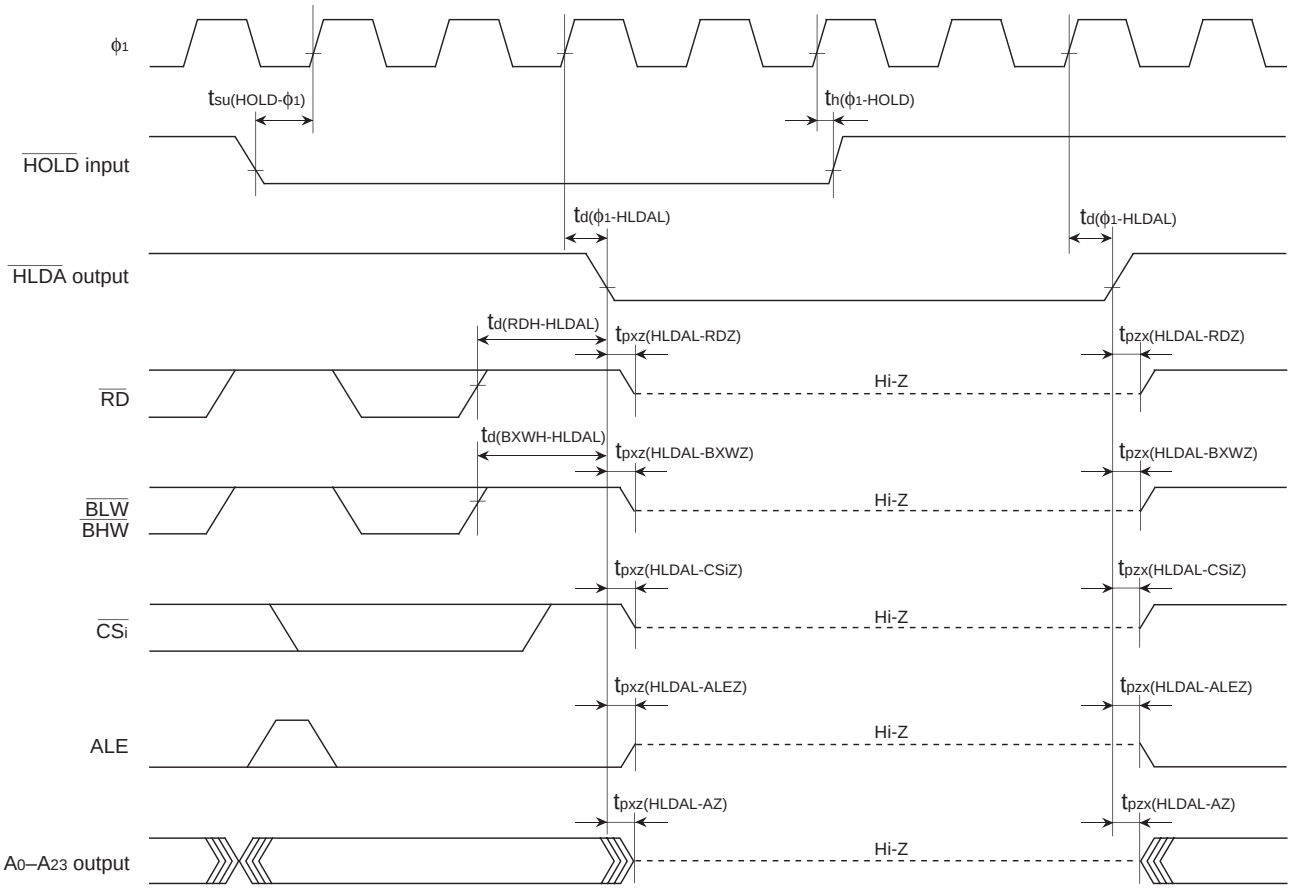
$\overline{RDY}$ input



: Wait inserted by software (The above is applied when 1 wait is selected.)

: Wait inserted by Ready function

$\overline{HOLD}$ input



Test conditions
- Vcc = 5 V ± 10 %, Ta = –20 to 85 °C
- $\overline{RDY}$ input, $\overline{HOLD}$ input : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- HLDA output : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF

External bus timing

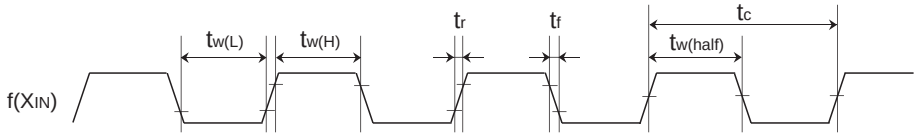
For limits depending on f(X_{IN}), their calculation formulas are shown below.

W = 0 (0 wait)
W = 1 (1 wait)
W = 2 (2 wait)
tc = 1/f(X_{IN}).

Timing Requirements (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		When 0/1/2 wait is selected		When ALE expansion wait is selected		
		Min.	Max.	Min.	Max.	
t_c	External clock input cycle time	50		50		ns
$t_{w(half)}$	External clock input pulse width with half input-volage	0.45tc	0.55tc	0.45tc	0.55tc	ns
$t_{w(H)}$	External clock input high-level pulse width	0.5tc – 8		0.5tc – 8		ns
$t_{w(L)}$	External clock input low-level pulse width	0.5tc – 8		0.5tc – 8		ns
t_r	External clock input rise time		8		8	ns
t_f	External clock input fall time		8		8	ns
$t_{a(A-D)}$	Address access time		(2 + W)tc – 45		4tc – 45	ns
$t_{a(CSiL-D)}$	Chip select access time		(1.5 + W)tc – 35		3.5tc – 35	ns
$t_{a(RDL-D)}$	Read access time		(1 + W)tc – 30		2tc – 30	ns
$t_{su(D-RDL)}$	Read data setup time	15		15		ns
$t_{h(RDH-D)}$	Data input hold time after read	0		0		ns
$t_{a(BA-D)}$	Address access time at burst ROM access		(1 + W)tc – 35		2tc – 35	ns
$t_{h(BA-D)}$	Data hold time after address at burst ROM access	0		0		ns

External clock input



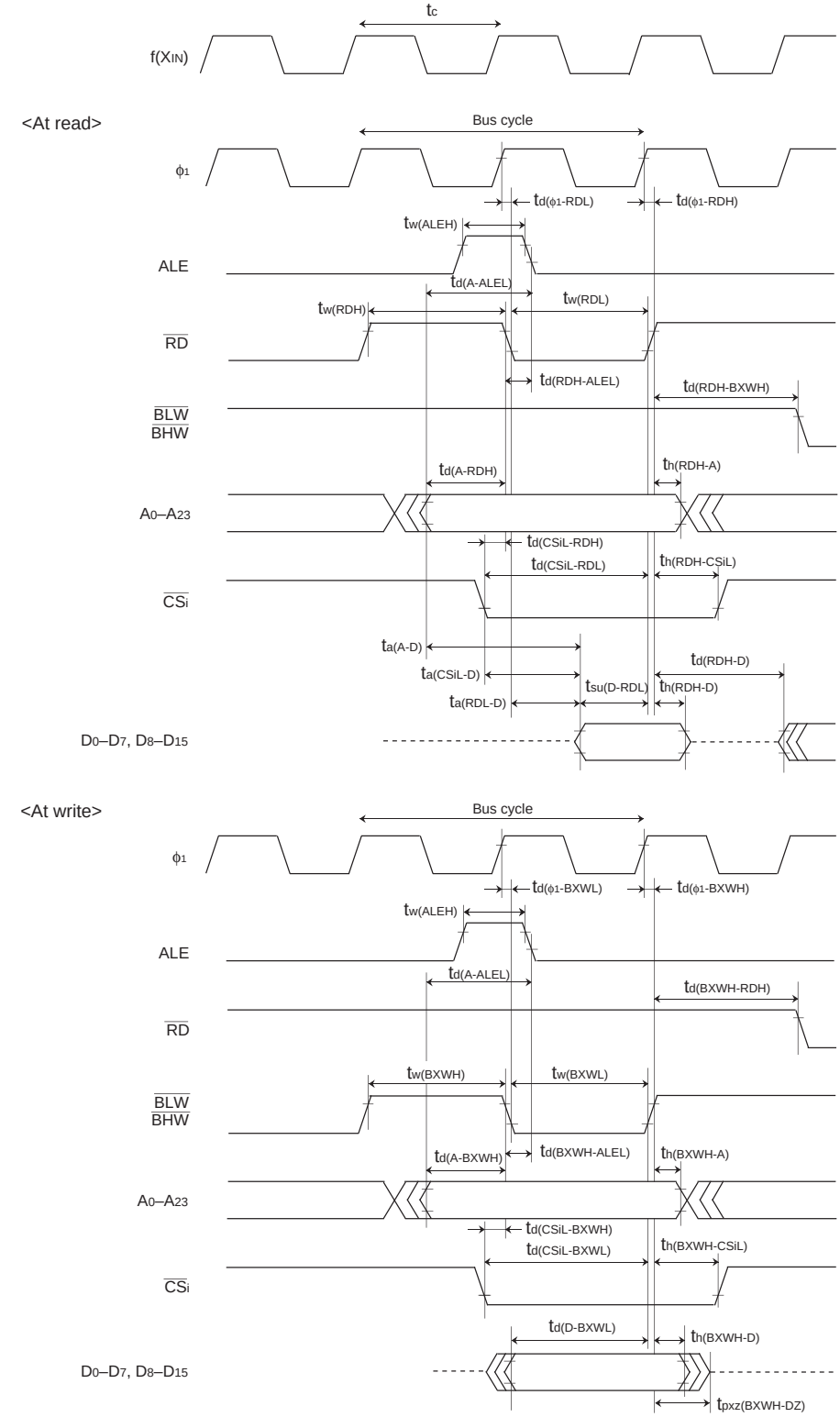
Test conditions
- Vcc = 5 V ± 10 %, Ta = –20 to 85 °C
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V ($t_{w(H)}$, $t_{w(L)}$, t_r, t_f)
- Input timing voltage : 2.5 V (t_c, $t_{w(half)}$)

Switching characteristics (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		When 0/1/2 wait is selected		When ALE expansion wait is selected		
		Min.	Max.	Min.	Max.	
td(φ1-RDL)	Read low-level output delay time	–10	15	–10	15	ns
td(φ1-RDH)	Read high-level output delay time	–10	10	–10	10	ns
td(φ1-BXWL)	Write low-level output delay time	–10	15	–10	15	ns
td(φ1-BXWH)	Write high-level output delay time	–10	10	–10	10	ns
tw(ALEH)	ALE pulse width	0.5tc – 20		tc – 20		ns
td(A-ALEL)	ALE completion delay time after address stabilization	tc – 30		1.5tc – 30		ns
tw(RDL)	Read output pulse width	(1 + W)tc – 15		2tc – 15		ns
tw(RDH)	Read output high-level width **(Note 1)**	tc – 15		2tc – 15		ns
td(RDH-BXWH)	Write disable valid time after read **(Note 2)**	tc – 15		tc – 15		ns
td(A-RDH)	Address valid time before read	tc – 30		2tc – 30		ns
th(RDH-A)	Address hold time after read **(Note 3)**	8		8		ns
td(RDH-ALEL)	ALE completion delay time after read start		20			ns
td(ALEL-RDH)	Read disable valid time after ALE completion			0.5tc – 20		ns
td(CSiL-RDH)	Chip select valid time before read	0.5tc – 20		1.5tc – 20		ns
td(CSiL-RDL)	Chip select output valid time before read completion	(1.5 + W)tc – 20		3.5tc – 20		ns
th(RDH-CSiL)	Chip select hold time after read	0.5tc – 20		0.5tc – 20		ns
td(RDH-D)	Next write cycle data output delay time after read **(Note 2)**	tc – 15		tc – 15		ns
tw(BXWL)	Write output pulse width	(1 + W)tc – 15		2tc – 15		ns
tw(BXWH)	Write output high-level width **(Note 1)**	tc – 15		2tc – 15		ns
td(BXWH-RDH)	Read disable valid time after write **(Note 2)**	tc – 15		tc – 15		ns
td(A-BXWH)	Address valid time before write	tc – 30		2tc-30		ns
th(BXWH-A)	Address hold time after write **(Note 3)**	8		8		ns
td(BXWH-ALEL)	ALE completion delay time after write start		20			ns
td(ALEL-BXWH)	Write disable valid time after ALE completion			0.5tc – 20		ns
td(CSiL-BXWH)	Chip select valid time before write	0.5tc – 20		1.5tc – 20		ns
td(CSiL-BXWL)	Chip select output valid time before write completion	(1.5 + W)tc – 20		3.5tc – 20		ns
th(BXWH-CSiL)	Chip select hold time after write	0.5tc – 20		0.5tc – 20		ns
td(D-BXWL)	Data output valid time before write completion	(1 + W)tc – 20		2tc – 20		ns
th(BXWH-D)	Data hold time after write	0.5tc – 10		0.5tc – 10		ns
tpxz(BXWH-DZ)	Floating start delay time after write		0.5tc + 10		0.5tc + 10	ns

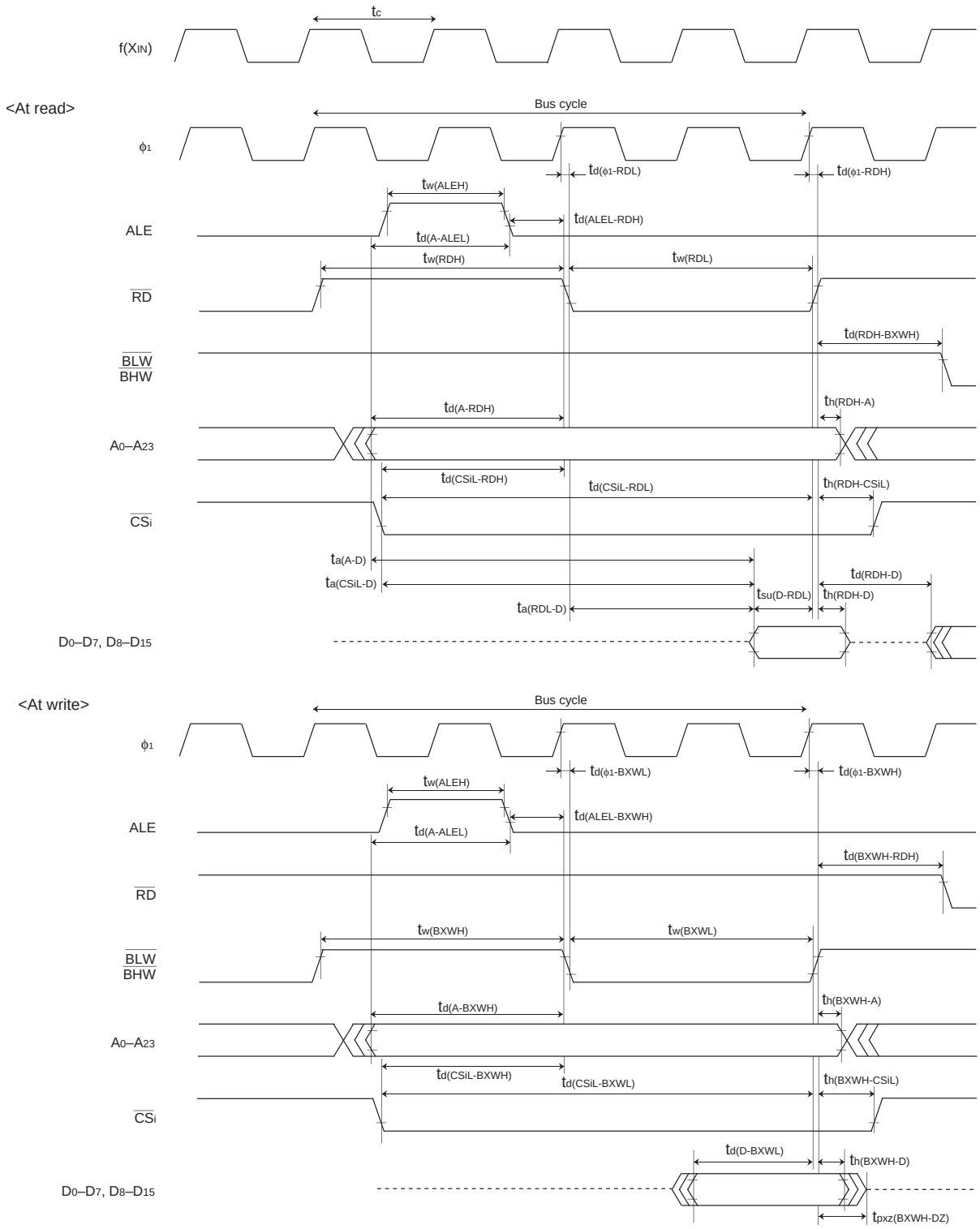
Notes 1: When the bus cycle just before this parameter is for the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns).
2: When accessing the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns).
3: When accessing the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns). However, except for the case at instruction prefetch.

Normal access: 0/1/2 wait



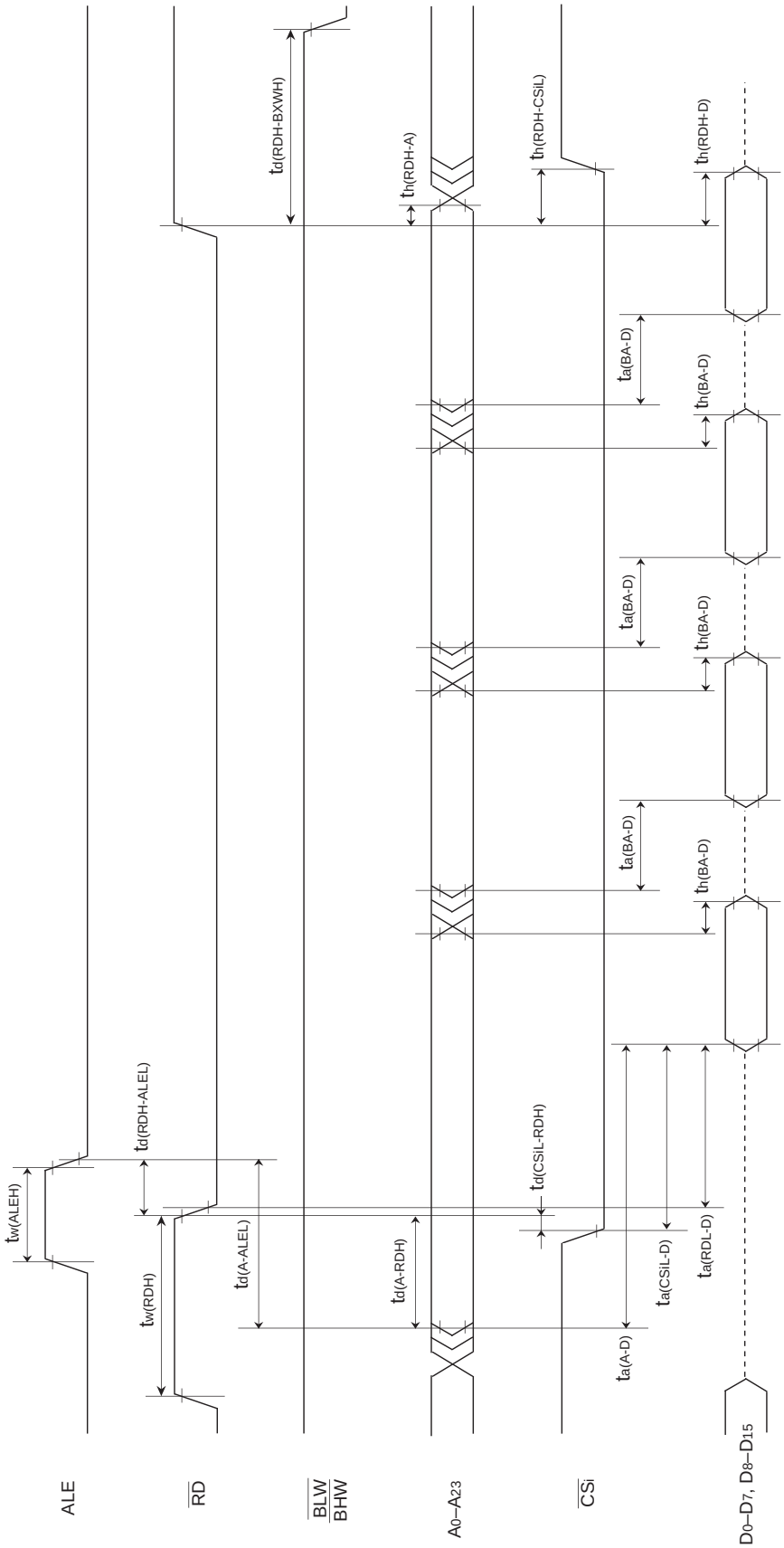
Test conditions
- Vcc = 5 V ± 10 %, Ta = –20 to 85 °C
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 15 pF ($\overline{CS_i}$)
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF (except for $\overline{CS_i}$)

Normal access : ALE extension wait



Test conditions
- Vcc = 5 V ± 10 %, Ta = –20 to 85 °C
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 15 pF ($\overline{CS_i}$)
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF (except for $\overline{CS_i}$)

Burst ROM access : 0/1/2 wait at instruction prefetch



Test conditions
- Vcc = 5 V ± 10 %, Ta = −20 to 85 °C
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 15 pF ($\overline{CSi}$)
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF (except for $\overline{CSi}$)

DRAM access

Timing Requirements (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = 0 to 70 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

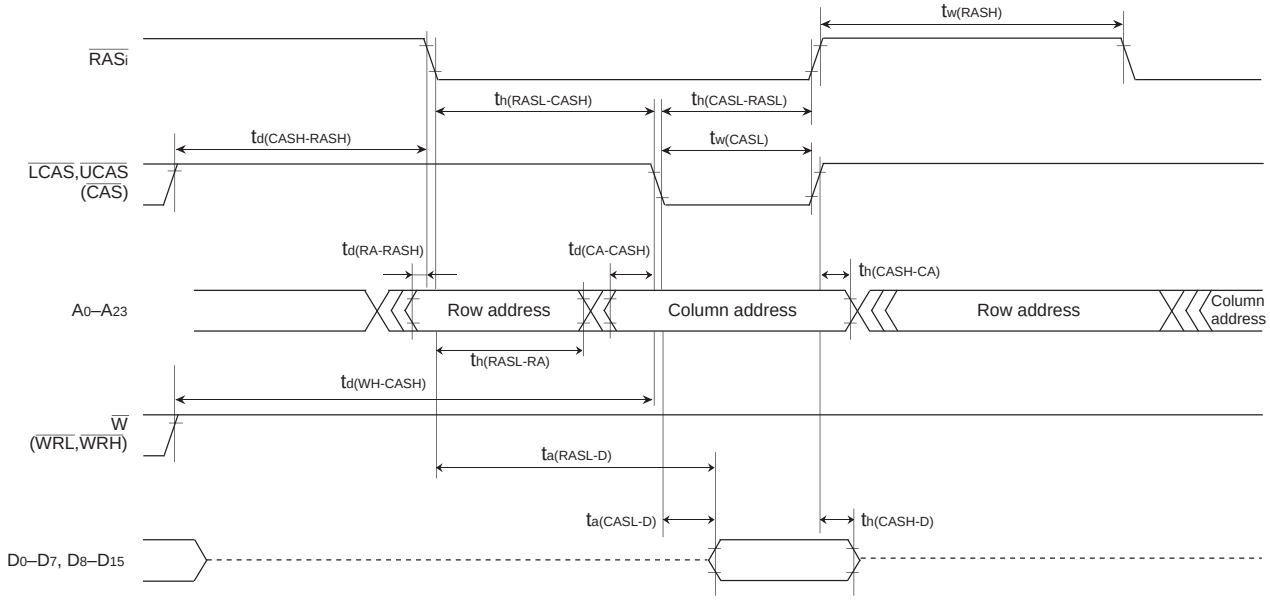
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{a(RASL-D)}$	$\overline{RAS}$ access time		2.5tc – 35	ns
$t_{a(CASL-D)}$	$\overline{CAS}$ access time		tc – 30	ns
$t_{h(CASH-D)}$	Data input hold time after $\overline{CAS}$	0		ns

Switching characteristics (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = 0 to 70 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

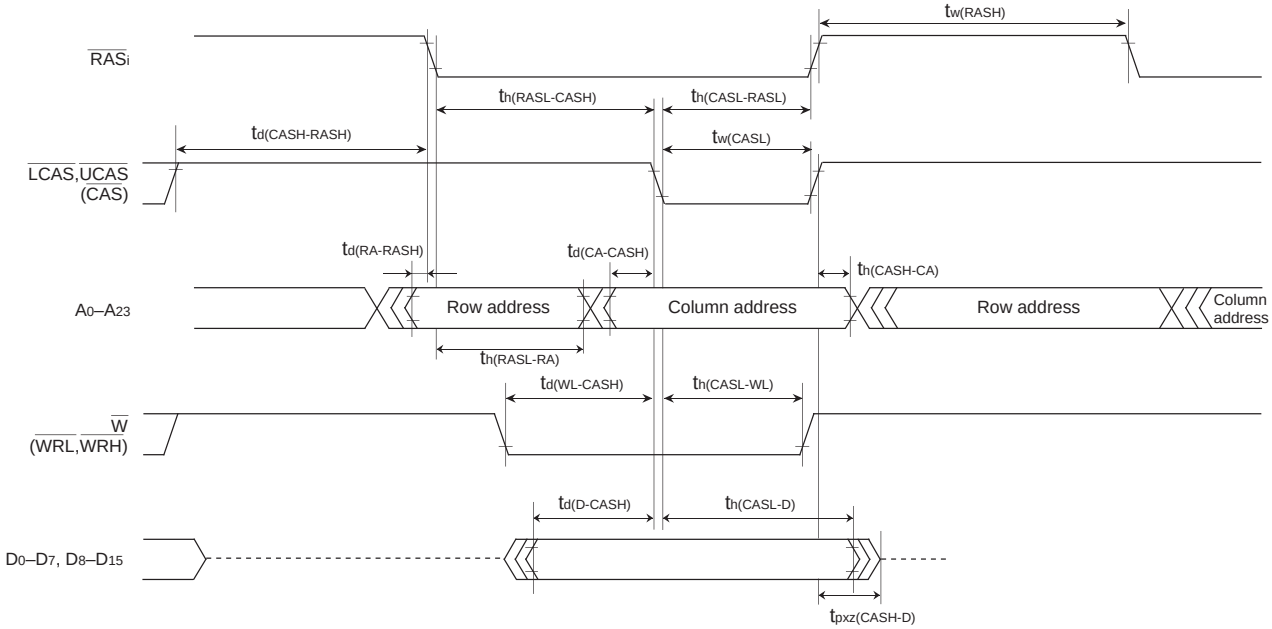
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(RASH)}$	$\overline{RAS}$ high-level pulse width	1.5tc – 20		ns
$t_{d(CASH-RASH)}$	$\overline{CAS}$ high-level valid time before $\overline{RAS}$	1.5tc – 20		ns
$t_{h(RASL-CASH)}$	$\overline{CAS}$ high-level hold time after $\overline{RAS}$'s low level	1.5tc – 20		ns
$t_{h(CASL-RASL)}$	$\overline{RAS}$ hold time after $\overline{CAS}$'s low level	tc – 15		ns
$t_{w(CASL)}$	$\overline{CAS}$ low-level pulse width	tc – 15		ns
$t_{d(RA-RASH)}$	Row address valid time before $\overline{RAS}$	0.5tc – 25		ns
$t_{h(RASL-RA)}$	Row address hold time after $\overline{RAS}$'s low level	tc – 40		ns
$t_{d(CA-CASH)}$	Column address valid time before $\overline{CAS}$	0.5tc – 20		ns
$t_{h(CASH-CA)}$	Column address hold time after $\overline{CAS}$'s high level	0		ns
$t_{d(WH-CASH)}$	$\overline{W}$ high-level valid time before $\overline{CAS}$	3tc – 15		ns
$t_{d(WL-CASH)}$	$\overline{W}$ low-level valid time before $\overline{CAS}$	tc – 15		ns
$t_{h(CASL-WL)}$	$\overline{W}$ hold time after $\overline{CAS}$'s low level	tc – 15		ns
$t_{d(D-CASH)}$	Data output valid time before $\overline{CAS}$	tc – 20		ns
$t_{h(CASL-D)}$	Data output hold time after $\overline{CAS}$'s low level	1.5tc – 15		ns
$t_{pxz(CASH-D)}$	Floating start delay time after $\overline{CAS}$	0.5tc + 10		ns
$t_{d(CAF-CASH)}$	Column address valid time before $\overline{CAS}$ (When fast page access ON is selected)	tc – 40		ns
$t_{d(WFL-CASH)}$	$\overline{W}$ low-level valid time before $\overline{CAS}$ (When fast page access ON is selected)	0.5tc – 20		ns
$t_{d(DF-CASH)}$	Data output valid time before $\overline{CAS}$ (When fast page access ON is selected)	0.5tc – 20		ns
$t_{pxz(WH-D)}$	Floating start delay time after write		0.5tc + 10	ns

DRAM access : fast page access = OFF

<At read>

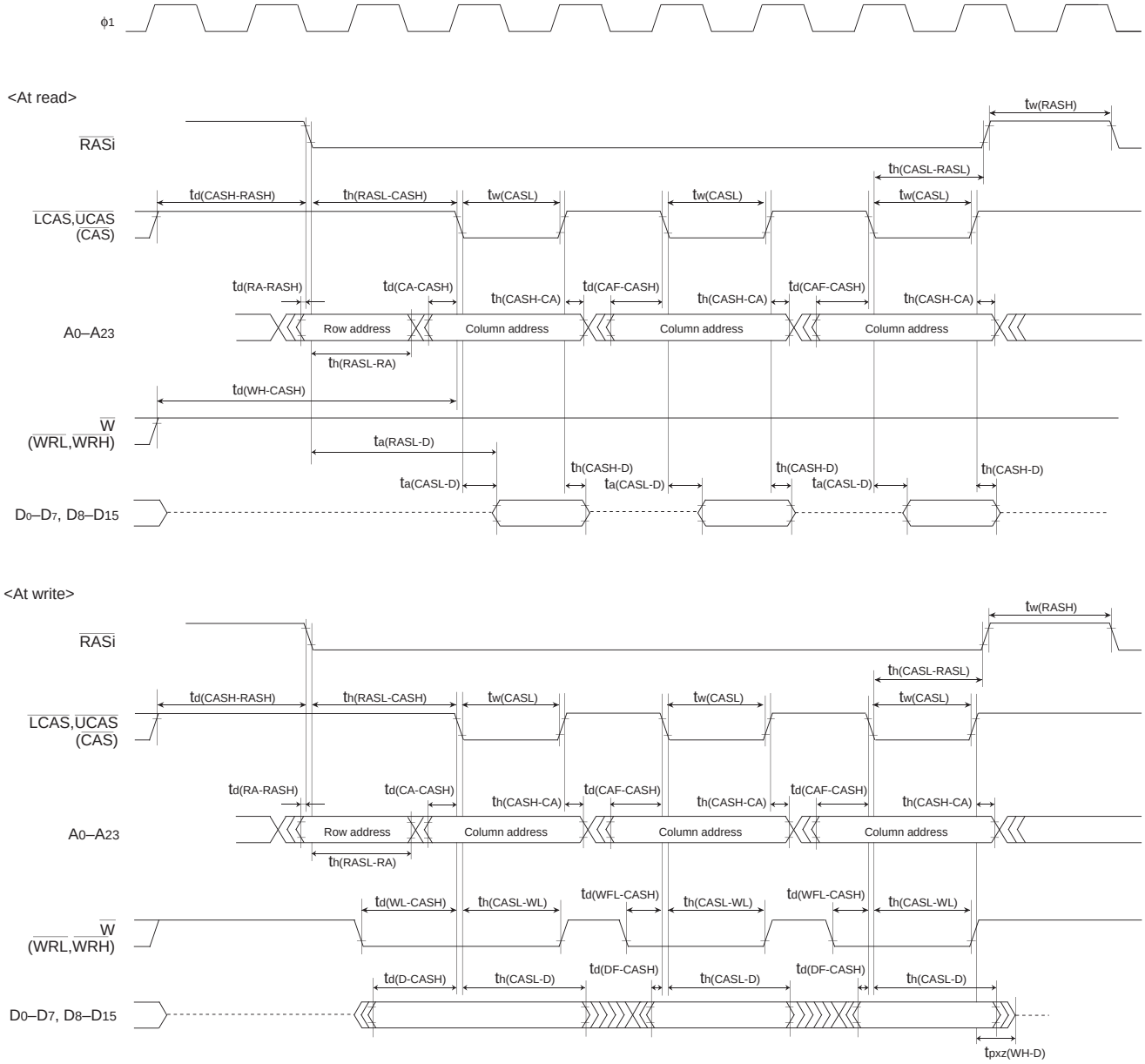


<At write>



Test conditions
- Vcc = 5 V ± 10 %, Ta = 0 to 70 °C
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 15 pF ($\overline{RAS_i}$)
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF (except for $\overline{RAS_i}$)

DRAM access : fast page access = ON



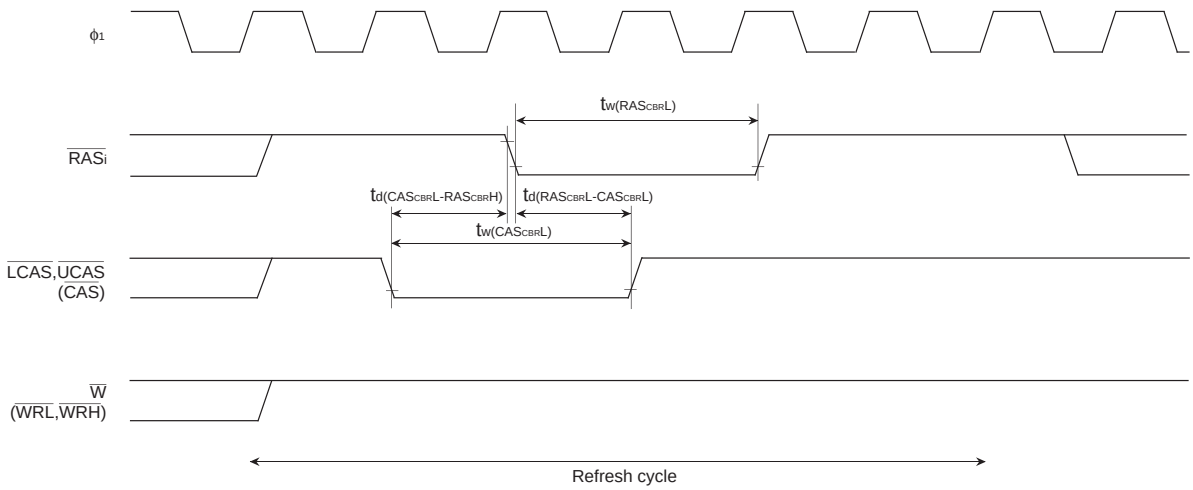
Test conditions
- Vcc = 5 V ± 10 %, Ta = 0 to 70 °C
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 15 pF ($\overline{RAS}i$)
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF (except for $\overline{RAS}i$)

DRAM refresh

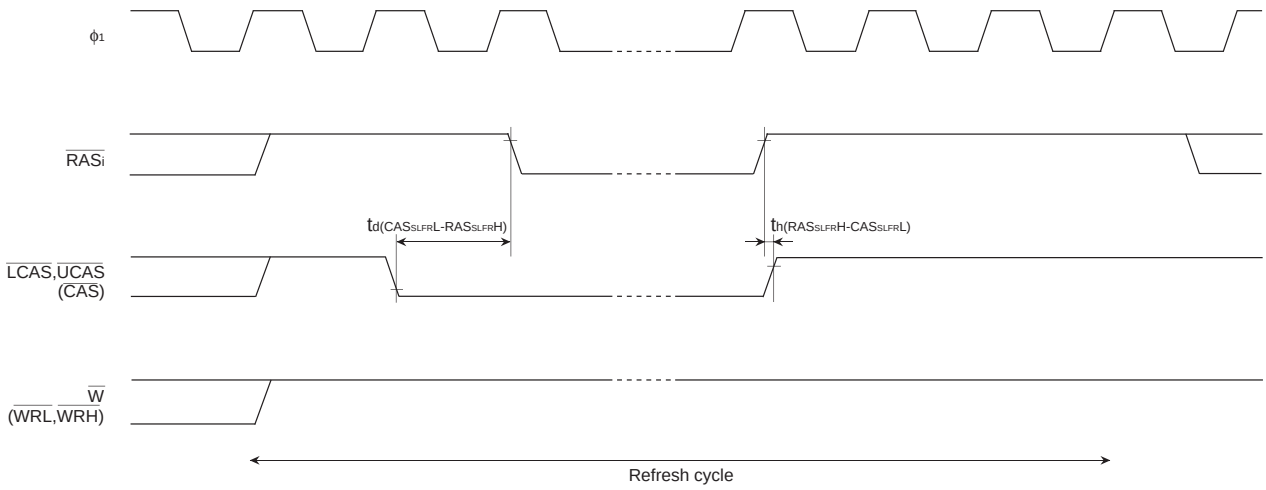
Switching characteristics (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = 0 to 70 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(RAS_{CBR}L)}$	$\overline{RAS}$ low-level pulse width (At $\overline{CAS}$ before $\overline{RAS}$ refresh)	2tc – 15		ns
$t_{w(CAS_{CBR}L)}$	$\overline{CAS}$ low-level pulse width (At $\overline{CAS}$ before $\overline{RAS}$ refresh)	2tc – 15		ns
$t_{d(CAS_{CBR}L\text{-}RAS_{CBR}H)}$	$\overline{RAS}$ high-level valid time after $\overline{CAS}$'s low level start (At $\overline{CAS}$ before $\overline{RAS}$ refresh)	tc – 15		ns
$t_{d(RAS_{CBR}L\text{-}CAS_{CBR}L)}$	$\overline{CAS}$ low-level valid time after $\overline{RAS}$'s low level start (At $\overline{CAS}$ before $\overline{RAS}$ refresh)	tc – 15		ns
$t_{d(CAS_{SLFR}L\text{-}RAS_{SLFR}H)}$	$\overline{RAS}$ high-level valid time after $\overline{CAS}$'s low level start (At self refresh)	tc – 15		ns
$t_{h(RAS_{SLFR}H\text{-}CAS_{SLFR}L)}$	$\overline{CAS}$ low-level hold time after $\overline{RAS}$'s high level (At self refresh)	–15	15	ns

DRAM refresh : $\overline{CAS}$ before $\overline{RAS}$ refresh



DRAM refresh : self refresh



Test conditions
- Vcc = 5 V ± 10 %, Ta = 0 to 70 °C
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 15 pF ($\overline{RAS_i}$)
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF (except for $\overline{RAS_i}$)

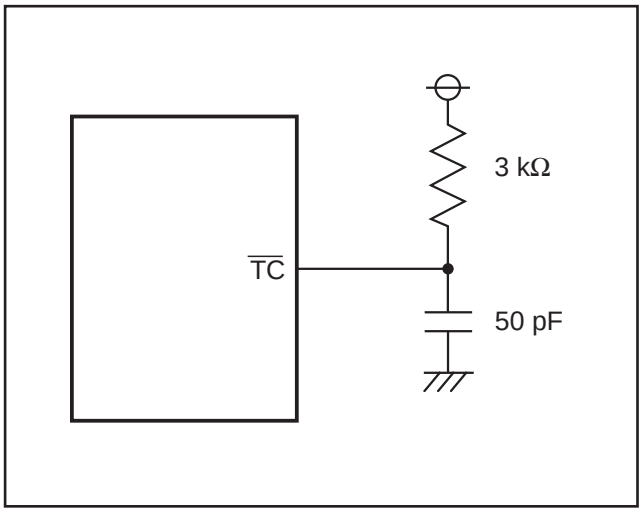
DMA transfer timing

Timing Requirements (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(TC_{IN}L-\phi1)}$	$\overline{TC}$ input setup time	40		ns
$t_{w(TC_{IN}L)}$	$\overline{TC}$ input pulse width	tc + 20		ns
$t_{su(DRQL-\phi1)}$	$\overline{DMAREQ}$i input setup time	40		ns
$t_{w(DRQL)}$	$\overline{DMAREQ}$i input pulse width	tc		ns

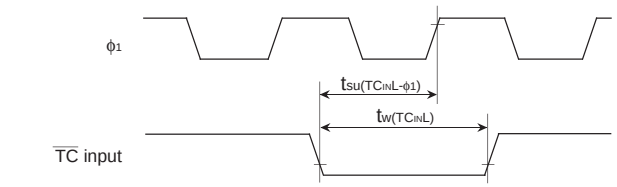
Switching characteristics (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(TCL)}$	$\overline{TC}$ output pulse width	tc – 20		ns
$t_{d(RDH-TCL)}$	$\overline{TC}$ output start delay time after read	tc – 15		ns
$t_{d(BXWH-TCL)}$	$\overline{TC}$ output start delay time after write	tc – 15		ns
$t_{d(TCL-DMAACKL)}$	$\overline{DMAACK}$ low-level output valid time after $\overline{TC}$ output start	2.5tc – 20		ns

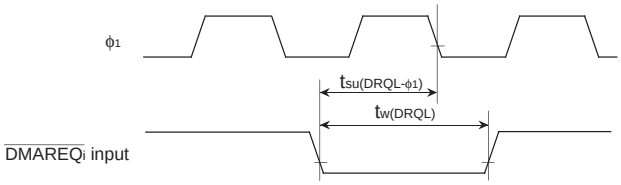


Test circuit for $\overline{TC}$ output

●$\overline{TC}$ input

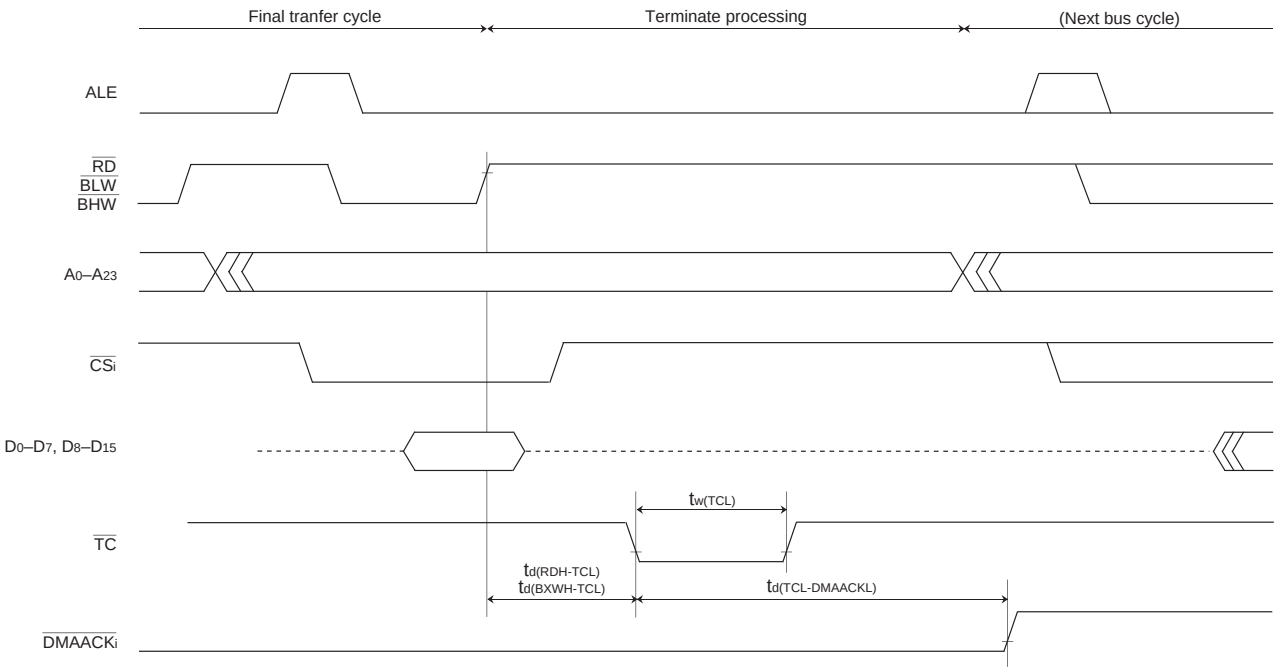


●$\overline{DMAREQ_i}$ input



Test conditions
- Vcc = 5 V ± 10 %, Ta = –20 to 85 °C
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF

●Transfer terminate timing



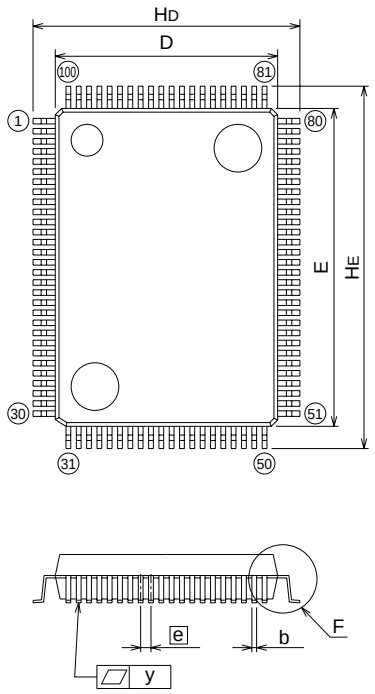
Test conditions
- Vcc = 5 V ± 10 %, Ta = –20 to 85 °C
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF

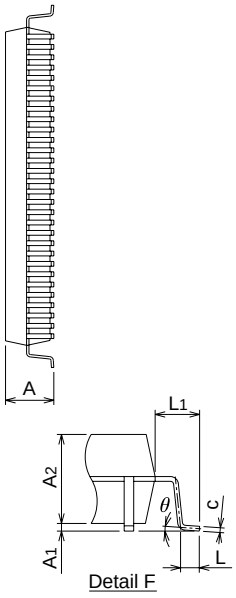
PACKAGE OUTLINE

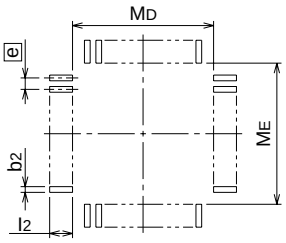
100P6S-A

Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42







Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	–	1.4	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.35	–
l_2	1.3	–	–
M_D	–	14.6	–
M_E	–	20.6	–

REVISION DESCRIPTION LIST	M37920S4CGP Datasheet

Rev. No.	Revision Description	Rev. date
1.00	First Edition	990916