



FEATURES

- Full Four-Quadrant Multiplying DAC
- Guaranteed Monotonic over Temperature
- Non-Linearity: $\pm 1/2$ LSB Achieved without Trimming
- Ultra Stable: 0.2 ppm/ $^{\circ}$ C Max Linearity Tempco
- 2 ppm/ $^{\circ}$ C Max Gain Error Tempco
- Low Output Capacitance
- Low Sensitivity to Amplifier Offset 330 μ V/mV
- Low Glitch Energy
- Low Feedthrough Error
- TTL/CMOS Compatible

- Latch-Up Free
- Improved Replacement for AD7533, AD7520
- Low Cost
- CDIP, PDIP, PLCC & SOIC Packages Available

APPLICATIONS

- Digitally Controlled Attenuators
- Programmable Gain Amplifiers
- Function Generation
- Linear Automatic Gain Control

GENERAL DESCRIPTION

The MP7633 is pin and functionally equivalent to industry's standard AD7533, AD7520 and AD7530. The MP7633 is recommended when lower output capacitance is required. The MP7633 incorporates a unique decoding technique yielding excellent accuracy and stability (0.2 ppm/ $^{\circ}$ C linearity drift and 2 ppm/ $^{\circ}$ C scale factor drift) over temperature and time.

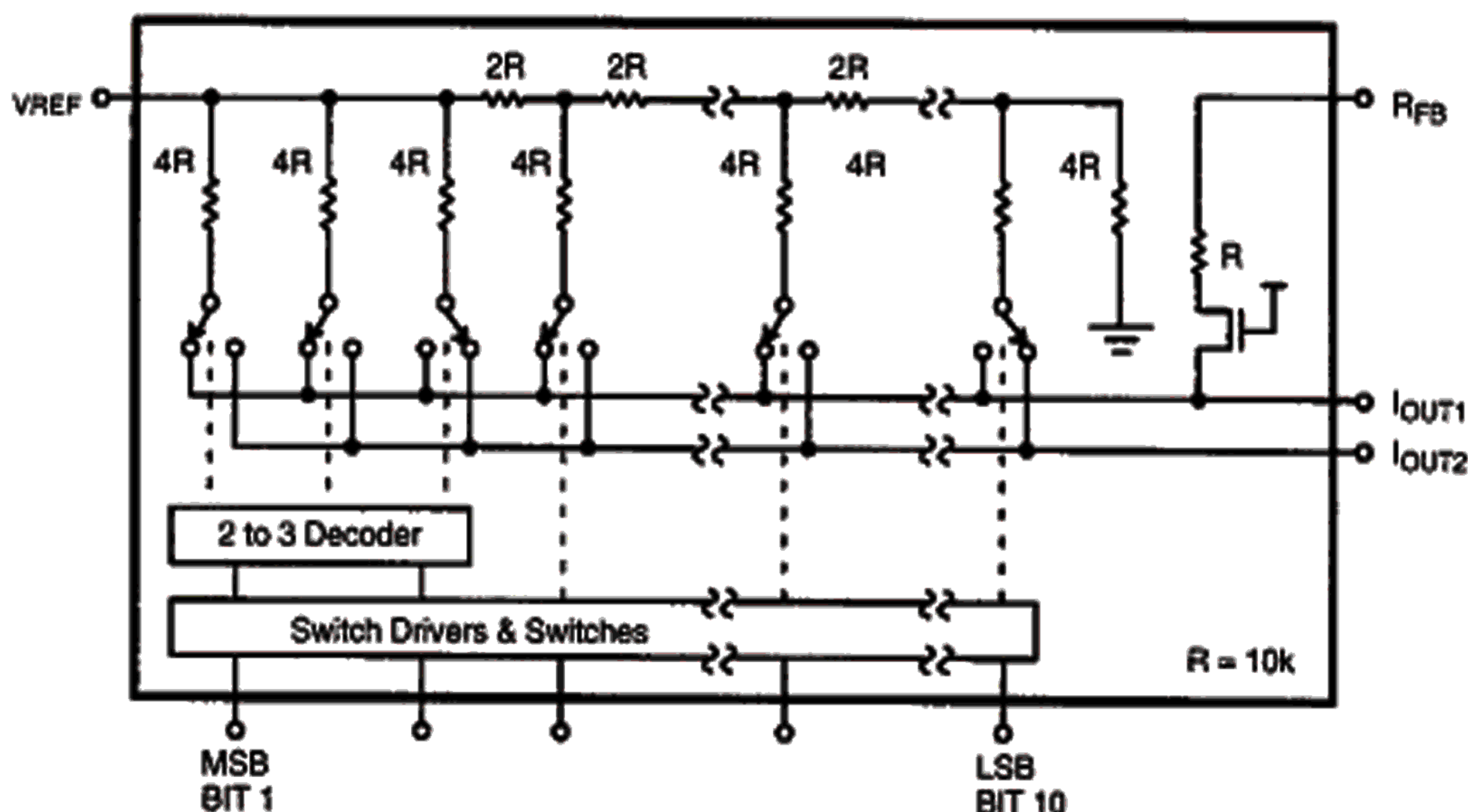
The 2-3 bit decoding architecture of the MP7633 results in

low output capacitances of 52/26pF at I_{OUT1} and 13/45pF at I_{OUT2} , low sensitivity to output amplifier offset of 330 μ V per millivolt offset, eliminating the need for trim pots in many applications.

Specified for operation over the commercial / industrial (-40 to $+85^{\circ}$ C) and military (-55 to $+125^{\circ}$ C) temperature ranges, the MP7633 is available in Plastic (PDIP) and Ceramic (CDIP) dual-in-line, Plastic leaded chip carrier (PLCC) and Surface Mount (SOIC) packages.

4

SIMPLIFIED BLOCK DIAGRAM

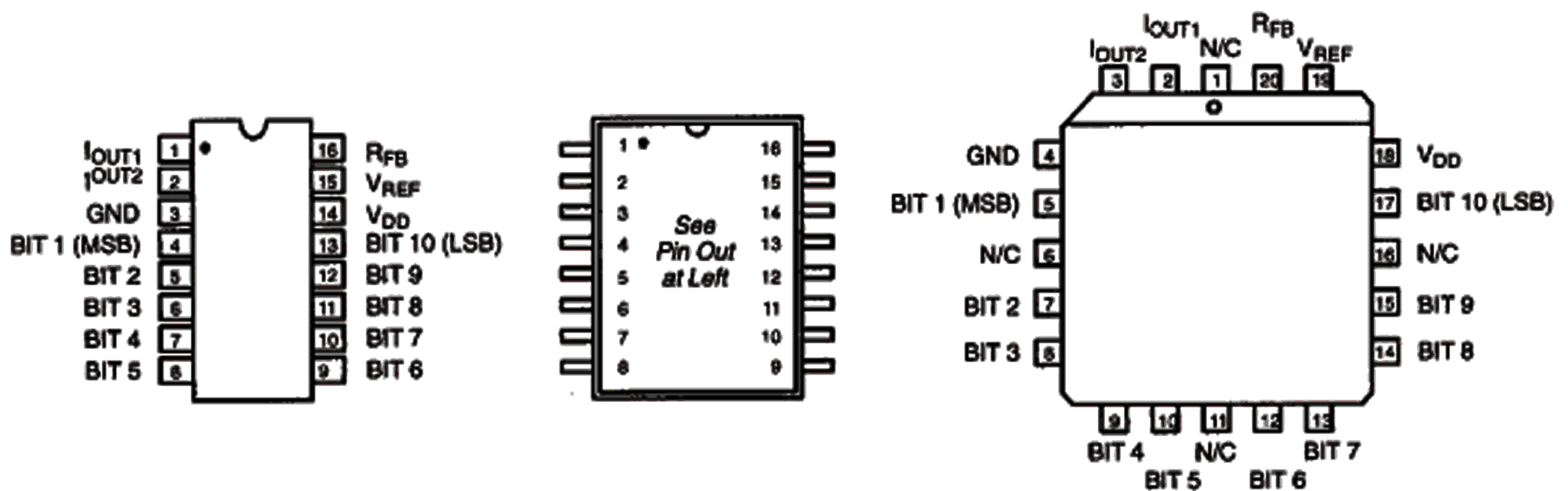


3 Segment D/A Converter with Termination to GND.
Logical "1" at Digital Input Steers Current to I_{OUT1}

ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	-40 to +85°C	MP7633JN	±2	±2	±0.4
Plastic Dip	-40 to +85°C	MP7633KN	±1	±1	±0.4
Plastic Dip	-40 to +85°C	MP7633LN	±1/2	±1/2	±0.4
SOIC	-40 to +85°C	MP7633JS	±2	±2	±0.4
SOIC	-40 to +85°C	MP7633KS	±1	±1	±0.4
SOIC	-40 to +85°C	MP7633LS	±1/2	±1/2	±0.4
PLCC	-40 to +85°C	MP7633JP	±2	±2	±0.4
PLCC	-40 to +85°C	MP7633KP	±1	±1	±0.4
PLCC	-40 to +85°C	MP7633LP	±1/2	±1/2	±0.4
Ceramic Dip	-40 to +85°C	MP7633AD	±2	±2	±0.4
Ceramic Dip	-40 to +85°C	MP7633BD	±1	±1	±0.4
Ceramic Dip	-40 to +85°C	MP7633CD	±1/2	±1/2	±0.4
Ceramic Dip	-55 to +125°C	MP7633SD	±2	±2	±0.4
Ceramic Dip	-55 to +125°C	MP7633SD/883	±2	±2	±0.4
Ceramic Dip	-55 to +125°C	MP7633TD	±1	±1	±0.4
Ceramic Dip	-55 to +125°C	MP7633TD/883	±1	±1	±0.4
Ceramic Dip	-55 to +125°C	MP7633UD	±1/2	±1/2	±0.4
Ceramic Dip	-55 to +125°C	MP7633UD/883	±1/2	±1/2	±0.4

PIN CONFIGURATIONS



16 Pin CDIP, PDIP (0.300")
D16, N16

16 Pin SOIC (Jedec, 0.300")
S16

20 Pin PLCC
P20



PIN OUT DEFINITIONS

16 Pin CDIP, PDIP, SOIC

PIN NO.	NAME	DESCRIPTION
1	I _{OUT1}	Current Output 1
2	I _{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5
9	BIT 6	Data Input Bit 6
10	BIT 7	Data Input Bit 7
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10 (LSB)
14	V _{DD}	Positive Power Supply
15	V _{REF}	Reference Input Voltage
16	R _{FB}	Internal Feedback Resistor

20 Pin PLCC

PIN NO.	NAME	DESCRIPTION
1	N/C	No Connection
2	I _{OUT1}	Current Output 1
3	I _{OUT2}	Current Output 2
4	GND	Ground
5	BIT 1	Data Input Bit 1 (MSB)
6	N/C	No Connection
7	BIT 2	Data Input Bit 2
8	BIT 3	Data Input Bit 3
9	BIT 4	Data Input Bit 4
10	BIT 5	Data Input Bit 5
11	N/C	No Connection
12	BIT 6	Data Input Bit 6
13	BIT 7	Data Input Bit 7
14	BIT 8	Data Input Bit 8
15	BIT 9	Data Input Bit 9
16	N/C	No Connection
17	BIT 10	Data Input Bit 10 (LSB)
18	V _{DD}	Positive Power Supply
19	V _{REF}	Reference Input Voltage
20	R _{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS

($V_{DD} = +15\text{ V}$, $V_{REF} = +10\text{ V}$ unless otherwise noted)

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
STATIC PERFORMANCE (1)								
Resolution (All Grades)	N	10			10		Bits	FSR = Full Scale Range
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL - Min INL) / 2
J, A, S				±2		±2		
K, B, T				±1		±1		
L, C, U				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
J, A, S				±2		±2		
K, B, T				±1		±1		
L, C, U				±1/2		±1/2		
Gain Error	GE		±0.3	±0.4		±0.4	% FSR	Using Internal R _{FB}
Gain Temperature Coefficient (2)	TC _{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		±5	±50		±50	ppm/%	ΔGain/ΔV _{DD} , ΔV _{DD} = ±5%
Output Leakage	I _{OUT}		<1	±10		±200	nA	I _{OUT1} V _{IN} = 0 V I _{OUT2} V _{IN} = V _{DD}
DYNAMIC PERFORMANCE (2)								
Current Settling Time	t _s		500	1000			ns	Full Scale Change to 1/2 LSB V _{REF} = 10kHz, 20 Vp-p, sinewave
AC Feedthrough at I _{OUT1}	F _T			1			mV p-p	
REFERENCE INPUT								
Input Resistance	R _{IN}	5	10	20	5	20	kΩ	V
Voltage Input Range (2)			±10	±25				
DIGITAL INPUTS (3)								
Logical "1" Voltage	V _{IH}	+2.4			+2.4		V	V _{IN} = 0 V and V _{DD}
Logical "0" Voltage	V _{IL}			+0.8		+0.8	V	
Input Leakage Current	I _{LKG}			±1.0		±1.0	μA	
ANALOG OUTPUTS								
Output Capacitance (2)	C _{OUT1}			52			pF	DAC Inputs all 1's DAC Inputs all 0's DAC Inputs all 1's DAC Inputs all 0's
	C _{OUT1}			26			pF	
	C _{OUT2}			13			pF	
	C _{OUT2}			45			pF	
Scale Factor (2)			100				μA/V _{REF}	
POWER SUPPLY (4)								
Functional Voltage Range (2)	V _{DD}	4.5	15	18	4.5	18	V	All digital inputs = 0 V or all = 5 V, 15 V
Supply Current	I _{DD}			2		2	mA	



ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

- (1) Full Scale Range (FSR) is 10V for unipolar mode.
- (2) Guaranteed but not production tested.
- (3) Digital Input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- (4) Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2) (TA = +25°C unless otherwise noted)

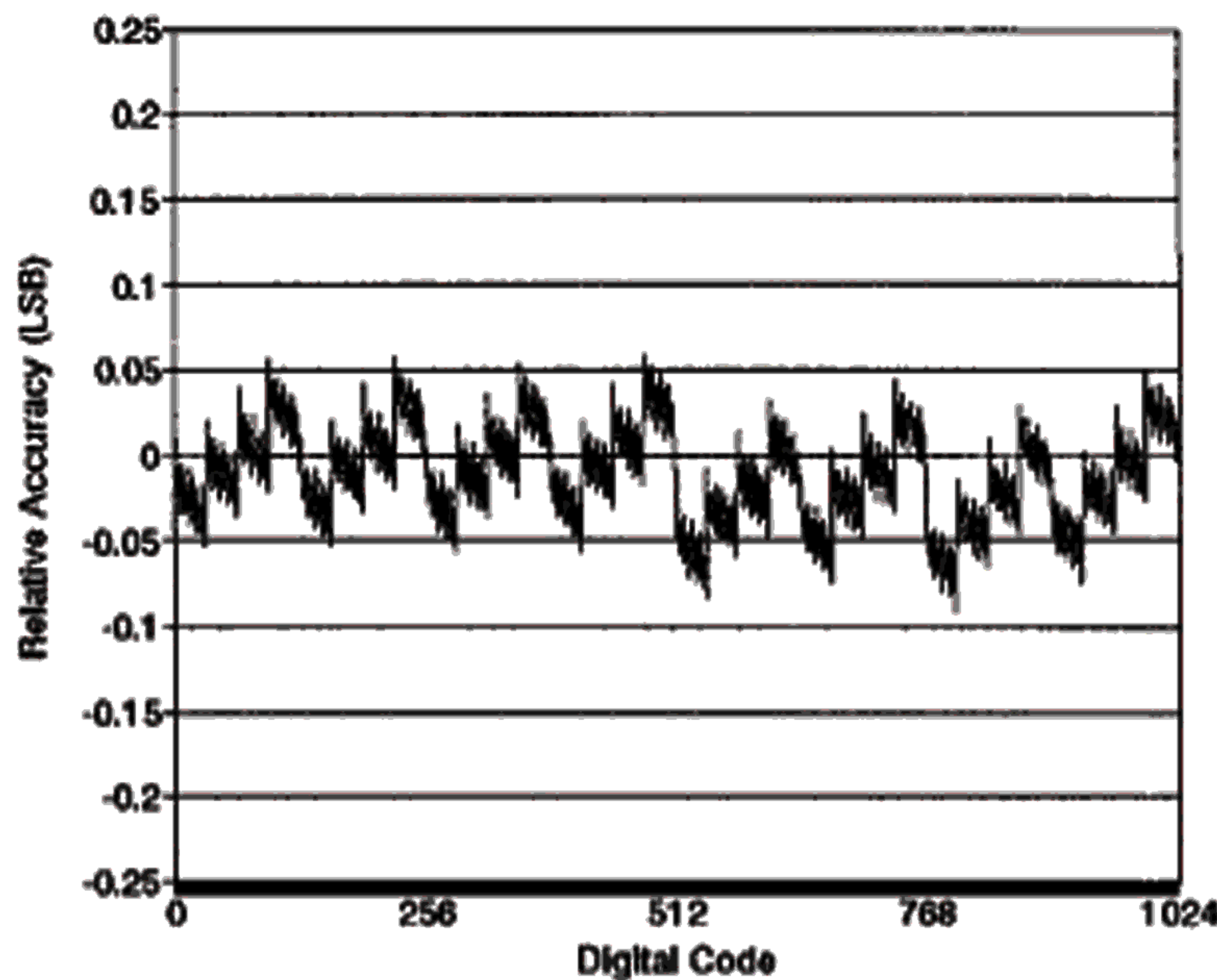
V _{DD} to GND -0.5, +17 V	Storage Temperature -65°C to +150°C
Digital Input Voltage to GND (2)	. GND -0.5 to V _{DD} +0.5 V	Lead Temperature (Soldering, 10 seconds) +300°C
I _{OUT1} , I _{OUT2} to GND (2) GND -0.5 to V _{DD} +0.5 V	Package Power Dissipation Rating to 75°C	
V _{REF} to GND ±25 V	CDIP, PDIP, SOIC, PLCC 800mW
V _{RFB} to GND ±25 V	Derates above 75°C 11mW/°C

NOTES:

- (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- (2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

4

PERFORMANCE CHARACTERISTICS



Graph 1. Relative Accuracy vs. Digital Code

APPLICATION NOTES

Refer to Section 8 for Applications Information