

# LH532600

CMOS 2M (256K × 8/128K × 16) MROM

## FEATURES

- 262,144 words × 8 bit organization (Byte mode)  
131,072 words × 16 bit organization (Word mode)
- Access time: 100 ns (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Power consumption:  
Operating: 412.5 mW (MAX.)  
Standby: 550 μW (MAX.)
- Mask-programmable control pin:  
Pin 1 = OE<sub>1</sub>/OE<sub>1</sub>/DC
- Packages:  
40-pin, 600-mil DIP  
40-pin, 525-mil SOP  
48-pin, 10 × 20 mm<sup>2</sup> TSOP (Type I)

## DESCRIPTION

The LH532600 is a 2M-bit mask-programmable ROM organized as 262,144 × 8 bits (Byte mode) or 131,072 × 16 bits (Word mode) that can be selected by BYTE input pin. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

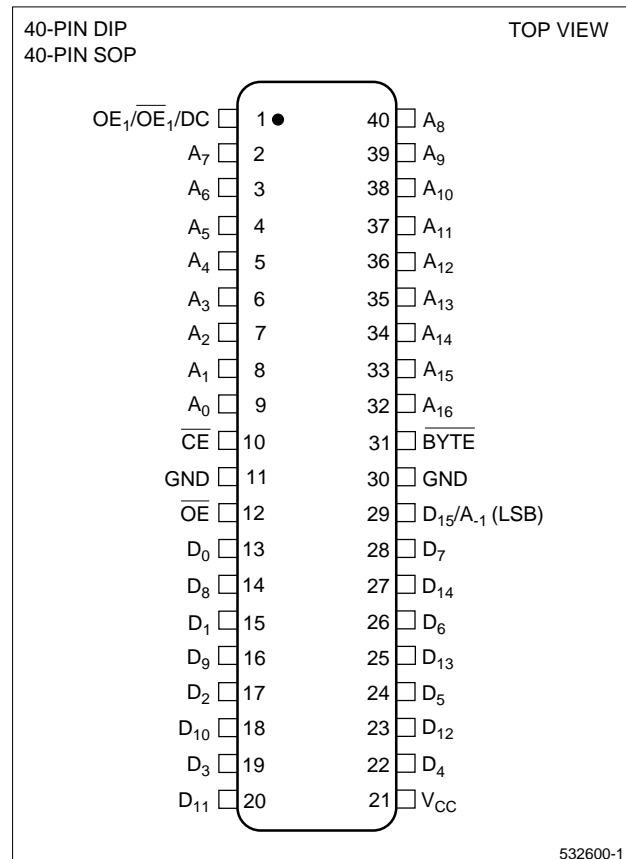
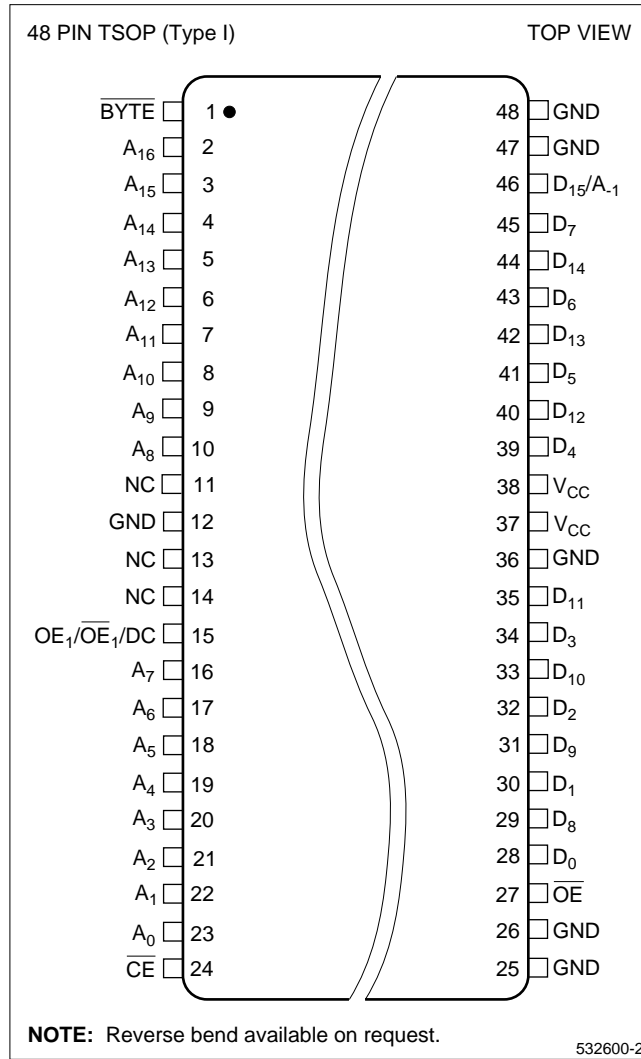


Figure 1. Pin Connections for DIP and SOP Packages



**Figure 2. Pin Connections for TSOP Package**

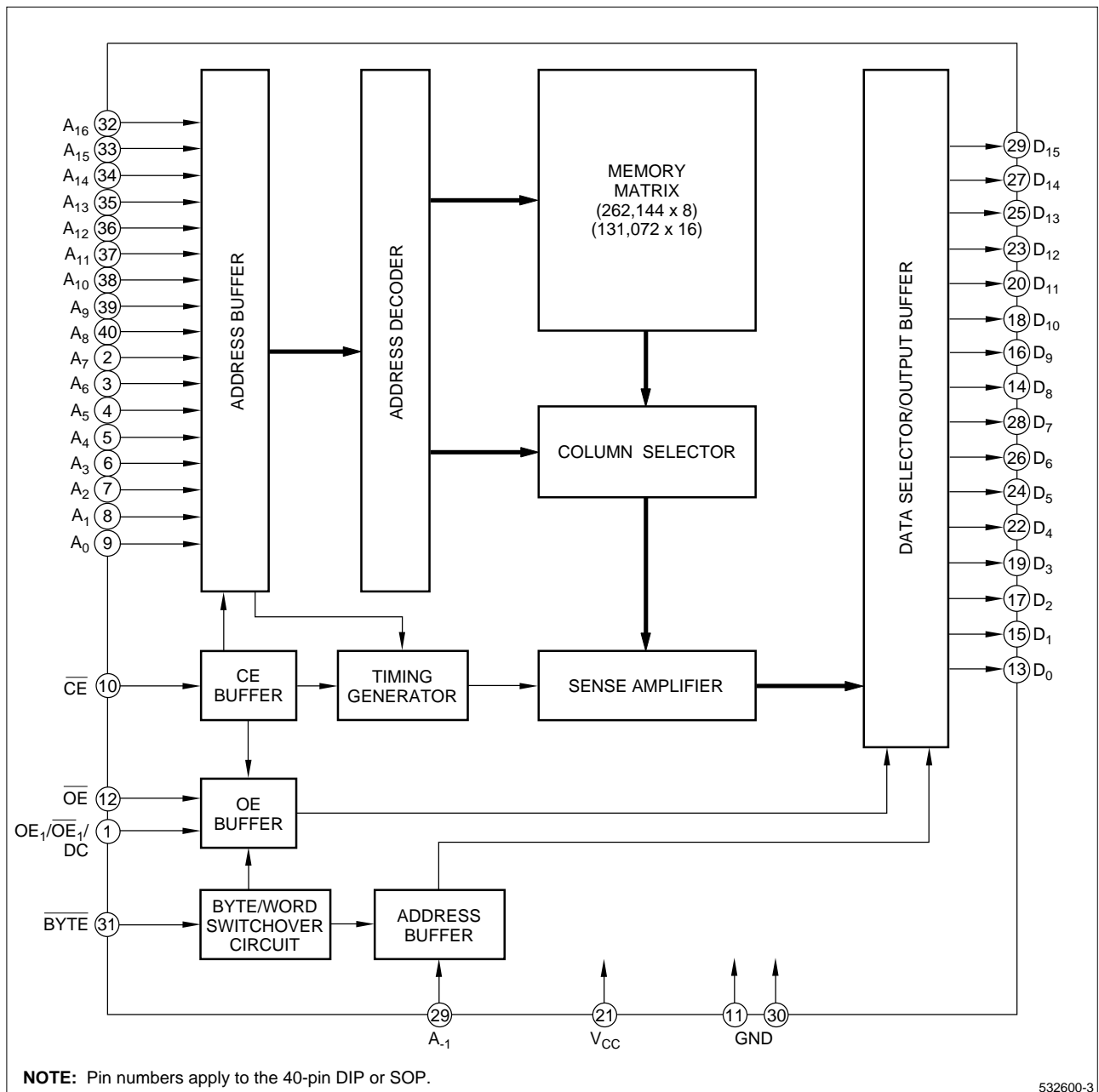


Figure 3. LH532600 Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME	NOTE
A <sub>-1</sub> – A <sub>16</sub>	Address input	1
D <sub>0</sub> – D <sub>15</sub>	Data output	1
BYTE	Byte/word mode switch	1
CE	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE	Output enable input	
OE <sub>1</sub> /OE <sub>1</sub> /DC	Output enable input	2, 3
V <sub>CC</sub>	Power supply (+5 V)	
GND	Ground	

**NOTES:**

1. The D<sub>15</sub>/A<sub>-1</sub> pin becomes LSB address input (A<sub>-1</sub>) when the  $\overline{\text{BYTE}}$  pin is set to be LOW in byte mode, and data output (D<sub>15</sub>) when set to be HIGH in word mode.
2. Active levels of OE<sub>1</sub>/OE<sub>1</sub>/DC are mask-programmable. When DC is selected out of OE<sub>1</sub>/OE<sub>1</sub>/DC, it is fixed to an active level. Then it is recommended to apply either V<sub>IH</sub> or V<sub>IL</sub> to the DC pin.
3. DC = Don't care.

## TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$OE_1/\overline{OE}_1$	$\overline{BYTE}$	$A_{-1}$ ( $D_{15}$ )	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					$D_0 - D_7$	$D_8 - D_{15}$	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	–	–	Standby
L	H	X	X	X	High-Z	High-Z	–	–	Operating
L	X	L/H	X	X	High-Z	High-Z	–	–	Operating
L	L	H/L	H	–	$D_0 - D_7$	$D_8 - D_{15}$	$A_0$	$A_{16}$	Operating
L	L	H/L	L	L	$D_0 - D_7$	High-Z	$A_{-1}$	$A_{16}$	Operating
L	L	H/L	L	H	$D_8 - D_{15}$	High-Z	$A_{-1}$	$A_{16}$	Operating

## NOTE:

X = H or L, High-Z = High-impedance

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	$V_{CC}$	–0.3 to +7.0	V
Input voltage	$V_{IN}$	–0.3 to $V_{CC} + 0.3$	V
Output voltage	$V_{OUT}$	–0.3 to $V_{CC} + 0.3$	V
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V

DC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	$V_{IH}$		2.2	$V_{CC} + 0.3$	V	
Input 'Low' voltage	$V_{IL}$		–0.3	0.8	V	
Output 'High' voltage	$V_{OH}$	$I_{OH} = -400\ \mu\text{A}$	2.4		V	
Output 'Low' voltage	$V_{OL}$	$I_{OL} = 2.0\ \text{mA}$		0.4	V	
Input leakage current	$ I_{LI} $	$V_{IN} = 0\ \text{V}$ to $V_{CC}$		10	$\mu\text{A}$	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\ \text{V}$ to $V_{CC}$		10	$\mu\text{A}$	1
Operating current	$I_{CC1}$	$t_{RC} = 100\ \text{ns}$		75	mA	2
	$I_{CC2}$	$t_{RC} = 1\ \mu\text{s}$		65	mA	2
	$I_{CC3}$	$t_{RC} = 100\ \text{ns}$		70	mA	3
	$I_{CC4}$	$t_{RC} = 1\ \mu\text{s}$		60	mA	3
Standby current	$I_{SB1}$	$\overline{CE} = V_{IH}$		3	mA	
	$I_{SB2}$	$\overline{CE} = V_{CC} - 0.2\ \text{V}$		100	$\mu\text{A}$	
Input capacitance	$C_{IN}$	$f = 1\ \text{MHz}$		10	pF	
Output capacitance	$C_{OUT}$	$T_A = 25^\circ\text{C}$		10	pF	

## NOTES:

- $CE/OE/OE_1 = V_{IH}$ ,  $OE_1 = V_{IL}$
- $V_{IN} = V_{IH}$  or  $V_{IL}$ ,  $CE = V_{IL}$ , outputs open
- $V_{IN} = (V_{CC} - 0.2\ \text{V})$  or  $0.2\ \text{V}$ ,  $CE = 0.2\ \text{V}$ , outputs open

**AC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	$t_{RC}$	100		ns	
Address access time	$t_{AA}$		100	ns	
Chip enable access time	$t_{ACE}$		100	ns	
Output enable delay time	$t_{OE}$		55	ns	
Output hold time	$t_{OH}$	5		ns	
CE to output in High-Z	$t_{CHZ}$		55	ns	1
OE to output in High-Z	$t_{OHZ}$				

**NOTE:**

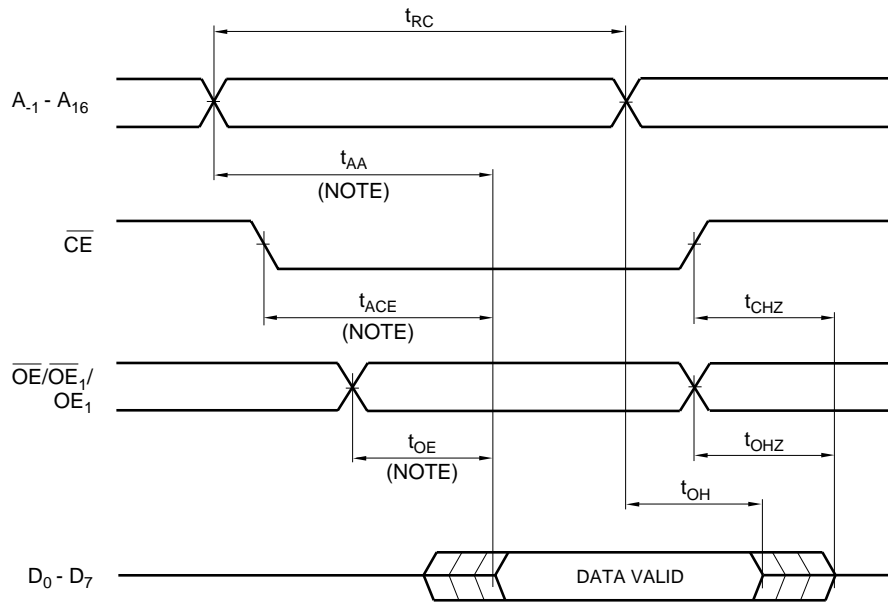
1. This is the time required for the outputs to become high-impedance.

**AC TEST CONDITIONS**

PARAMETER	RATING
Input voltage amplitude	0.4 to 2.6 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF

**CAUTION**

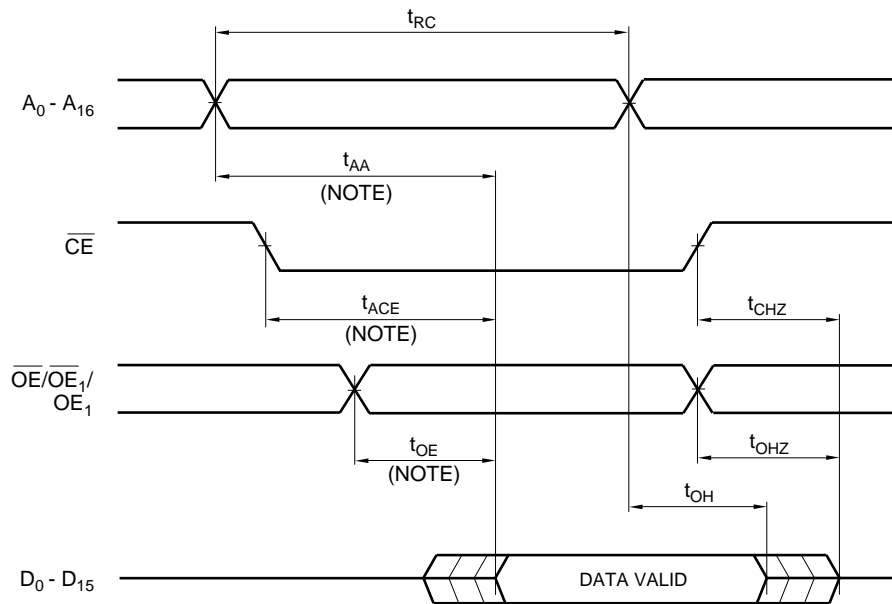
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the  $V_{CC}$  pin and the GND pin.



**NOTE:** The output data becomes valid when the last intervals,  $t_{AA}$ ,  $t_{ACE}$ , or  $t_{OE}$ , have concluded.

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**Figure 4. Byte Mode (BYTE = V<sub>IL</sub>)**

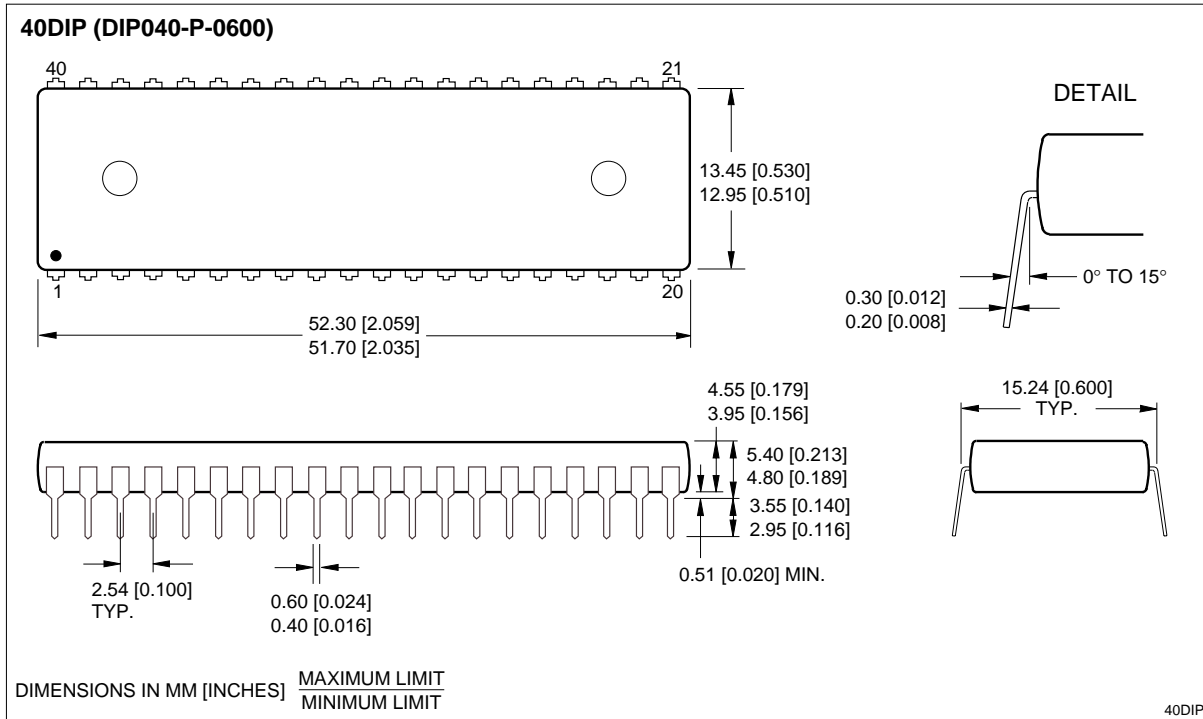


**NOTE:** The output data becomes valid when the last intervals,  $t_{AA}$ ,  $t_{ACE}$ , or  $t_{OE}$ , have concluded.

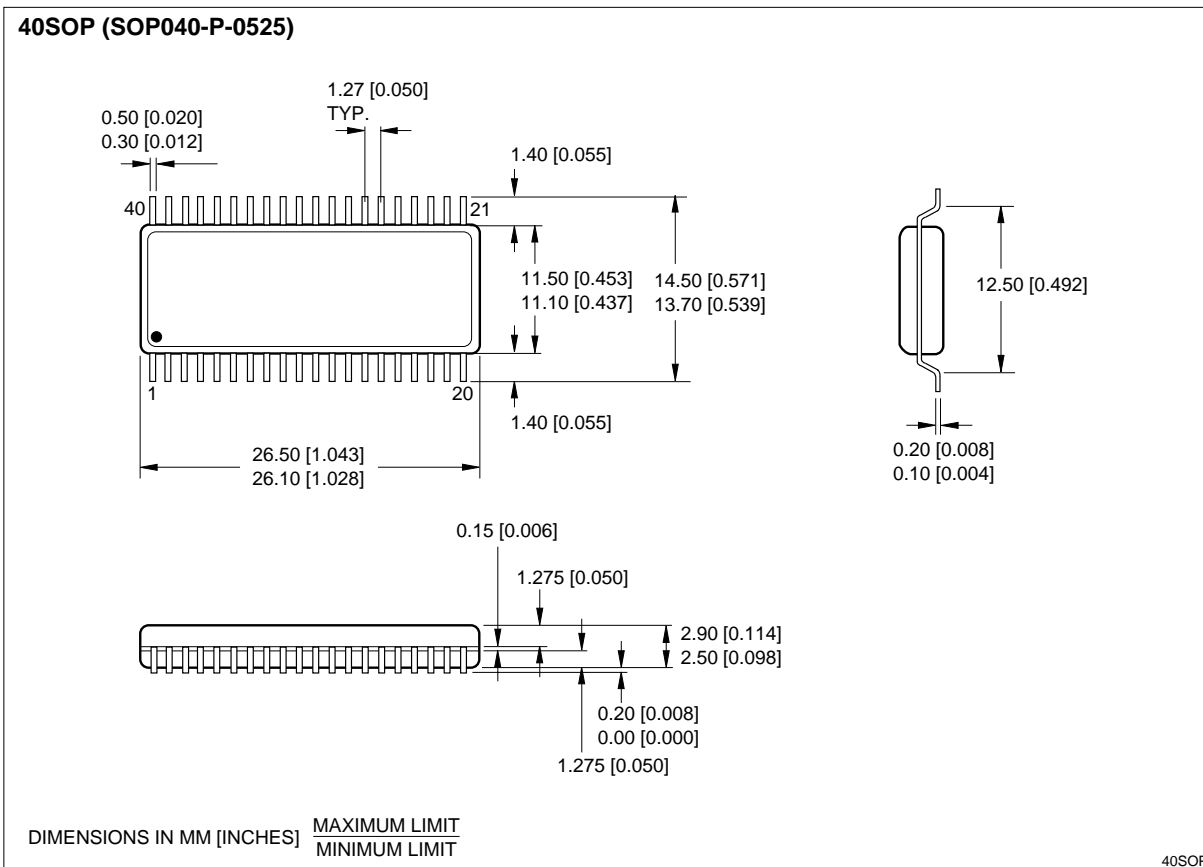
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**Figure 5. Word Mode (BYTE = V<sub>IH</sub>)**

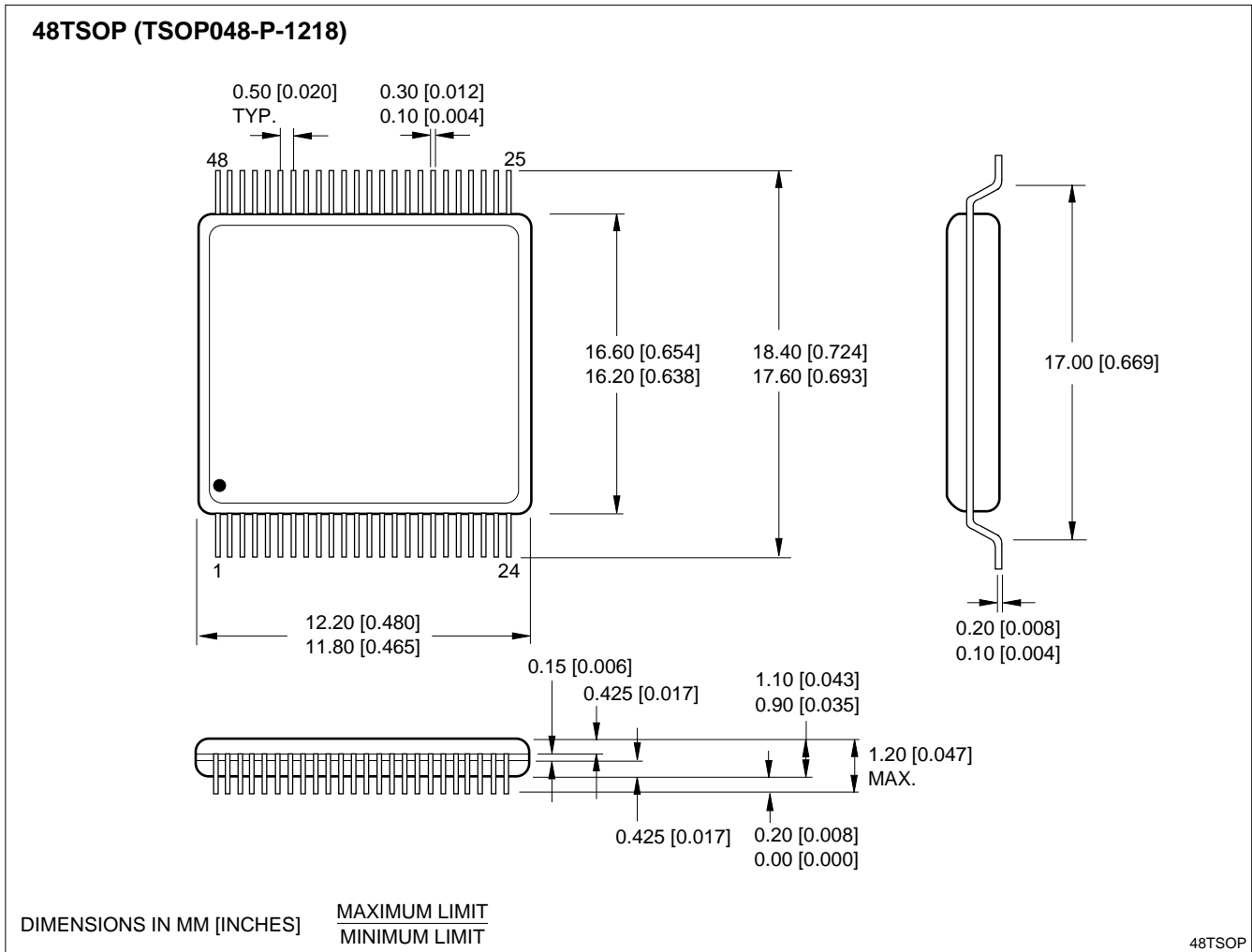
PACKAGE DIAGRAMS



40-pin, 600-mil DIP



40-pin, 525-mil SOP



**48-pin, 10 × 20 mm<sup>2</sup> TSOP (Type I)**

**ORDERING INFORMATION**

