LXT331

Dual T1/E1 Line Interface Unit

General Description

The LXT331 is a Dual Line Interface Unit (DLIU) optimized for North America 1.544 Mbps (T1) and international 2.048 Mpbs (E1/CEPT) applications. It features a constant low output impedance transmitter for high return loss. Transmit pulse shape is selectable for various line lengths and cable types. The data recovery circuit also offers selectable slicer ratios for T1 or E1 applications.

The LXT331 offers both a serial interface (SIO) for microprocessor control and a hardware control mode for standalone operation.

The LXT331 offers a variety of advanced diagnostic and performance monitoring features. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

Applications

- Digital Access and Cross-connect Systems (DACS)
- T1 / E1 Multiplexer
- SONET/SDH Multiplexers
- Digital Loop Carrier (DLC) terminals
- Cost efficient analog frontend for Digital Backend ASICS
- Analog LOS using PMRK/NMRK

Features

- Complete line driver and data recovery functions
- Constant low output impedance transmitter with programmable equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- High transmit and receive return loss
- Meets or exceeds industry specifications including ITU G.703 and ANSI T1. 102-1993
- Compatible with industry standard framers
- Minimum receive signal of 500 mV, with selectable slicer levels (E1/DSX-1) to improve SNR
- Analog loopback function
- Transmit performance monitors with Driver Fail Monitor (DFM) output for transmit driver short circuit detection
- Transmit Driver Performance Monitor (DPM) output with external monitor pins MTIP and MRING
- Available in 44-pin PLCC and 44-pin QFP

LXT331 Block Diagram
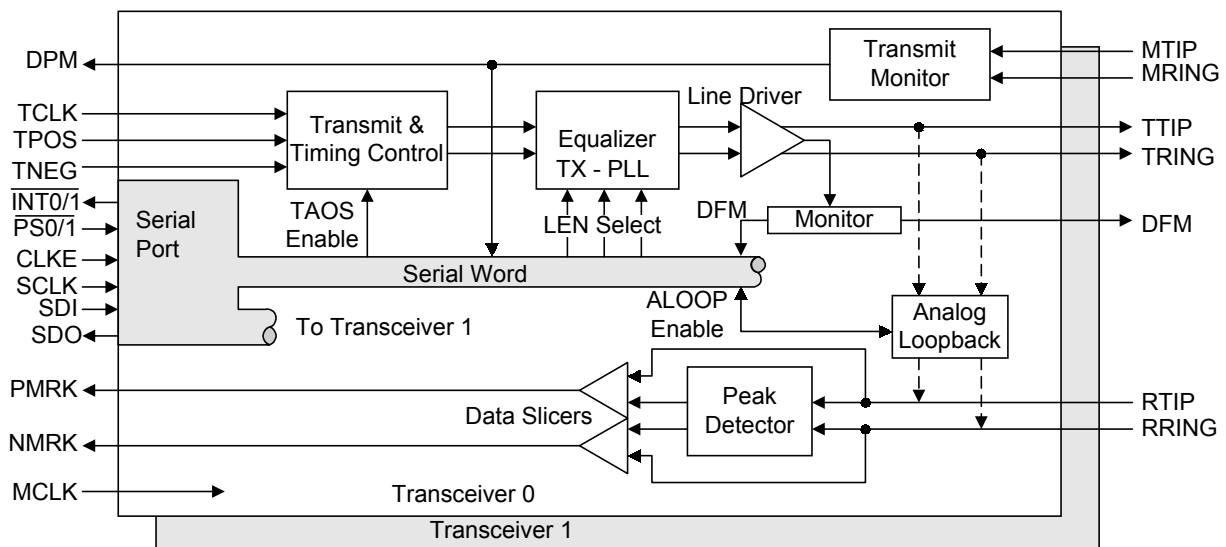
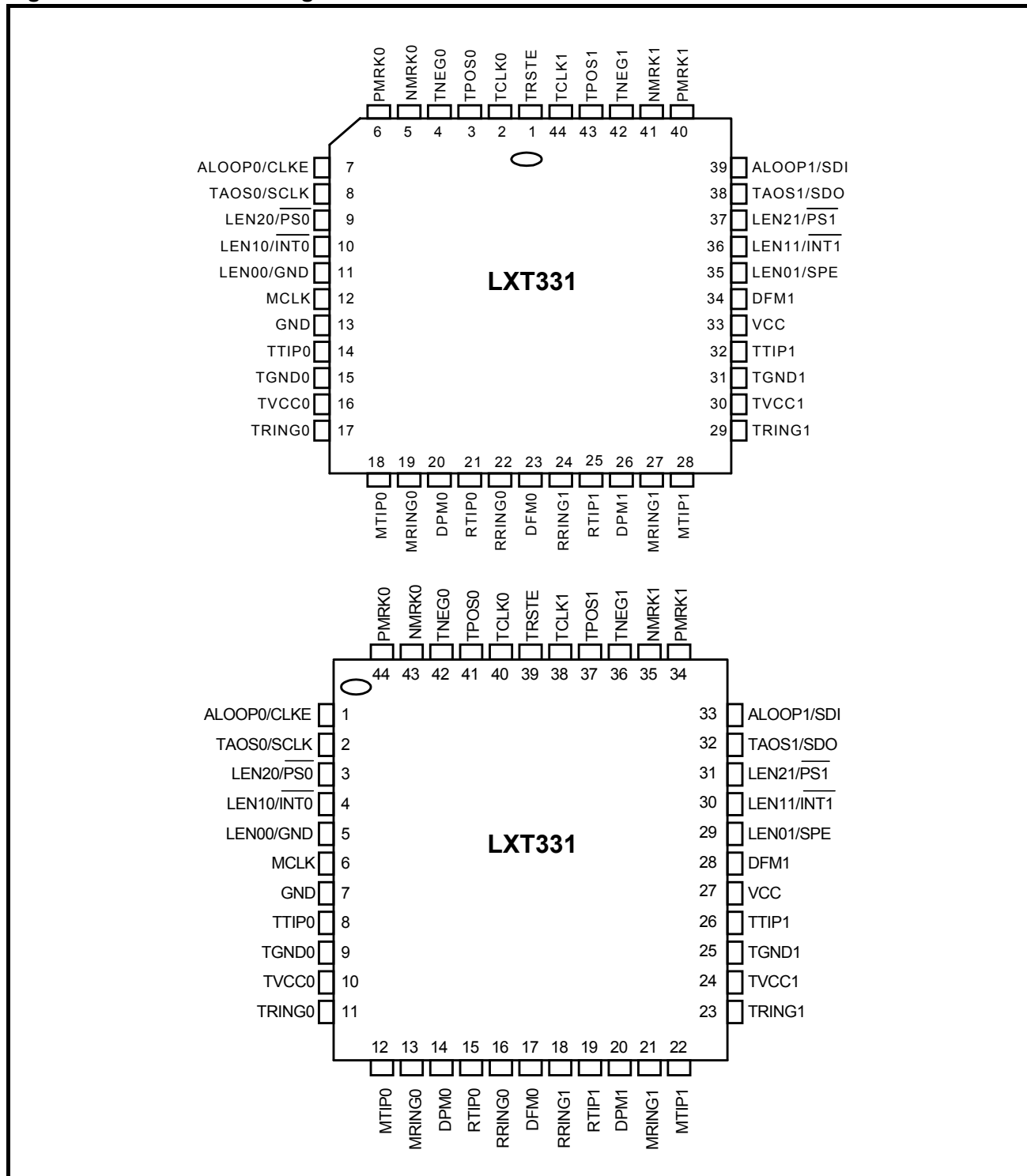# PIN ASSIGNMENTS & SIGNAL DESCRIPTION

Figure 1: LXT331 Pin Assignments

Table 1: Pin Descriptions

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
1	39	TRSTE	DI	**Tristate Enable**. Forces all output pins to tri-state when held High and forces chip into reset mode. Holds reset mode for 6 μs after TRSTE returns Low.
2	40	TCLK0	DI	**Transmit Clock — Port 0**. 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK. If TCLK0 is pulled Low, the transmit drivers are powered down and TTIP0 and TRING0 transmit outputs go to a high impedance state.
3 4	41 42	TPOS0 TNEG0	DI DI	**Transmit Positive and Negative Data — Port 0**. These pins are the positive and negative sides of a bipolar input pair for port 0. Data to be transmitted onto the line is input at these pins.
5 6	43 44	NMRK0 PMRK	DO DO	**Receive Negative and Positive Marks — Port 0**. These pins are the data outputs from port 0. A signal on NMRK corresponds to receipt of a negative pulse on RTIP/RRING. A signal on PMRK corresponds to receipt of a positive pulse on RTIP/RRING. NMRK/PMRK outputs are Return-to-Zero (RZ).
12	6	MCLK	DI	**Master Clock (1.544 MHz for T1. 2.048 MHz for E1)**. Can be held Low if TCLK is present.
13	7	GND	S	**Ground.** Ground return for power supply VCC.
14	8	TTIP0	AO	**Transmit Tip — Port 0**. The tip and ring pins for each port are differential driver outputs designed to drive a 35-200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height.
15	9	TGND0	S	**Ground**. Ground return for supply TVCC0.
16	10	TVCC0	S	**+ 5 volt power supply input for the port 0 transmit driver**. TVCC0 must not vary from TVCC1 or VCC by more than ± 0.3 V.
17	11	TRING0	AO	**Transmit Ring — Port 0**. The tip and ring pins for each port are differential driver outputs designed to drive a 35-200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height.
18 19	12 13	MTIP0 MRING0	AI AI	**Monitor Tip and Ring — Port 0**. These pins monitor tip and ring outputs, either its own or those of an adjacent LXT331 on the same board. If the application does not use this feature, tie one of these pins to a clock source and the other to a mid-level (referenced to the clock signal) voltage. (The clock frequency can range from 100 kHz to the TCLK frequency).
20	14	DPM0	DO	**Driver Performance Monitor — Port 0**. Output goes High on detection of 63 consecutive zeros, and goes Low on receipt of a one on transmit monitor loop (MTIP/MRING).
21 22	15 16	RTIP0 RRING0	AI AI	**Receive Tip and Ring — Port 0**. RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a 1:1 transformer.
23	17	DFM0	DO	**Driver Fail Monitor — Port 0**. Signal goes High to indicate driver output short.
24 25	18 19	RRING1 RTIP1	AI AI	**Receive Tip and Ring — Port 1**. Refer to pins RRING0 and RTIP0.
26	20	DPM1	DO	**Driver Performance Monitor — Port 1**. Refer to pin 20.
27 28	21 22	MRING1 MTIP0	AI	**Monitor Ring and Tip — Port 1**. Refer to pins MRING0 and MTIP0.
29	23	TRING1	AO	**Transmit Ring — Port 1**. Refer to pin TRING0.
30	24	TVCC1	DI	**+ 5 volt power supply** input for the port 0 transmit driver. TVCC1 must not deviate from TVCC0 or VCC by more than ± 0.3 V.
31	25	TGND1	S	**Ground**. Ground return for power supply TVCC1.
32	26	TTIP1	AO	**Transmit Tip — Port 1**. Refer to pin TTIP0.

LEVEL ONE.

Table 1: Pin Descriptions – continued

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
33	27	VCC	DI	**+ 5 VDC power supply** input for all circuits except the transmit drivers.
34	28	DFM1	DO	**Driver Fail Monitor — Port 1**. Refer to pin DFM0.
40 41	34 35	PMRK1 NMRK1	DO	**Receive Negative and Positive Marks — Port 1**. Refer to pins PMRK0 and NMRK0.
42 43	36 37	TNEG1 TPOS1	DI DI	**Transmit Negative and Positive Data — Port 1**. Refer to pins TNEG0 and TPOS0.
44	38	TCLK1	DI	**Transmit Clock — Port 1**. Refer to pin TCLK0.

Table 2: Host Mode Pin Descriptions

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
7	1	CLKE	DI	**Clock Edge Select**. When CLKE is High, SDO is valid on the rising edge of SCLK.When CLKE is Low, SDO is valid on the falling edge of SCLK.
8	2	SCLK	DI	**Serial Clock**. Shifts data into or our from the serial interface register of the selected port.
9	3	$\overline{PS0}$	DI	**Port Select — Port 0**. Inputs access the serial interface registers for the respective port. For each read or write operation, PSn must transition from High to Low, and remain Low.
10	4	$\overline{INT0}$	DO	**Interrupt — Port** 0. Outputs go Low to flag the host processor that the respective port has changed state. INT0 and INT1 are open drain outputs. Each must be tied to VCC through a resistor.
11	5	GND	S	**Ground**. Tie to ground.
35	29	SPE	DI	**Serial Port Enable**. SPE must be clocked with MCLK, TCLK0 or TCLK1 to enable Host Mode control through the serial port.
36	30	$\overline{INT1}$	DO	**Interrupt — Port 1**. Refer to pin $\overline{INT0}$.
37	31	$\overline{PS1}$	DI	**Port Select — Port 1**. Refer to pin $\overline{PS0}$.
38	32	SDO	DO	**Serial Data Output**. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK.
39	33	SD1	DI	**Serial Data Input**. SDI is sampled on the rising edge of SCLK.

1. I/O Designations: A1 = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, S = Power Supply

Table 3: Hardware Mode Pin Descriptions

Pin PLCC	Pin QFP	Symbol	I/O[1]	Description
7	1	ALOOP0	DI	**Analog Local Loopback Enable — Port 0**. When ALOOP is High, the RTIP/RRING inputs from the port 0 twisted-pair line are disconnected and the transmit data outputs (TTIP/TRING) are routed back into the receive inputs. For normal operation, hold ALOOP Low.
8	2	TAOS0	DI	**Transmit All Ones Enable — Port 0**. When TAOS is High, the TPOS/TNEG input is ignored and Port 0 transmits a stream of ones at the TCLK frequency. With no TCLK the MCLK input becomes the transmit reference. For normal operation, hold TAOS Low.
9 10 11	3 4 5	LEN20 LEN10 LEN00	DI DI DI	**Line Length Equalizer — Port 0**. Determine the shape and amplitude of the transmit pulse.
35 36 37	29 30 31	LEN01 LEN11 LEN21	DI DI DI	**Line Length Equalizer — Port 1**. Determine the shape and amplitude of the transmit pulse.
38	32	TAOS1	DI	**Transmit All Ones Enable — Port 1**. Refer to pin TAOS0.
39	33	ALOOP1	DI	**Analog Local Loopback Enable — Port 1**. Refer to pin ALOOP1.
1. I/O Designations: A1 = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, S = Power Supply				

FUNCTIONAL DESCRIPTION

The LXT331 is a Dual Line Interface Unit (DLIU), which contains two ports. Refer to the simplified block diagram on page 1. The DLIU is designed for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. Both ports operate at the same frequency, which is determined by the TCLK input.

Each DLIU port front end interfaces with two lines, one line for transmit, one line for receive. These two lines comprise a digital data loop for full duplex transmission.

Each DLIU port back-end interfaces with a layer processor through bipolar data I/O channels. The DLIU may be controlled by a microprocessor through the serial port (Host control mode), or by hard-wired pins for stand-alone operation (Hardware control mode).

Receiver

The two receivers in the LXT331 DLIU are identical. The following paragraphs describe the operation of a single receiver.

The input signal is received via a 1:1 transformer. The receiver requires fully differential inputs which are internally self-biased into 2.5 V. Recovered data is output at PMRK and NMRK. Refer to Test Specifications for receiver timing.

The receive signal is processed through an adaptive peak detector and data slicers. The peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (line length inputs LEN0-LEN2 ≠

000 or 001) the threshold is set to 70% (typical) of the peak value. This threshold is maintained above the specified level for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (LENxn inputs = 000 or 001) the threshold is 50% (typical).

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of 0.3 V (typical) to provide immunity from impulsive noise. Built in pulse stretching circuitry maintains a minimum positive and negative mark pulse width (see Table 15 and Figure 14 on page 105).

Transmitter

The two transmitters in the LXT331 DLIU are identical. The following paragraphs describe the operation of a single transmitter.

Transmit data is clocked serially into the device at TPOS/TNEG. Input synchronization is supplied by the transmit clock (TCLK). The TPOS/TNEG inputs are sampled on the falling edge of TCLK. If TCLK is held Low the transmitter remains powered down and the TTIP/TRING outputs are held in a high-Z state, except during TAOS if MCLK is available. Each output driver is supplied by a separate power supply (TVCC0 or TVCC1). Current limiters on the output drivers provide short circuit protection. Refer to Test Specifications for TCLK timing characteristics. The LXT331 transmits data as a 50% AMI line code as shown in Figure 2.

Table 4: Equalizer Control Inputs - Hardware Mode[1]

| LEN2	LEN1	LEN0	Line Length[2]	Cable Loss[3]	Application	Frequency
Low	High	High	0 - 133 ft ABAM	0.6 dB		
High	Low	Low	133-266 ft ABAM	1.2 dB		
High	Low	High	266-399 ft ABAM	1.8 dB	DSX-1	1.544 MHz
High	High	Low	399-533 ft ABAM	2.4 dB		
High	High	High	533-655 ft ABAM	3.0 dB		
Low	Low	Low	ITU Recommendation G.703		E1 - Coax (75 Ω)	2.048 MHz
Low	Low	High			E1 - Twisted-pair (120 Ω)	
Low	High	Low	FCC Part 68, Option A		CSU	1.544 MHz

1. LEN*n* inputs are shown as High or Low for Hardware mode. For Host Mode serial inputs, High = 1 and Low = 0.
2. Line length from LXT331 to DSX-1 cross-connect point.
3. Maximum cable loss at 772 kHz.

Pulse Shape

The transmitted pulse shape is determined by Line Length equalizer control signals LEN0 through LEN2. Equalizer codes are hard-wired in Hardware mode as shown in Table 4. In Host mode the LEN*xn* codes are input through the serial interface. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant Low output impedance of < 3 Ω (typical) regardless of whether it is driving marks or spaces or during transitions. This well-controlled imped-ance provides excellent return loss when used with external precision resistors (±1% accuracy). See Tables 8 and 9 for recommended transformer specifications, ratios, series resistor (Rt) values, and typical return losses for various LEN*xn* codes. To minimize power consumption the DC block capacitor and LXT331 can be connected directly to a 1:1.15 transformer without series resistors.

Pulses can be shaped for either 1.544 or 2.048 Mbps appli-cations. 1.544 Mbps pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of 22 AWG ABAM cable. A combination of 9.1 Ω resistors and a 1:2.3 transformer is recommended for DSX-1 applica-tions and maximum transmit return loss. The LXT331 also matches FCC pulse mask specifications for CSU applica-tions.

Figure 2:   50% AMI Coding
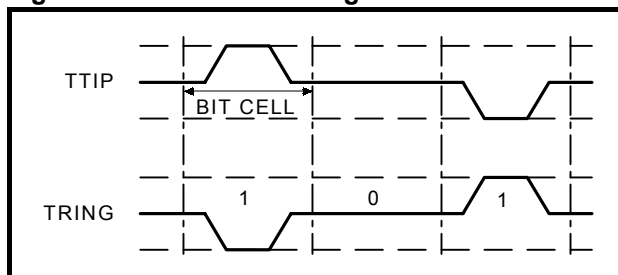
The LXT331 produces 2.048 Mbps pulses for both 75 Ω coaxial (2.37 V) or 120 Ω shielded twisted-pair (3.0 V) lines through an output transformer with a 1:2 turns ratio.

Driver Performance Monitor

The LXT331 incorporates a Driver Performance Monitor (DPM) as shown in Figure 3 on page 94. The DPM output goes High on receipt of 63 consecutive zeros and returns Low on receipt of a transition. A reset command also drives the output signal Low.

The LXT331 uses its MTIP and MRING pins to monitor its own TTIP and TRING outputs or those of an adjacent chip. Mark detection involves two measures:

3. Voltage threshold: a pulse must trip a threshold voltage above or below (depending on its polarity) the input bias voltage level. The LXT331 bias voltage is 2.5 V and the threshold for a mark is 2.5 ± 0.79 V.

4. Pulse width: the monitor distinguishes between marks and noise pulses by the pulse width. LXT331 requires a mark pulse to be at least 120 ns wide (typically).

There are two type of marks: Figure 2 labels them "A" and "B". C1 and C2 detect "A" marks; the AND gate (A1) ensures that both mark signals are present at the same time. If the pulse widths are adequate, with both a positive mark on MTIP and a negative mark on MRING, the A1 output goes High. Likewise C3 and C4 detect "B" marks. If the pulse meets the minimum width requirement, the AND gate (A2) output goes High when there are both a negative mark on MTIP and a positive mark on MRING. The OR gate (O1) passes the mark, as the signal "zero", on to the clock/counter circuit which controls the DPM output.

A latch samples the counter which goes High if the DPM circuit sees 63 consecutive zeros. Any mark resets the counter.   The DPM signal goes High after the 63rd zero.

Driver Failure Monitor

The transceiver incorporates an internal Driver Failure Monitor (DFM) in parallel with TTIP and TRING. A capacitor, charged via a measure of the driver output cur-rent and discharged by a measure of the maximum allow-able current detects driver failure. Shorted lines draw excess current, overcharging the cap. When the capacitor charge deviates outside the nominal charge window, a driver failure is reported. In Host mode the DFM bit is set in the serial word. In both Hardware and Host modes the DFM pin goes High. During a long string of spaces, a short-induced overcharge eventually bleeds off, clearing the DFM flag.

Control Modes

The LXT331 transceiver operates in standalone Hardware (default) Mode or Host Mode depending on the input to pin 35. When pin 35 is clocked by MCLK, TCLK0 or TCLK1, it acts as a Serial Port Enable (SPE) signal to force the LXT331 into the Host mode.

Host Mode Control

The LXT331 operates in the Host mode when pin 35 (SPE) is clocked. In Host mode a microprocessor controls the LXT331 through the serial I/O port (SIO) which provides common access to both LIUs. Each of the two LIUs contains a pair of data registers, one for command inputs and one for status outputs. An SIO transaction is initiated by a falling pulse on one of the two Port Select pins, $\overline{PS0}$ or $\overline{PS1}$. Only one LIU can be selected at a time. A High-to-Low transition on PS*n* is required for each subsequent access to the Host mode registers. If both $\overline{PS0}$ and $\overline{PS1}$ are active simultaneously, Port 0 has priority over Port1.

The LIU addressed by the $\overline{PSn}$ pulse responds by writing the incoming serial word from the SDI pin into its command register. Figure 4 on page 95 shows an SIO write operation. The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte. If the command word contains a read request, the addressed LIU subsequently outputs the contents of its status register onto the SDO pin.

Figure 5 on page 96 shows an SIO read operation. The Clock Edge(CLKE) signal determines when the SDO output is valid, relative to the Serial Clock (SCLK) as follows:

If CLKE = High, SDO is valid on the rising edge of SCLK.
If CLKE = Low, SDO is valid on the falling edge of SCLK.
Refer to Test Specifications for SIO timing.

Serial Input Word

Figure 4 shows the Serial Input data structure. The LXT331 is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. Bit 1 of the serial Address/Command byte provides Read/Write (R/W) control when the chip is accessed. The R/W bit is set to logic 1 to read the data output byte from the chip, and set to logic 0 to write the input data byte to the chip.

The second 8 bits of a write operation, the Data Input byte, clear the Driver Performance Monitor (DPM) and Driver Fail Monitor (DFM) interrupts, reset the chip, and control diagnostic modes. The first and second bits (D0-1) clear and/or mask the DPM and DFM interrupts, and the last 2 bits (D6-7) control operating modes (normal and diagnostic) and chip reset. Refer to Table 5 for details on bits D6-7.

Table 5: SIO Input Bit Settings (See Figure 4)

Mode	TST Bit D5	ALOOP Bit D6	TAOS Bit D7
ALOOP	0	1	0
TAOS	0	X	1
RESET	1	1	0

Figure 3: LXT331 Driver Performance Monitor
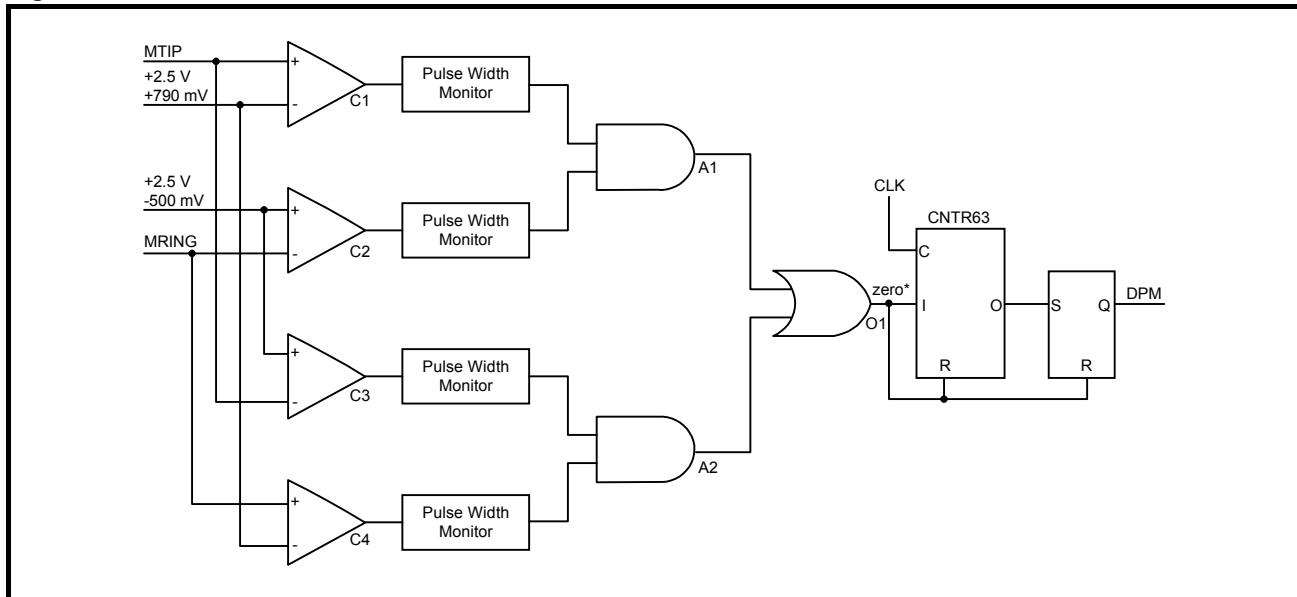
Serial Output Word

Figure 5 shows the Serial Output data structure. SDO is high impedance when SDI receives an Address/Command byte. If SDI receives a write command (R/$\overline{W}$ = 0), SDO remains in high impedance. If the command is a read (R/$\overline{W}$ = 1), then SDO becomes active after the last Command/ Address bit (A6) and remains active for eight SCLK cycles. Typically the first bit out of SDO changes the state of SDO from high Z to a Low/High. This occurs approximately 100 ns after the eighth following edge of SCLK.

The output data byte reports DPM and DFM conditions, equalizer settings, and operating modes (normal or diagnostic). The first 5 bits (D0-4) report DPM and DFM status and the Line Length Equalizer settings. The last 3 bits (D5-7) report operating modes and interrupt status as defined in Table 6 on page 96.

If the $\overline{INT}$ line for the respective port is High (no interrupt is pending), bits D5-7 report the operating modes listed in Table 6 on page 96. If the $\overline{INT}$ line for the respective port is Low, the interrupt status overrides all other reports and bits D5-7 reflect the interrupt status as listed in Table 6.

Interrupt Handling

The Host mode provides two latched Interrupt output pins, $\overline{INT0}$ and $\overline{INT1}$, one for each LIU. An interrupt is triggered by a change in the DPM or DFM bit (D0=DPM, D1=DFM). As shown in Figure 6, either or both interrupt generators can be masked by writing a 1 to the corresponding bit (D0 or D1) of the input data byte. When an interrupt has occurred, the $\overline{INT}$ output pin is pulled Low. The output stage of each $\overline{INT}$ pin consists only of a pull-down device. Hence, an external pull-up resistor is required. Clear the interrupts as follows:

1. If one or both interrupt bits (DPM or DFM - D0 or D1 of the output data byte) are high, write a 1 to the corresponding bit of the input data byte to clear the interrupt. Leave a 1 in either bit position to effectively mask that interrupt. To re-enable the interrupt capability, reset either D0 or D1 or both to 0.

2. If neither DPM nor DFM is high, reset the chip to clear the interrupt. To reset the chip, set data input bits D5 and D6 = 1, and D7 = 0.

Figure 4:   LXT331 SIO Write Operations
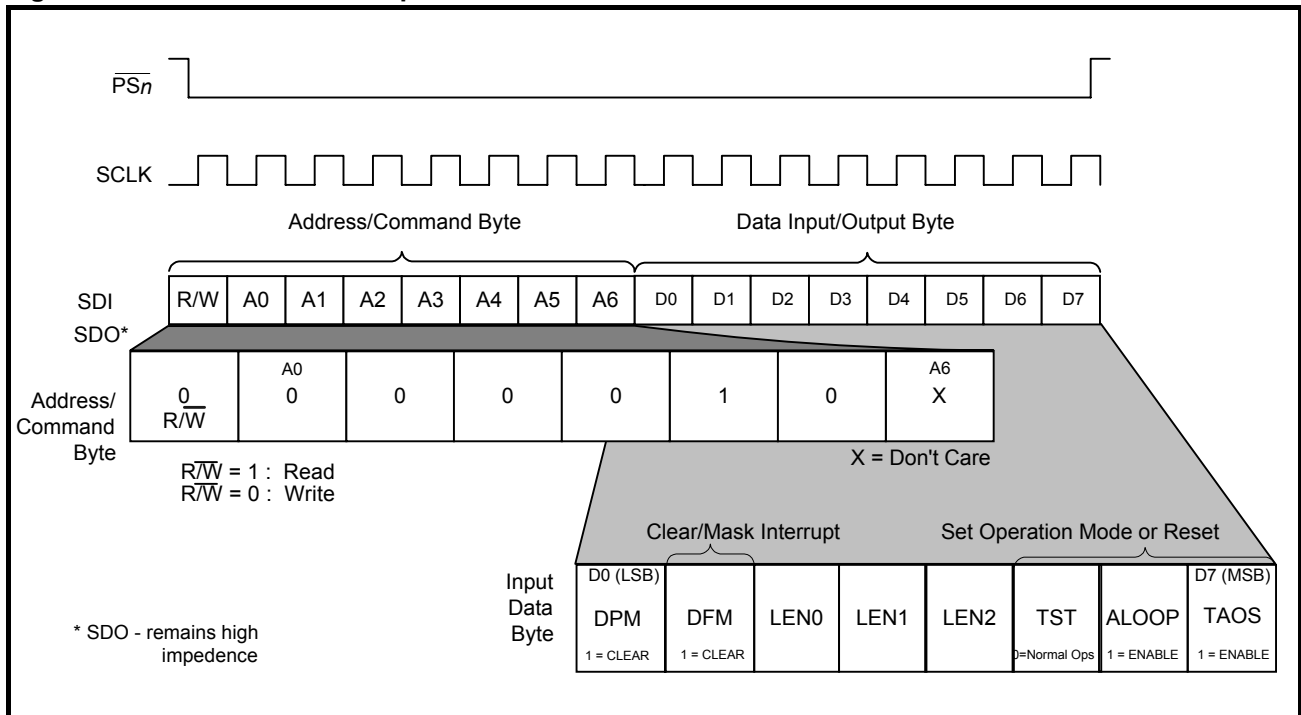
Figure 5: LXT331 SIO Read Operation
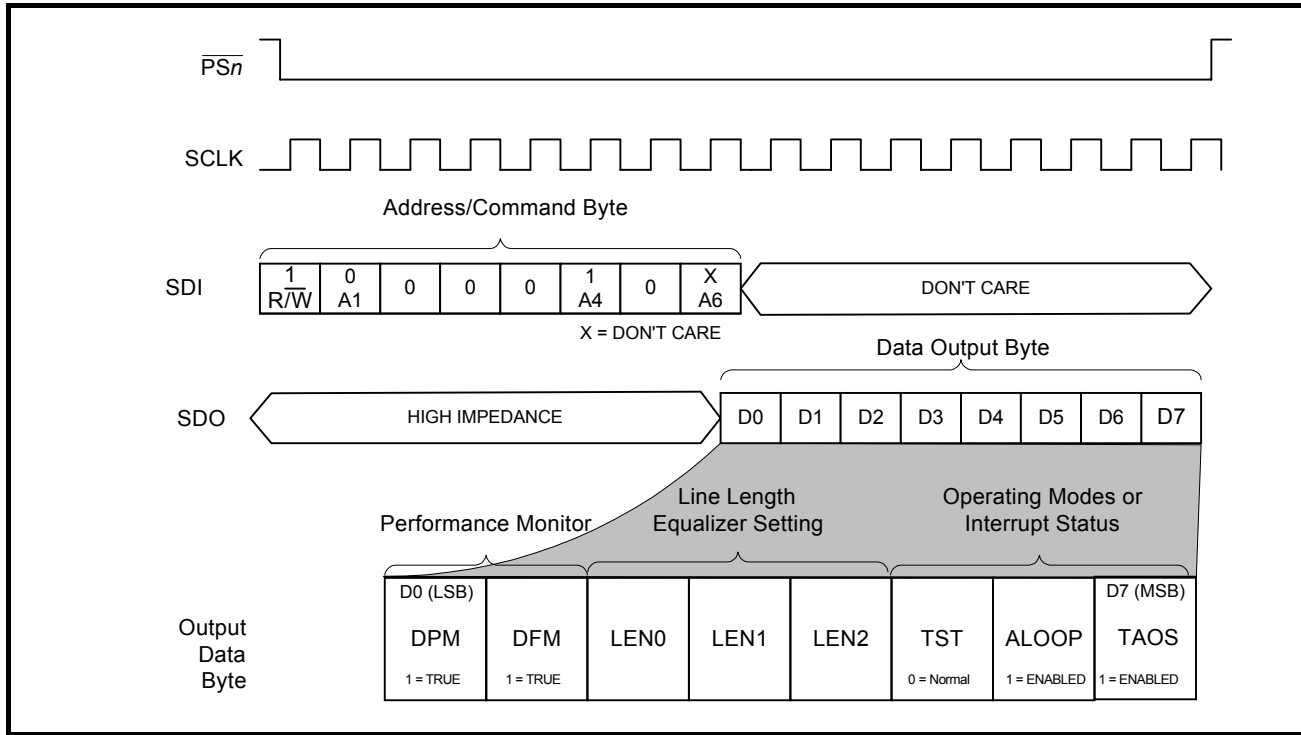
Table 6: LXT331 Serial Data Output Bit Coding

Bit D5	Bit D6	Bit D7	Operating Modes
0	0	0	Reset has occurred, or no program input (i.e. normal operation).
0	0	1	TAOS active
0	1	0	ALOOP active
0	1	1	TAOS and ALOOP active
Bit D5	**Bit D6**	**Bit D7**	**Interrupt Status**
1	0	1	DFM has changed state since the last Clear DFM occurred
1	1	0	DPM has changed state since the last Clear DPM occurred
1	1	1	DPM and DFM have changed state since the last Clear DPM and DMF occurred

Figure 6: LXT331 Interrupt Handling
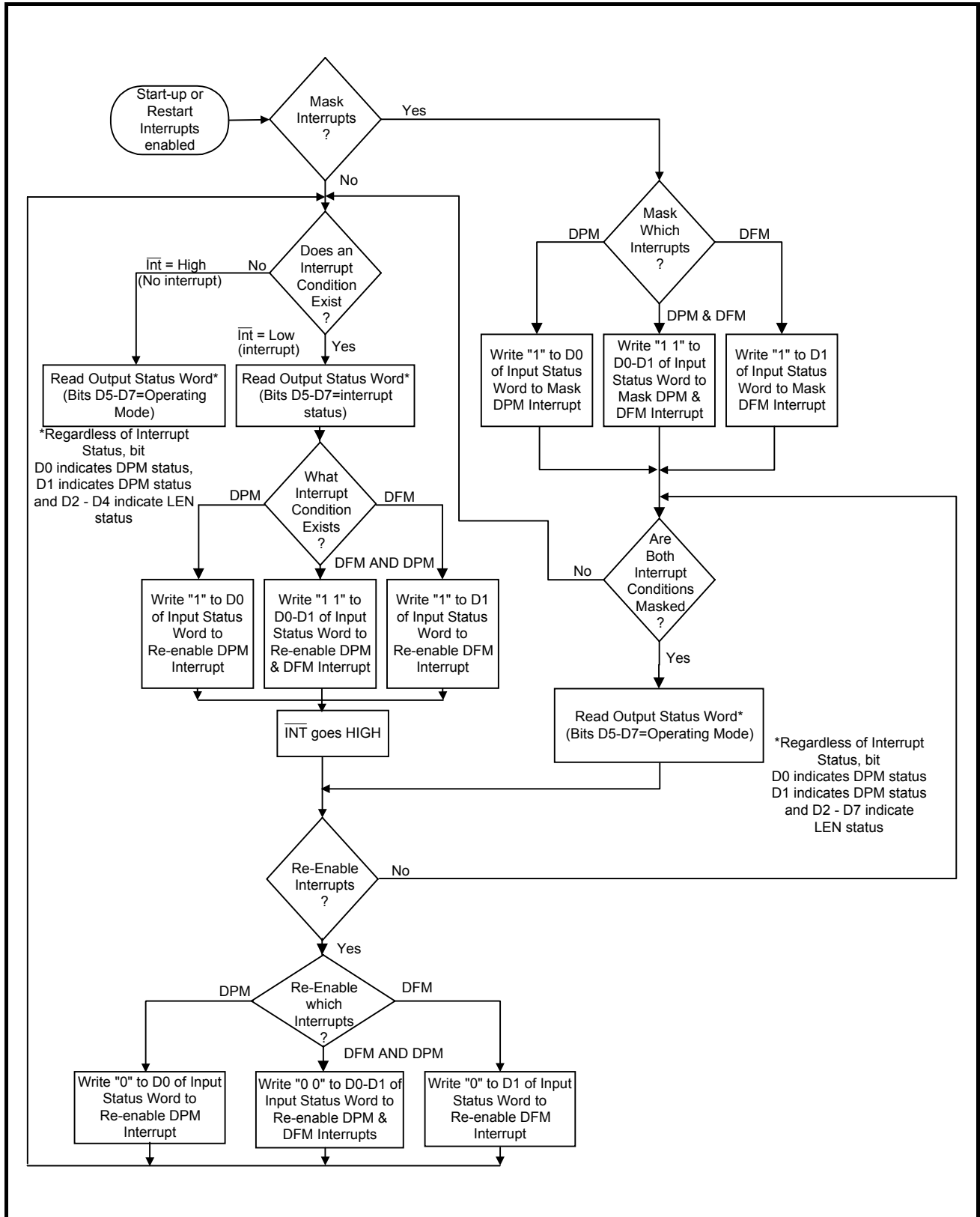
Hardware Mode Control

Hardware control is the default operating mode; the LXT331 operates in Hardware mode unless pin 35 (LEN21/SPE) is clocked. In Hardware mode the transceiver is controlled through individual pins; a μP is not required. The SIO pins are re-mapped to provide control functions. In Hardware mode the PMRK/NMRK outputs are valid on the rising edge of RCLK.

Diagnostic Mode Operation

The LXT331 offers two diagnostic modes. Analog Loopback (ALOOP) and Transmit All Ones (TAOS) are available under both Host and Hardware control modes.

In Host mode, diagnostic modes are selected by writing the appropriate SIO bits. In Hardware mode, diagnostic modes are selected by a combination of pin settings. The pins must be held at the specified levels for a minimum of 20 ns (typically). Table 7 lists Hardware Mode control settings for the various diagnostic modes.

Transmit All Ones. See Figure 7. Transmit All Ones (TAOS) is selected when TAOS = 1. In TAOS mode the TPOS and TNEG inputs are ignored, but the transmitter remains locked to the TCLK input. When TAOS is selected, the transceiver transmits a continuous stream of 1s at the TCLK frequency. If TCLK is not supplied, MCLK is used as the transmit reference. TAOS and Analog Loopback can be selected simultaneously as shown in Figure 8.

Analog Loopback. See Figure 9. Analog Loopback (ALOOP) is selected when ALOOP = 1. In ALOOP mode the receive line input (RTIP/RRING) is blocked. The transmit outputs (TTIP and TRING) are looped back through the receiver input and output at PMRK and NMRK. The transmitter circuits are unaffected by ALOOP. Transmitting onto an improperly terminated line may produce unexpected pulse widths at PMRK and NMRK.

Tri-State. By holding pin 1 (TRSTE) High for at least 200 ns all output drivers (both digital and analog) go to high Z state and the chip logic goes into a reset condition which lasts 6 μs longer than in the tri-state. All pins go to a high-Z condition, and the internal circuits go to a known condition.

Table 7: Hardware Mode Diagnostic Settings

Mode	TRSTE	ALOOP	TAOS
ALOOP	L	H	L
TAOS	L	X	H
RESET	H	X	X

Initialization/Reset Operation

Upon initial power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device clears all internal registers. TCLK is the transmit reference, and MCLK is the bias reference. The PLLs are continuously calibrated.

The transceiver can be reset from the Host or Hardware mode. In Host mode, reset is commanded by writing 1s to TST and ALOOP, and a 0 to TAOS (bits D5, D6 and D7, respectively, of the SIO input data byte). In either mode, command reset by holding TRSTE High for approximately 200 ns. All output signals are tri-stated at this time. The falling edge of the TRSTE initiates reset. Both modes reset each port independently. Reset clears and sets all SIO registers to 0 at the affected port. Reset is not generally required for the port to be operational.
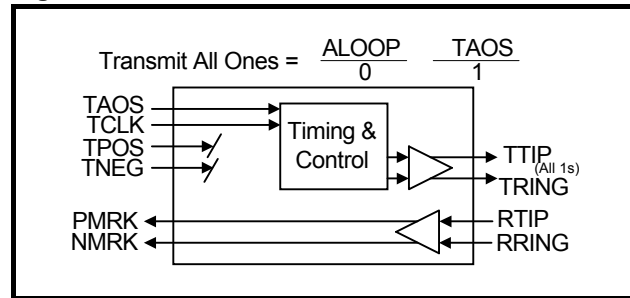
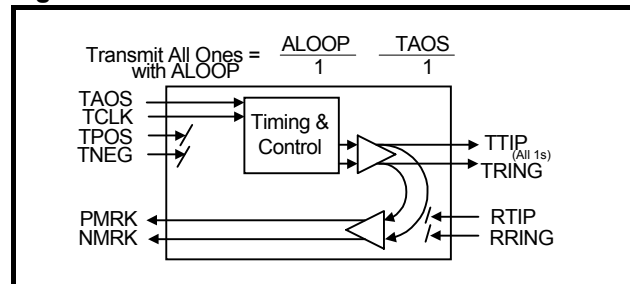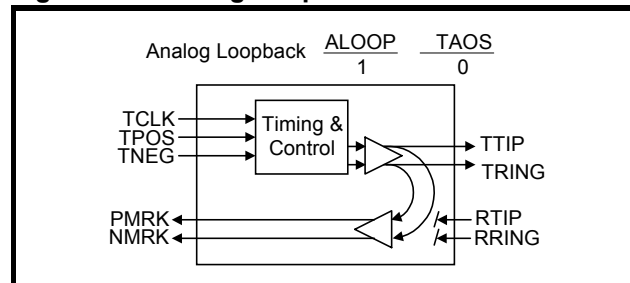**Figure 7:   TAOS Data Path**

Figure 8:   TAOS with ALOOP

Figure 9:   Analog Loopback

APPLICATION INFORMATION

Power Requirements

The LXT331 is a low-power CMOS device. It operates from a single +5 V power supply which can be tied to all three VCC inputs. However, all inputs must be within ± .3 V of each other, and decoupled to their respective grounds separately. Isolation between the transmit and receive circuits is provided internally. During normal operation or analog loopback, the transmitter powers down if TCLK is not supplied.

Line Interface Requirements

Table 8 lists transformer values for 1.544 Mbps and 2.048 Mbps applications. Table 9 shows combinations of transformers, series resistors and the LEN*xn* settings that produce a variety of return loss values.

Table 8: Recommended Transformer Values

Parameter	Value
Turns Ratio (T1)	1:2.3 (Tx) / 1: 1 (Rx)
Turns Ratio (E1)	1:2 (Tx) / 1: 1 (Rx)
Primary Inductance	1.2 mH minimum
Leakage Inductance	0.5 μH maximum
Interwinding Capacitance	25 pF maximum
DC Resistance (Primary)	1 Ω maximum
ET (Breakdown Voltage)	1 kV minimum

1.544 Mbps T1 Applications

Figure 11 on page 100 shows a typical host mode application. The eight serial interface pins are grouped at the top. Host mode is selected by the clock input to SPE. Other mode selection pins are shown at the bottom. With the TRSTE pin pulled Low, the LXT331 operates normally. Pulling this pin High causes all outputs to go to a high impedance state.

Figure 11 on page 100 shows a pair of framers. An LXP600A Clock Adapter (CLAD) converts the 2.048 MHz backplane clock to provide the 1.544 MHz input to the MCLK and TCLK inputs of both LIU ports.

The DFM indicator shown in the diagram lower left is available to drive optional external circuits. The driver power supply inputs (bottom) are tied to a common bus with 68 μF decoupling capacitors installed. The power sup-

ply for the remaining (non-driver) circuitry is shown at center right with 1.0 μF and 0.1 μF decoupling capacitors.

The line interface circuitry is identical for both LIU ports. The precision resistors in line with the transmit transformer provide optimal return loss. The recommended transformer/resistor combination is listed at the bottom of Figure 10. 1:1 transformers are used on the receive side.

Table 9: Transformer Combinations

LEN	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
For T1/DSX-1 100 Ω Twisted-Pair Applications:			
011-111	1:2	Rt = 9.1 Ω	14dB
011-111	1:2.3	Rt = 9.1 Ω	18dB
011-011	1:1.15	Rt = 0 Ω	1dB
For E1 120 Ω Twisted-Pair Applications:			
001	1:2	Rt = 15 Ω	18dB
000	1:2	Rt = 9.1 Ω	10dB
For E1 75 Ω Coaxial Applications:			
001	1:2	Rt = 14.3 Ω	10dB
000	1:2	Rt = 9.1 Ω	18dB

2. Transformer turns ratio accuracy is ± 2%.
3. Rt values are ± 1%.
4. Typical return loss, 51kHz - 3.072 MHz band, with a capacitor in parallel with the primary side of the transformer.

2.048 Mbps E1 Applications

E1 Coaxial Applications

Figure 11 on page 100 shows the line interface for a typical 2.048 Mbps E1/CEPT coaxial (75 Ω) application. The LEN code should be set to 000 for coax. With 9.1 Ω Rt resistors in line with the 1:2 output transformers, the LXT331 produces 2.37 V peak pulses as required for coax applications. As in the T1 application shown in Figure 10, 1:1 transformers are used on the receive side.

Figure 10: Line Interface for E1 Coax

Typical value, adjust for board parasitics to obtain optimum return loss
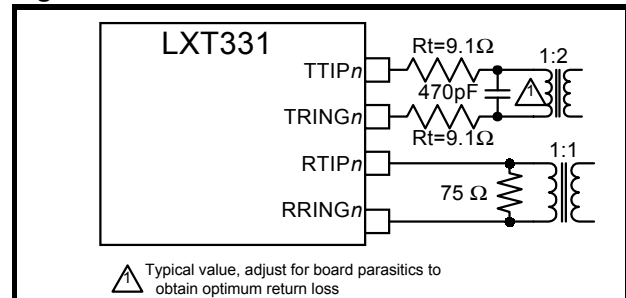
Figure 11: Typical LXT331 T1 Application (Host Control Mode, Bipolar I/O))

Media: 100 Ω Twisted Pair

LEN	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
011-111	1:2.3	Rt = 9.1 Ω	18 dB

NOTES:

1. Transformer turns ratio accuracy is ± 2%.

2. Rt values are ± 1%.

3. Typical return loss, 51 kHz - 3.072 MHz band.
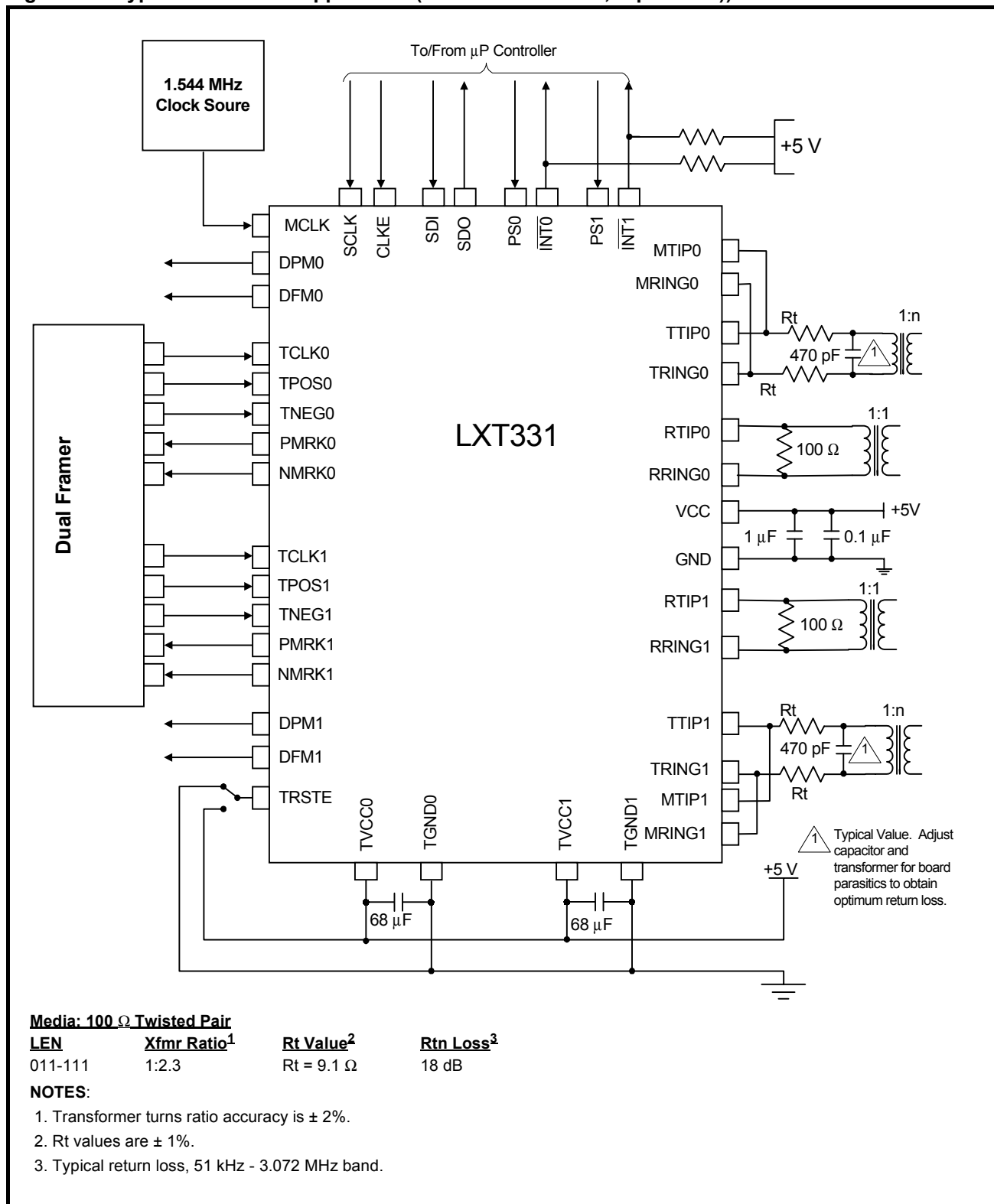
E1 Twisted-Pair Applications

Figure 12 shows a typical 2.048 Mbps E1 twisted-pair (120 Ω) application. The line length equalizers are controlled by the hardwired LEN inputs. With the LEN code set to 001 and 15 Ω Rt resistors in line with the 1:2 output transformers, the LXT331 produces the 3.0 V peak pulses required for this application.

Figure 12: Typical LXT331 E1 120 Ω Twisted Pair Application (Hardware Control Mode))

Media	LEN	Xfmr Ratio[1]	Rt[2]	Rr	Rtn Loss[3]
120 TWP	001	1:2	15 Ω	240 Ω	18 dB
75 Coax	000	1:2	9.1Ω	150 Ω	18 dB

NOTES:

1. Transformer turns ratio accuracy is ± 2%.
2. Rt values are ± 1%.
3. Typical return loss, 51 kHz - 3.072 MHz band.
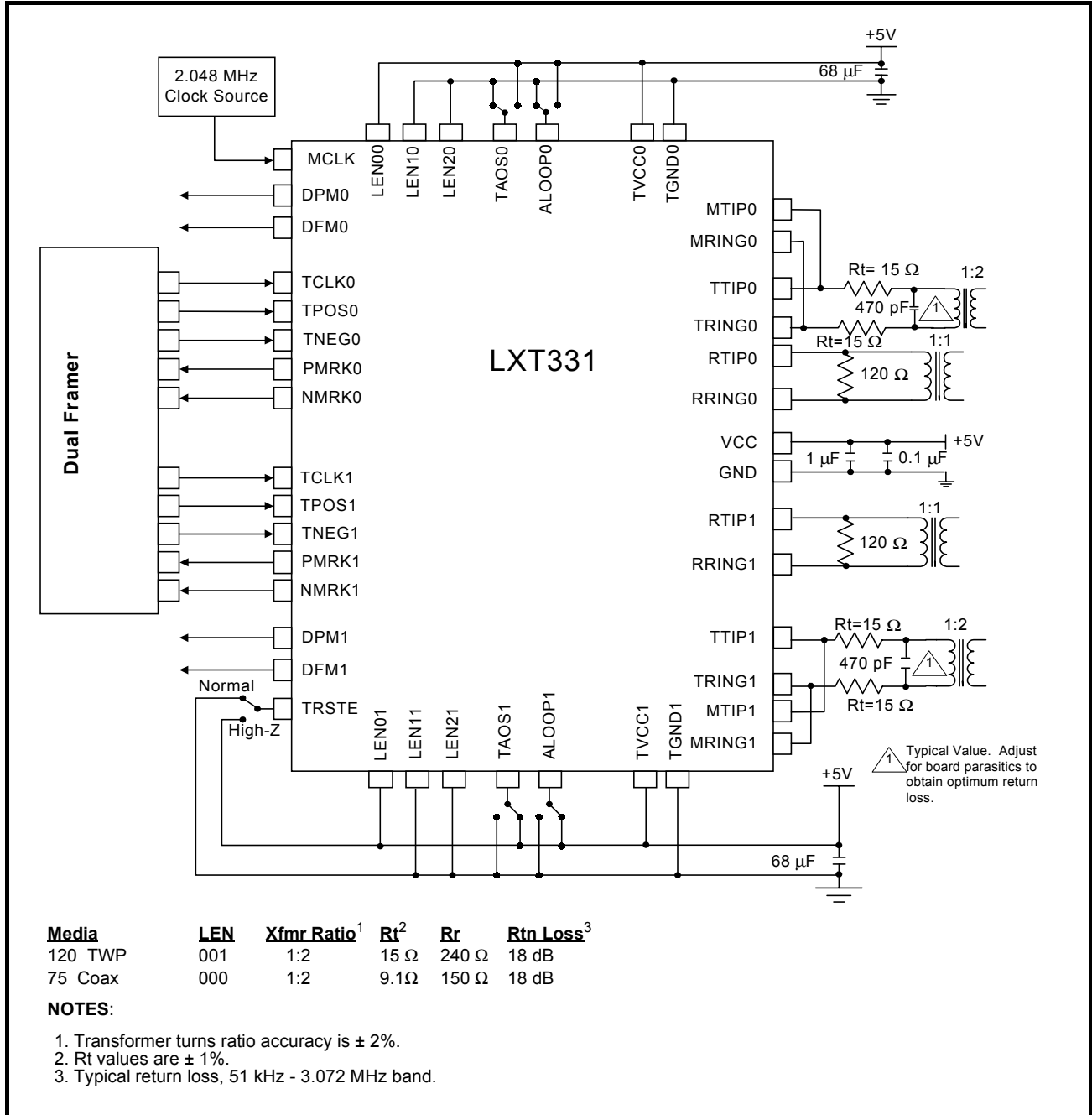
TEST SPECIFICATIONS

Table 10: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	VCC, TVCC0, TVCC1	-0.3	6.0	V
Input voltage, any pin [1]	V_{IN}	GND - 0.3	Vcc + 0.3	V
Input current, any pin [2]	I_{IN}	-10	10	mA
Storage temperature	T_{ST}	-65	150	°C
CAUTION Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed or implied at these extremes.				

1. Excluding RTIP and RRING which must stay within - 6 V to VCC + 0.3 V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP0 & 1, TRING0 & 1, VCC, TVCC0 & 1 and TGND0 & 1 can withstand continuous current of 100 mA.

Table 11: Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
DC supply [2]	VCC, TVCC0, TVCC1	4.75	5.0	5.25	V
Ambient operating temperature [3]	T_A	-40	25	85	°C
Ambient operating temperature [4]	T_A	-5	25	85	°C

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Variation between TVCC0, TVCC1 and VCC must be - 0.3 V.
3. LXT331PE & QE
4. LXT331PH & QH

Table 12: Electrical Characteristics (Over Recommended Operating Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Total power dissipation - T1 [2] (Maximum line length, 75 Ω load)	P_P	-	-	680	mW	-40 to +85 °C
	P_D	-	-	650	mW	0 to +85 °C
Total power dissipation - T1 [3] (Maximum line length, 43 Ω load)	P_P	-	-	1000	mW	-40 to +85 °C
	P_D	-	-	980	mW	0 to +85 °C
Total power dissipation - E1 [2]	P_D	-	-	520	mW	100% ones density
High level input voltage [4,5]	V_{IH}	2.0	-	-	V	
Low level input voltage [4,5]	V_{IL}	-	-	0.8	V	
High level output voltage [4,5]	V_{OH}	2.4	-	-	V	$I_{OUT} = -400 \, \mu A$
Low level output voltage [4,5]	V_{OL}	-	-	0.4	V	$I_{OUT} = 1.6 \, mA$
Input leakage current [6]	I_{LLD}	0	-	± 10	μA	
Input leakage current [7]	I_{LLM}	0	-	± 50	μA	
Three-state leakage current [4]	I_{SL}	-	-	± 10	μA	
TTIP/TRING leakage current	I_{TR}	-	-	1.2	mA	in power down and tri-state

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. 100% 1s density and maximum line length. Driving 75 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
3. 100% 1s density and maximum line length. Driving 43 Ω load (corresponding to an Rt value of 9.1 Ω and a 1:2 transformer ratio) over operating range. include device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
4. Functionality of pins depends on mode.
5. Output drivers will output CMOS logic levels into CMOS loads.
6. All digital input pins.
7. For MTIP0, MRING0, MTIP1 AND MRING1.

Table 13: Analog Specifications (Over Recommended Operating Range)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
AMI output pulse amplitudes	DSX-1	2.4	3.0	3.6	V	measured at the DSX
	E1 (120 Ω)	2.7	3.0	3.3	V	measured at line side
	E1 (75 Ω)	2.13	2.37	2.61	V	measured at line side
Transmit amplitude variation with supply [3]		-	1	2.5	%	
Recommended output load at TTIP and TRING		-	75	-	Ω	
Driver output impedance [3]		-	3	10	Ω	@ 772 kHz
Jitter added by the transmitter [2]	10 Hz - 8kHz [3]	-	0.005	0.01	UI	T1 Jitter Bands
	8 kHz - 40 kHz [3]	-	0.015	0.025	UI	
	10 Hz - 40 Hz [3]	-	0.02	0.025	UI	
	Broad band	-	0.03	0.05	UI	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal at TCLK is jitter-free.
3. Not production tested, but guaranteed by design and other correlation methods.

Table 13: Analog Specifications (Over Recommended Operating Range) – continued

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Jitter added by the transmitter [2]	20 Hz - 100 kHz	-	-	0.05	UI	E1 Jitter Band
Output power levels [3] DSI 2 kHz BW	@ 772 kHz	12.6	-	17.9	dBm	
	@ 1544 kHz	-29	-	-	dB	
Positive-to-negative pulse imbalance		-	-	0.5	dB	
Differential		-	40	-	kΩ	
Sensitivity below DSX (0 dB = 2.4 V) (max 6 dB cable attenuation)		13.6	-	-	dB	
		500	-	-	mV	
Peak detector sqelch level		-	226	-	mV	
Data decision threshold	DSX-1	63	70	77	% peak	
	E1	43	50	57	% peak	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal at TCLK is jitter-free.
3. Not production tested, but guaranteed by design and other correlation methods.

Table 14: LXT331 Master Clock and Transmit Timing Characteristics (See Figure 13)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	-	1.544	-	MHz
	E1	MCLK	-	2.048	-	MHz
Master clock tolerance		MCLKt	-	± 50	-	ppm
Master clock duty cycle		MCLKd	40	-	60	%
Transmit clock frequency	DSX-1	TCLK	-	1.544	-	MHz
	E1	TCLK	-	2.048	-	MHz
Transmit clock tolerance		TCLKt	-	± 50	-	ppm
Transmit clock duty cycle		TCLKd	10	-	90	%
TPOS/TNEG to TCLK setup time		tSUT	25	-	-	ns
TCLK to TPOS/TNEG Hold time		tHT	25	-	-	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

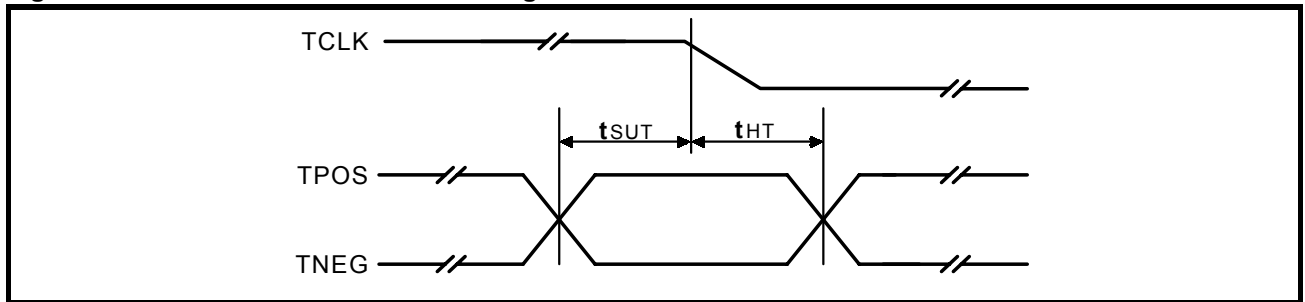**Figure 13: LXT331 Transmit Clock Timing**

Table 15: LXT331 Receive Characteristics (See Figure 14)

| Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
PMRK/NMRK pulse width	T1	tMPW	-	324	-	ns	
	E1	tMPW	-	244	-	ns	
Receiver throughput delay		tRXD	-	65	-	ns	3.0 V pulse
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.							

Table 16: LXT331 Serial I/O Timing Characteristics (See Figures 15 and 16)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	tRF	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	tDC	50	-	-	ns	
SCLK to SDI hold time	tCDH	50	-	-	ns	
SCLK low time	tCL	240	-	-	ns	
SCLK high time	tCH	240	-	-	ns	
SCLK rise and fall time	tR, tF	-	-	50	ns	
PS to SCLK setup time	tPC	50	-	-	ns	
SCLK to PS hold time	tCPH	50	-	-	ns	
PS inactive time	tPWH	250	-	-	ns	
SCLK to SDO valid	tCDV	-	-	200	ns	
16th SCLK falling edge or PS rising edge to SDO high Z	tCDZ	-	100	-	ns	
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 14: LXT331 Receive Timing
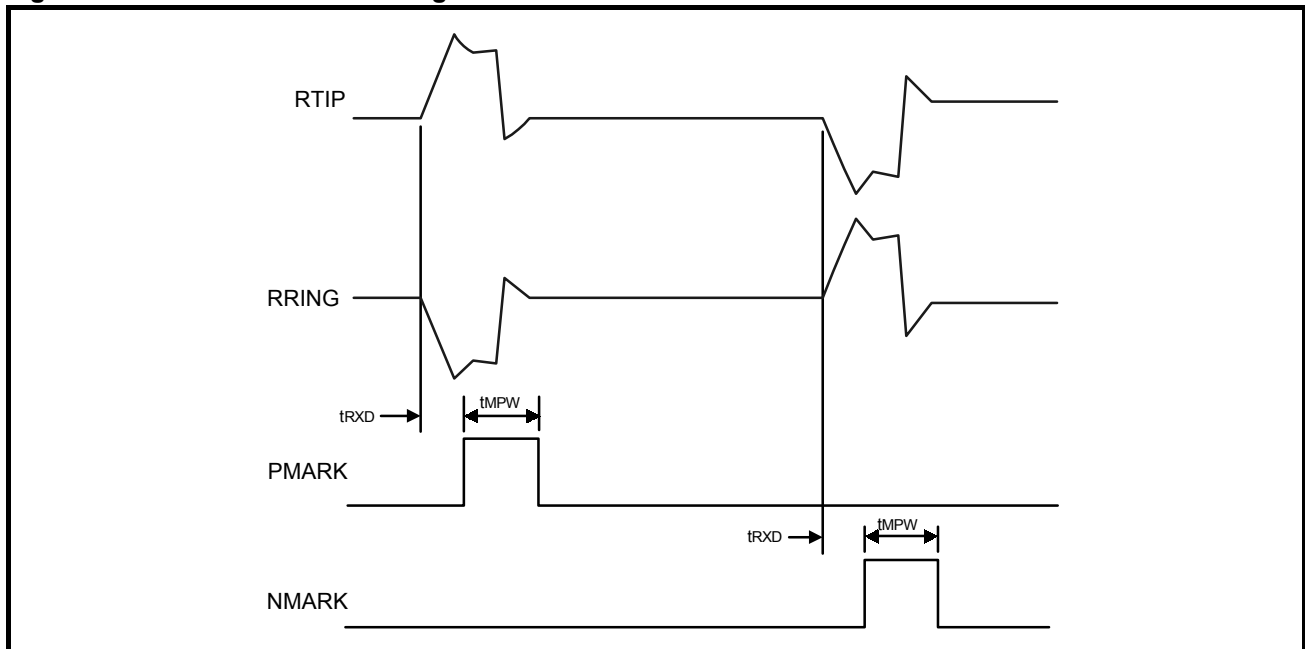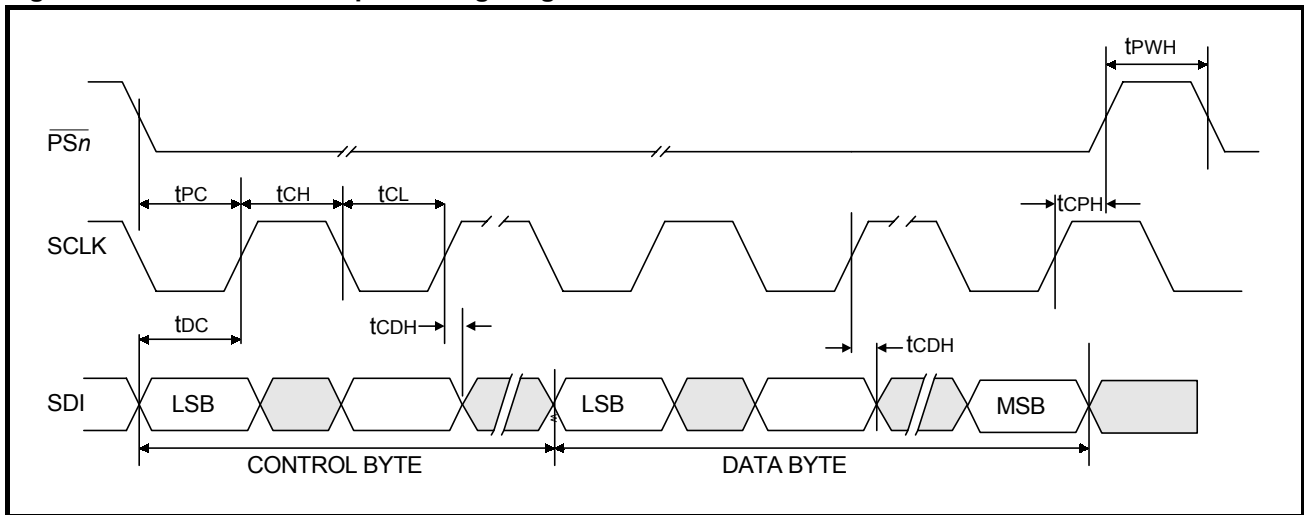
Figure 15: LXT331 Serial Input Timing Diagram

Figure 16: LXT331 Serial Output Timing Diagram