

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4521B

### MSI

## 24-stage frequency divider and oscillator

Product specification  
File under Integrated Circuits, IC04

January 1995

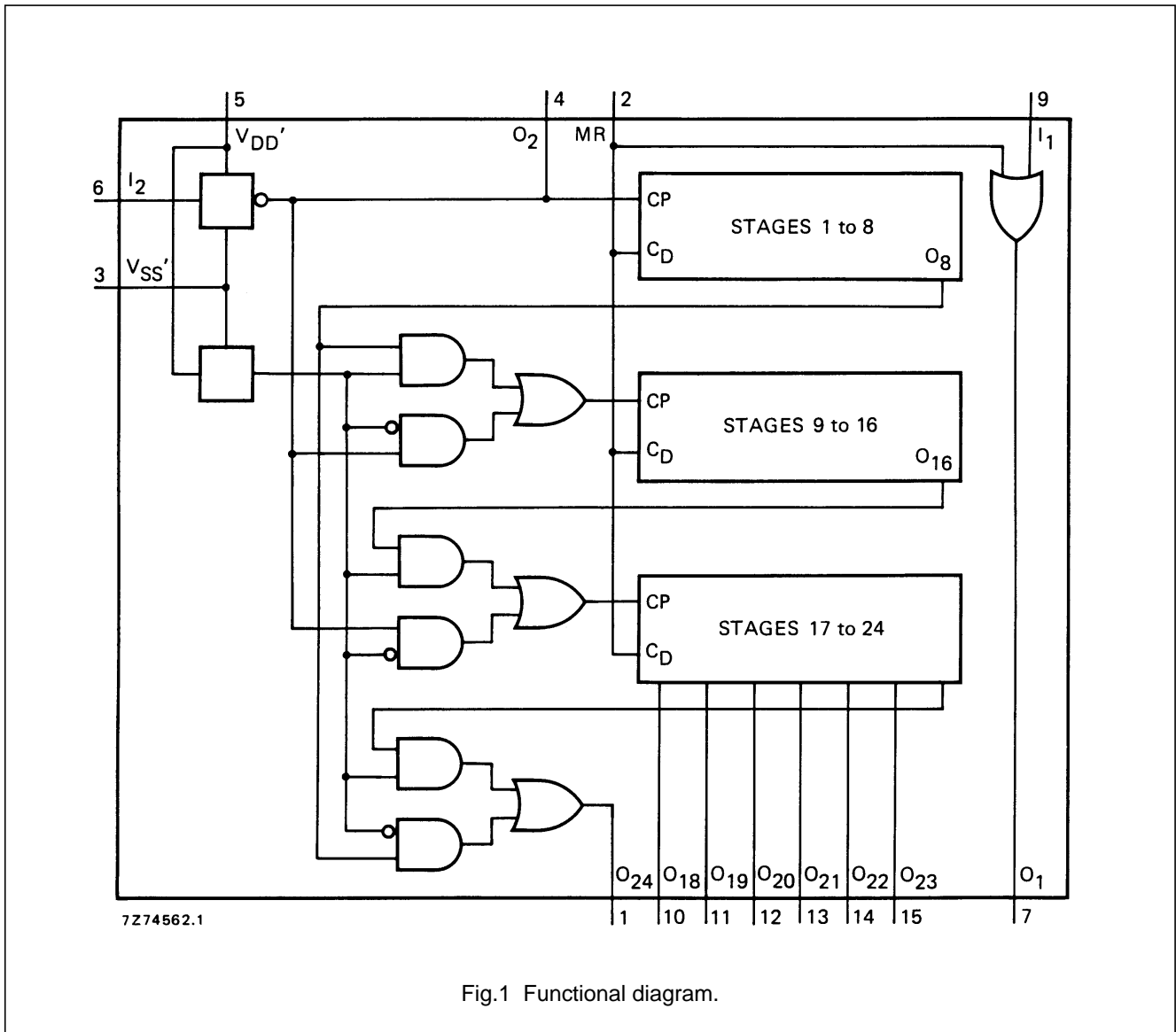
# 24-stage frequency divider and oscillator

## HEF4521B MSI

### DESCRIPTION

The HEF4521B consists of a chain of 24 toggle flip-flops with an overriding asynchronous master reset input (MR), and an input circuit that allows three modes of operation. The single inverting stage ( $I_2/O_2$ ) will function as a crystal oscillator, or in combination with  $I_1$  as an RC oscillator, or as an input buffer for an external oscillator. Low-power

operation as a crystal oscillator is enabled by connecting external resistors to pins 3 ( $V_{SS}'$ ) and 5 ( $V_{DD}'$ ). Each flip-flop divides the frequency of the previous flip-flop by two, consequently the HEF4521B will count up to  $2^{24} = 16777216$ . The counting advances on the HIGH to LOW transition of the clock ( $I_2$ ). The outputs of the last seven stages are available for additional flexibility.

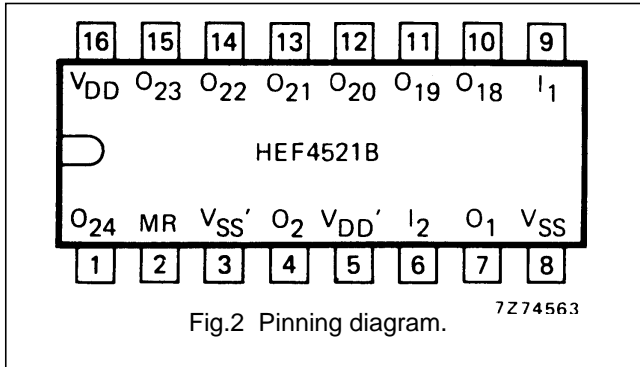


### FAMILY DATA, $I_{DD}$ LIMITS category MSI

See Family Specifications

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COUNT CAPACITY

OUTPUT	COUNT CAPACITY
O <sub>18</sub>	2 <sup>18</sup> = 262 144
O <sub>19</sub>	2 <sup>19</sup> = 524 288
O <sub>20</sub>	2 <sup>20</sup> = 1 048 576
O <sub>21</sub>	2 <sup>21</sup> = 2 097 152
O <sub>22</sub>	2 <sup>22</sup> = 4 194 304
O <sub>23</sub>	2 <sup>23</sup> = 8 388 608
O <sub>24</sub>	2 <sup>24</sup> = 16 777 216

- HEF4521BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4521BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4521BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

FUNCTIONAL TEST SEQUENCE

INPUTS		CONTROL TERMINALS			OUTPUTS	REMARKS
MR	I <sub>2</sub>	O <sub>2</sub>	V <sub>SS</sub> '	V <sub>DD</sub> '	O <sub>18</sub> to O <sub>24</sub>	
H	L	L	V <sub>DD</sub>	V <sub>SS</sub>	L	counter is in three 8-stage sections in parallel mode; I <sub>2</sub> and O <sub>2</sub> are interconnected (O <sub>2</sub> is now input); counter is reset by MR
L			V <sub>DD</sub>	V <sub>SS</sub>	H	255 pulses are clocked into I <sub>2</sub> , O <sub>2</sub> (the counter advances on the LOW to HIGH transition)
L	L	L	V <sub>SS</sub>	V <sub>SS</sub>	H	V <sub>SS</sub> ' is connected to V <sub>SS</sub>
L	H	L	V <sub>SS</sub>	V <sub>SS</sub>	H	the input I <sub>2</sub> is made HIGH
L	H	L	V <sub>SS</sub>	V <sub>DD</sub>	H	V <sub>DD</sub> ' is connected to V <sub>DD</sub> ; O <sub>2</sub> is now made floating and becomes an output; the device is now in the 2 <sup>24</sup> mode
L			V <sub>SS</sub>	V <sub>DD</sub>	L	counter ripples from an all HIGH state to an all LOW state

A test function has been included for the reduction of the test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections by connecting V<sub>SS</sub>' to V<sub>DD</sub> and V<sub>DD</sub>' to V<sub>SS</sub>. Via I<sub>2</sub> (connected to O<sub>2</sub>) 255 counts are loaded into each of the 8-stage sections in parallel. All flip-flops are now at a HIGH state.

The counter is now returned to the normal 24-stage in series configuration by connecting V<sub>SS</sub>' to V<sub>SS</sub> and V<sub>DD</sub>' to V<sub>DD</sub>. One more pulse is entered into input I<sub>2</sub>, which will cause the counter to ripple from an all HIGH state to an all LOW state.

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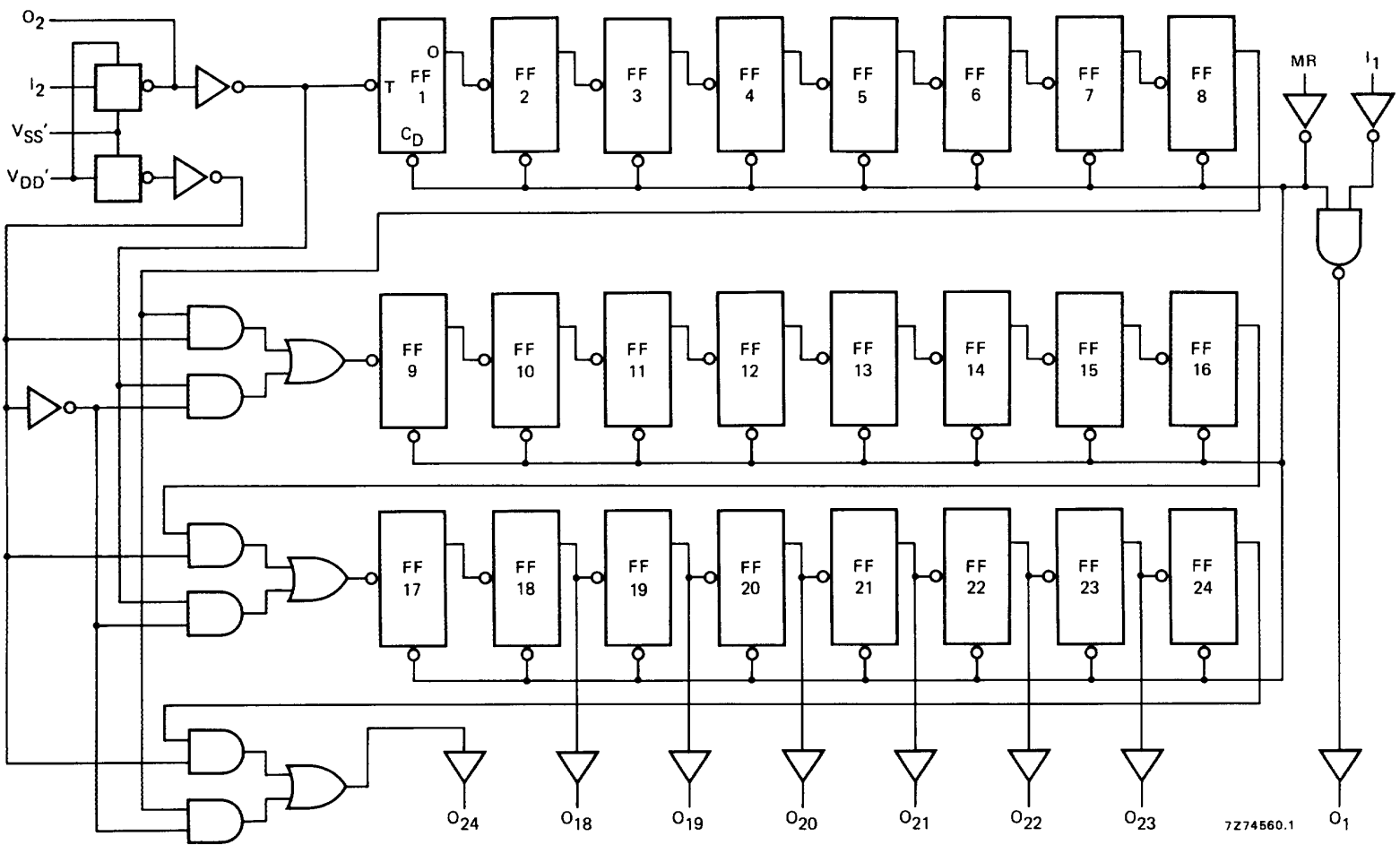


Fig.3 Logic diagram; for schematic diagram of clock circuit see Fig.4.

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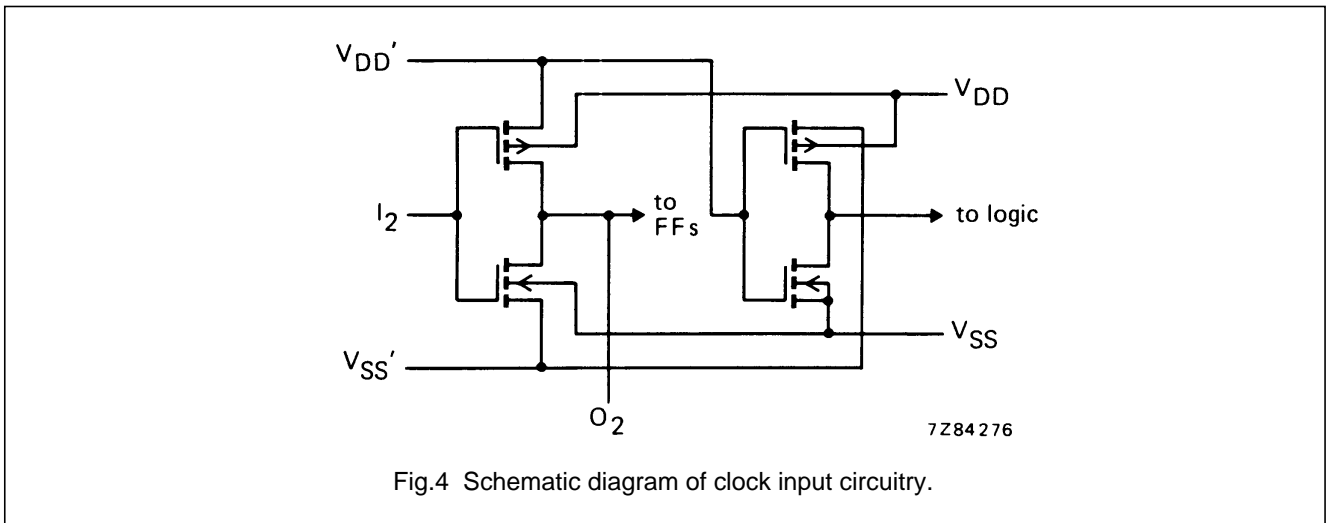


Fig.4 Schematic diagram of clock input circuitry.

**AC CHARACTERISTICS**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $I_2 \rightarrow O_{18}$ HIGH to LOW	5	$t_{PHL}$		950	1900	ns	923 ns + (0,55 ns/pF) $C_L$
	10			350	700	ns	339 ns + (0,23 ns/pF) $C_L$
	15			220	440	ns	212 ns + (0,16 ns/pF) $C_L$
LOW to HIGH	5	$t_{PLH}$		950	1900	ns	923 ns + (0,55 ns/pF) $C_L$
	10			350	700	ns	339 ns + (0,23 ns/pF) $C_L$
	15			220	440	ns	212 ns + (0,16 ns/pF) $C_L$
$O_n \rightarrow O_{n+1}$ HIGH to LOW	5	$t_{PHL}$		40	80	ns	13 ns + (0,55 ns/pF) $C_L$
	10			15	30	ns	4 ns + (0,23 ns/pF) $C_L$
	15			10	20	ns	2 ns + (0,16 ns/pF) $C_L$
LOW to HIGH	5	$t_{PLH}$		40	80	ns	13 ns + (0,55 ns/pF) $C_L$
	10			15	30	ns	4 ns + (0,23 ns/pF) $C_L$
	15			10	20	ns	2 ns + (0,16 ns/pF) $C_L$
$MR \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$		120	240	ns	93 ns + (0,55 ns/pF) $C_L$
	10			55	110	ns	44 ns + (0,23 ns/pF) $C_L$
	15			40	80	ns	32 ns + (0,16 ns/pF) $C_L$
$I_1 \rightarrow O_1$ HIGH to LOW	5	$t_{PHL}$		90	180	ns	63 ns + (0,55 ns/pF) $C_L$
	10			35	70	ns	24 ns + (0,23 ns/pF) $C_L$
	15			25	50	ns	17 ns + (0,16 ns/pF) $C_L$
LOW to HIGH	5	$t_{PLH}$		60	120	ns	33 ns + (0,55 ns/pF) $C_L$
	10			30	60	ns	19 ns + (0,23 ns/pF) $C_L$
	15			20	40	ns	12 ns + (0,16 ns/pF) $C_L$

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	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Output transition times HIGH to LOW	5	t <sub>THL</sub>		60	120	ns	10 ns + (1,0 ns/pF) C <sub>L</sub>
	10		30	60	ns	9 ns + (0,42 ns/pF) C <sub>L</sub>	
	15		20	40	ns	6 ns + (0,28 ns/pF) C <sub>L</sub>	
LOW to HIGH	5	t <sub>TLH</sub>		60	120	ns	10 ns + (1,0 ns/pF) C <sub>L</sub>
	10		30	60	ns	9 ns + (0,42 ns/pF) C <sub>L</sub>	
	15		20	40	ns	6 ns + (0,28 ns/pF) C <sub>L</sub>	

AC CHARACTERISTICS

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = 25 °C; C<sub>L</sub> = 50 pF; input transition times ≤ 20 ns

	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.	
Minimum I <sub>2</sub> pulse width; HIGH	5	t <sub>WI2H</sub>	80	40		ns
	10		40	20		ns
	15		30	15		ns
Minimum MR pulse width; HIGH	5	t <sub>WMRH</sub>	70	35		ns
	10		40	20		ns
	15		30	15		ns
Recovery time for MR	5	t <sub>RMR</sub>	20	-10		ns
	10		15	-5		ns
	15		15	0		ns
Maximum clock pulse frequency	5	f <sub>max</sub>	6	12		MHz
	10		12	25		MHz
	15		17	35		MHz

see also waveforms  
Fig.5

	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	1 200 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	where f <sub>i</sub> = input freq. (MHz) f <sub>o</sub> = output freq. (MHz) C <sub>L</sub> = load capacitance (pF) ∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs V <sub>DD</sub> = supply voltage (V)
	10	5 100 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	
	15	13 050 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	

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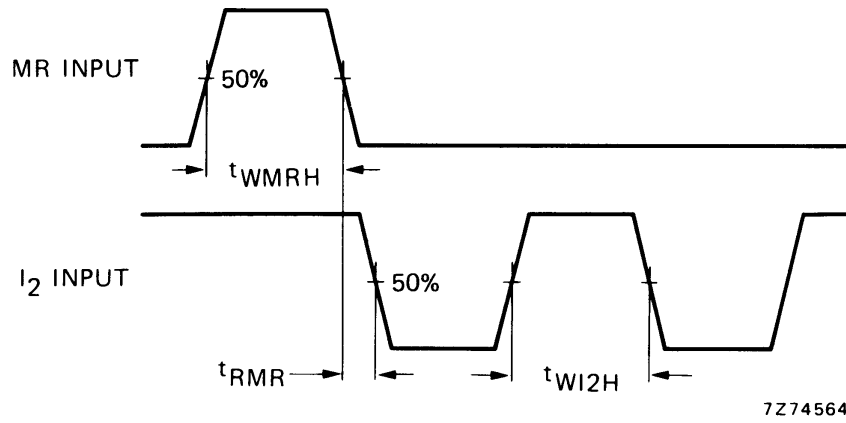
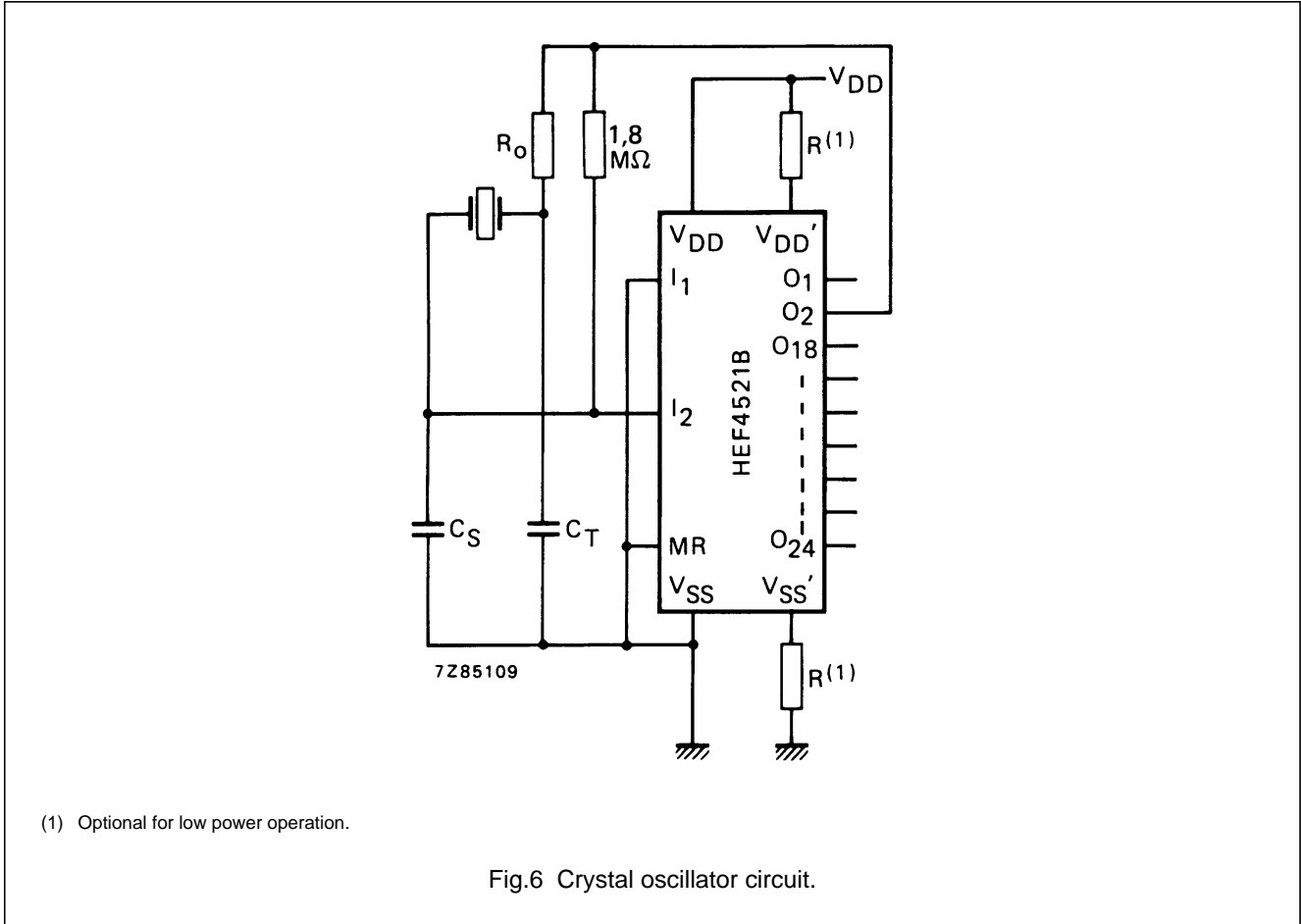


Fig.5 Waveforms showing minimum pulse widths for MR and I<sub>2</sub>, recovery time for MR.

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APPLICATION INFORMATION



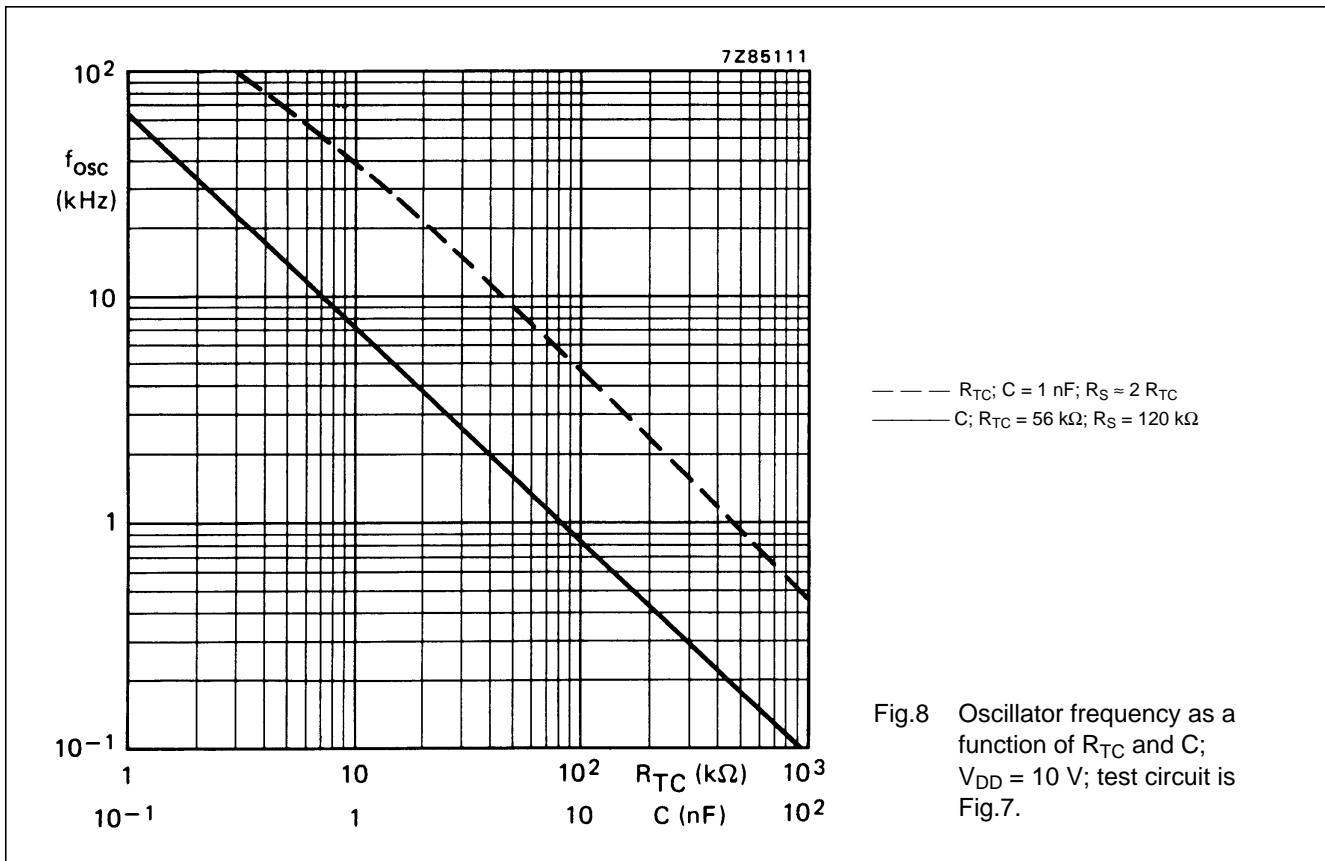
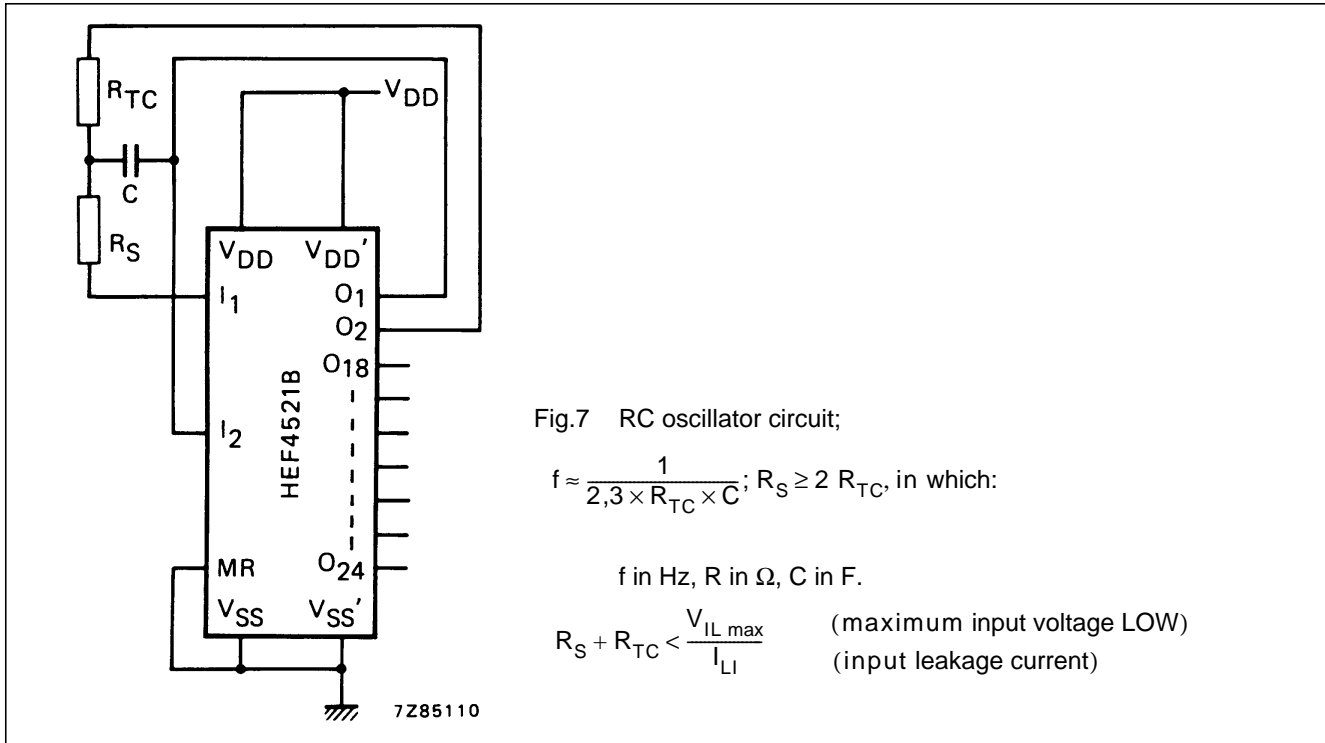
Typical characteristics for crystal oscillator circuit (Fig.6):

	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal characteristics			
resonance frequency	500	50	kHz
crystal cut	S	N	-
equivalent resistance; $R_S$	1	6,2	k $\Omega$
External resistor/capacitor values			
$R_o$	47	750	k $\Omega$
$C_T$	82	82	pF
$C_S$	20	20	pF



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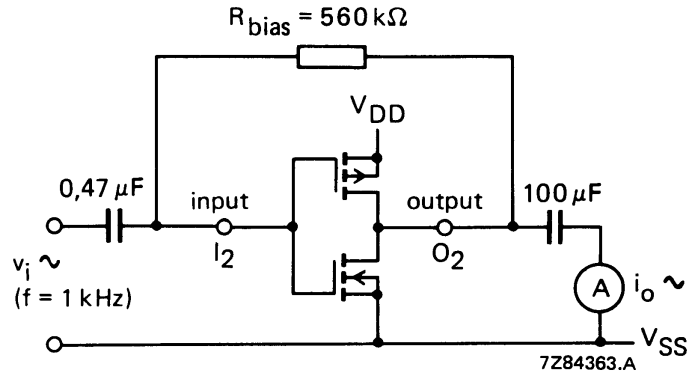
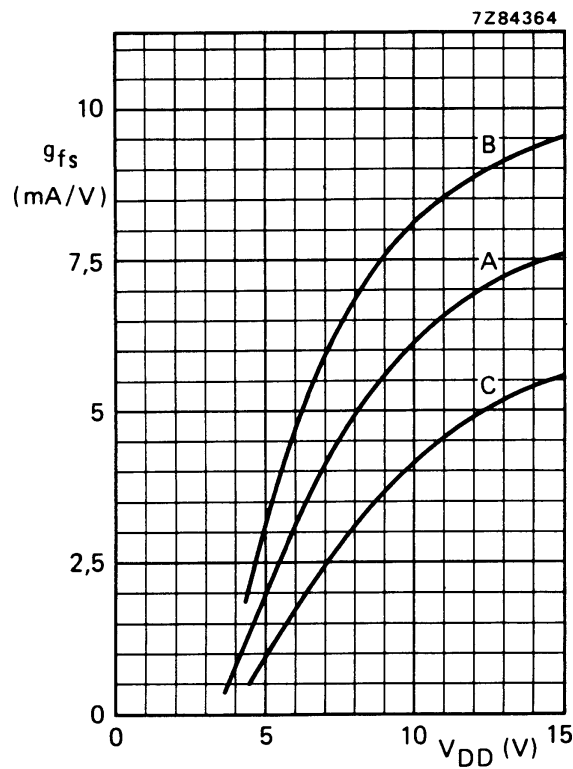


Fig.9 Test set-up for measuring forward transconductance  $g_{fs} = di_o/dv_i$  at  $v_o$  is constant (see also graph Fig.10).



A: average,  
 B: average + 2 s,  
 C: average - 2 s, in which: 's' is the observed standard deviation.

Fig.10 Typical forward transconductance  $g_{fs}$  as a function of the supply voltage at  $T_{amb} = 25^\circ\text{C}$ .

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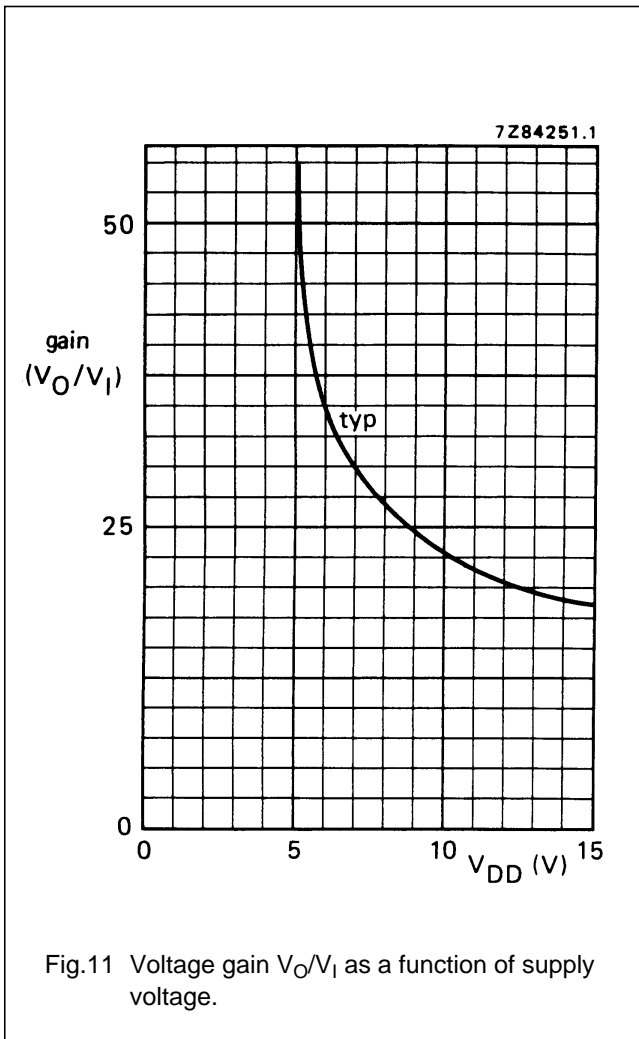


Fig.11 Voltage gain  $V_O/V_I$  as a function of supply voltage.

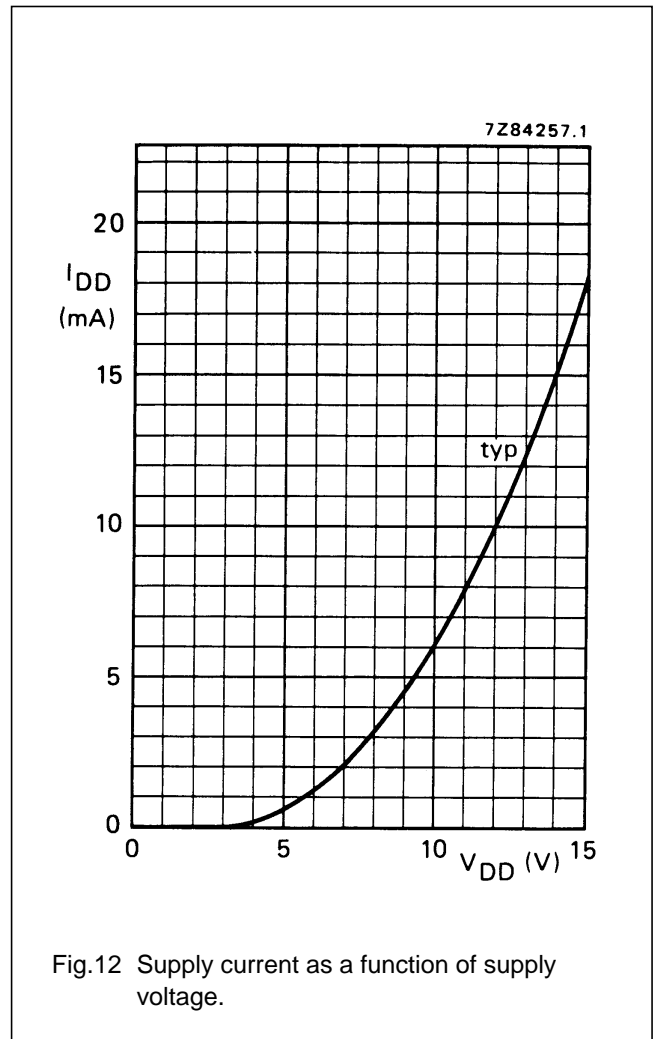


Fig.12 Supply current as a function of supply voltage.

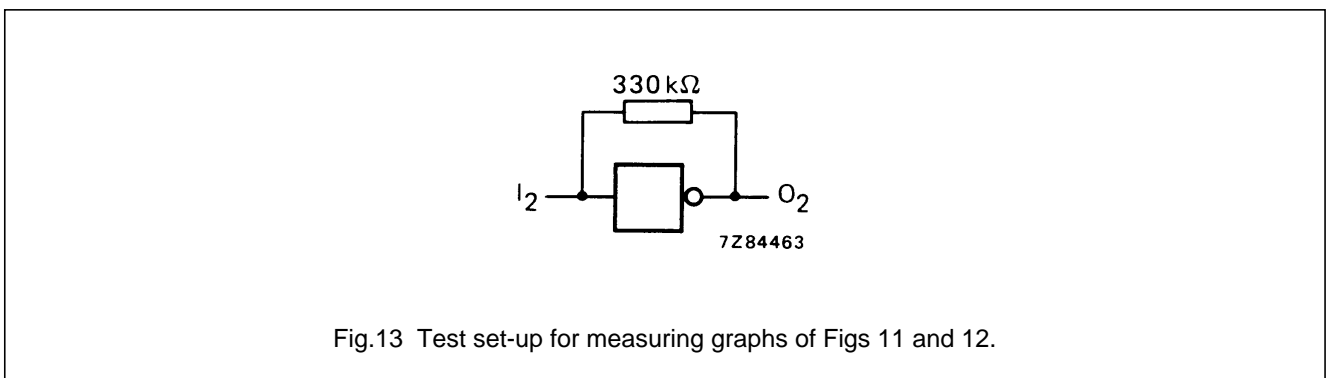


Fig.13 Test set-up for measuring graphs of Figs 11 and 12.