Ordering number: EN 5591

Monolithic Linear IC

LA6541D

4-channel Bridge Driver for Compact Discs

Functions and Features

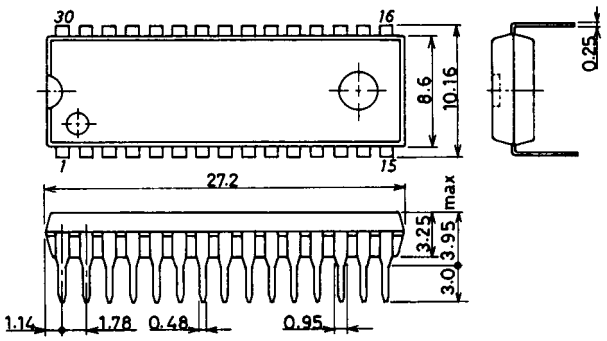
- 4-channel bridge (BTL) power amplifier.
- I_O max. 700 mA.
- With mute circuit
  (Affects all amplifier outputs, Amp 1 to Amp 8).
  (When the mute voltage is low, the outputs turn off; when the mute voltage is high, the outputs turn on).
- 5.0 V regulator built in (Uses external PNP transistor).
- Reset circuit built in (The reset output delay time can be adjusted through an external capacitor).

Package Dimensions

unit : mm

3196-DIP30SLF

[LA6541D]



SANYO : DIP30SLF

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		14	V
Maximum input voltage	V_{IN}		13	V
Mute pin voltage	V_{Mute}		13	V
Allowable power dissipation	Pd max	When using standard board (material: glass epoxy)	2.5	W
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +150	°C

Recommended Operating Conditions at Ta = 25°C

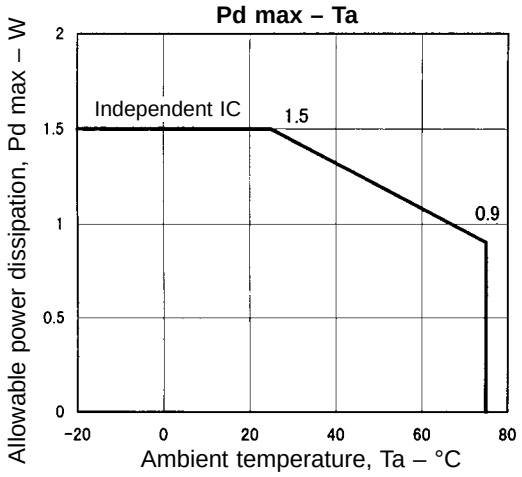
Parameter	Symbol	Conditions	Ratings	Unit
Operating voltage	V_{CC}		5.6 to 13	V
Reset output source current	I_{ORH}		0 to 200	µA
Reset output sink current	I_{ORL}		0 to 2	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 8.0 V, V_{REF} = 4 V

Parameter	Symbol	Conditions	min	typ	max	Unit
No-load current drain	$I_{CC}1$	When all amplifier outputs are on (Mute high)		20	40	mA
	$I_{CC}2$	When all amplifier outputs are off (Mute low)		15	35	mA
Output offset voltage	$V_{OF}1$	Amplifier 1 to 2 (V_O1 to V_O2), Amplifier 3 to 4 (V_O3 to V_O4)	–50		50	mV
	$V_{OF}2$	Amplifier 5 to 6 (V_O5 to V_O6), Amplifier 7 to 8 (V_O7 to V_O8)	–50		50	mV
Buffer amplifier input voltage range	V_{BIN}		1.5		V_{CC}–1.5	V
Input voltage range	V_{IN}		1.0		V_{CC}–1.5	V
Output source voltage	V_O1	Note 1, when R_L = 8.0 Ω	5.0	5.6		V
Output sink voltage	V_O2	Note 2, when R_L = 8.0 Ω		1.8	2.4	V
Closed-circuit voltage gain	VG	Between bridge amplifiers		9		dB
Slew rate	SR			0.15		V/µs
Mute on voltage	V_{Mute}	Note 3		1.2		V
[Power Supply] (with 2SK632K connected externally)						
Output voltage	$V_{OUT}1$	I_O = 200 mA	4.75	5.0	5.25	V
Line regulation	$\Delta V_{OLN}1$	5.6 ≦ $V_{IN}1$ ≦ 12 V		20	100	mV
Load regulation	$\Delta V_{OLD}1$	5 mA ≦ I_O ≦ 200 mA		50	150	mV
[Reset]						
High reset output voltage	V_{ORH}	I_{ORH} = 200 µA, Cd pin open	4.73	4.98	5.23	V
Low reset output voltage	V_{ORL}	I_{SRL} = 2 mA, Cd is shorted to GND		100	200	mV
Reset threshold voltage	V_{RT}	Note 4		4.3		V
Reset hysteresis voltage	Vhys	Note 5	40	100	200	mV
Reset output delay time	td	Cd = 0.1 µF		10		ms

Notes:

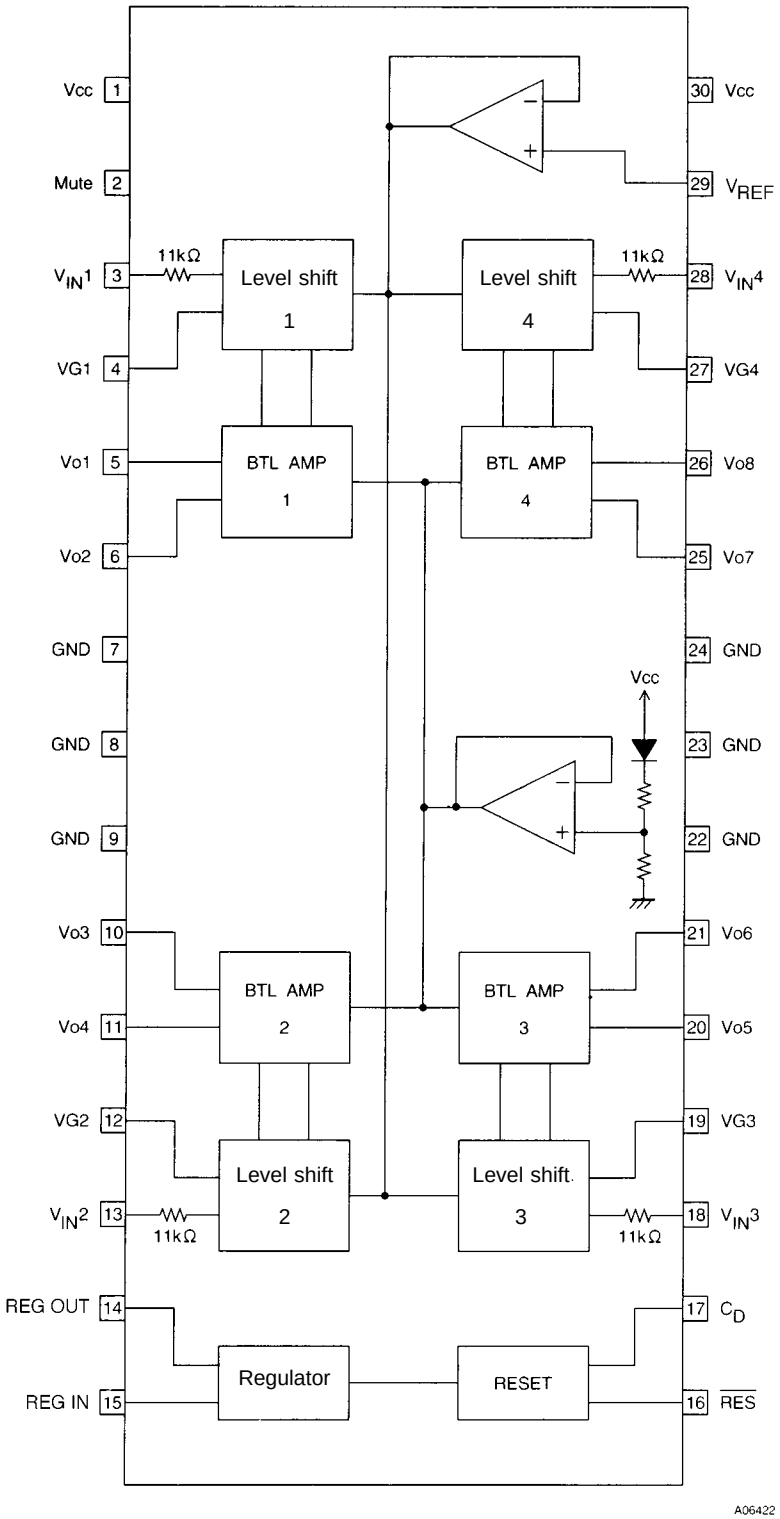
1. Source voltage to ground when an 8 Ω load is connected between bridge amplifier outputs.
2. Sink voltage to ground when an 8 Ω load is connected between bridge amplifier outputs.
3. When the mute signal is high, all amplifier outputs turn on, and when low, all amplifier outputs turn off. When the mute signal is low, amplifier output is undefined.
4. 5 V supply voltage when the reset output goes low.
5. Potential difference from the 5 V supply voltage when the reset output goes low and when it goes high.



Pin Functions

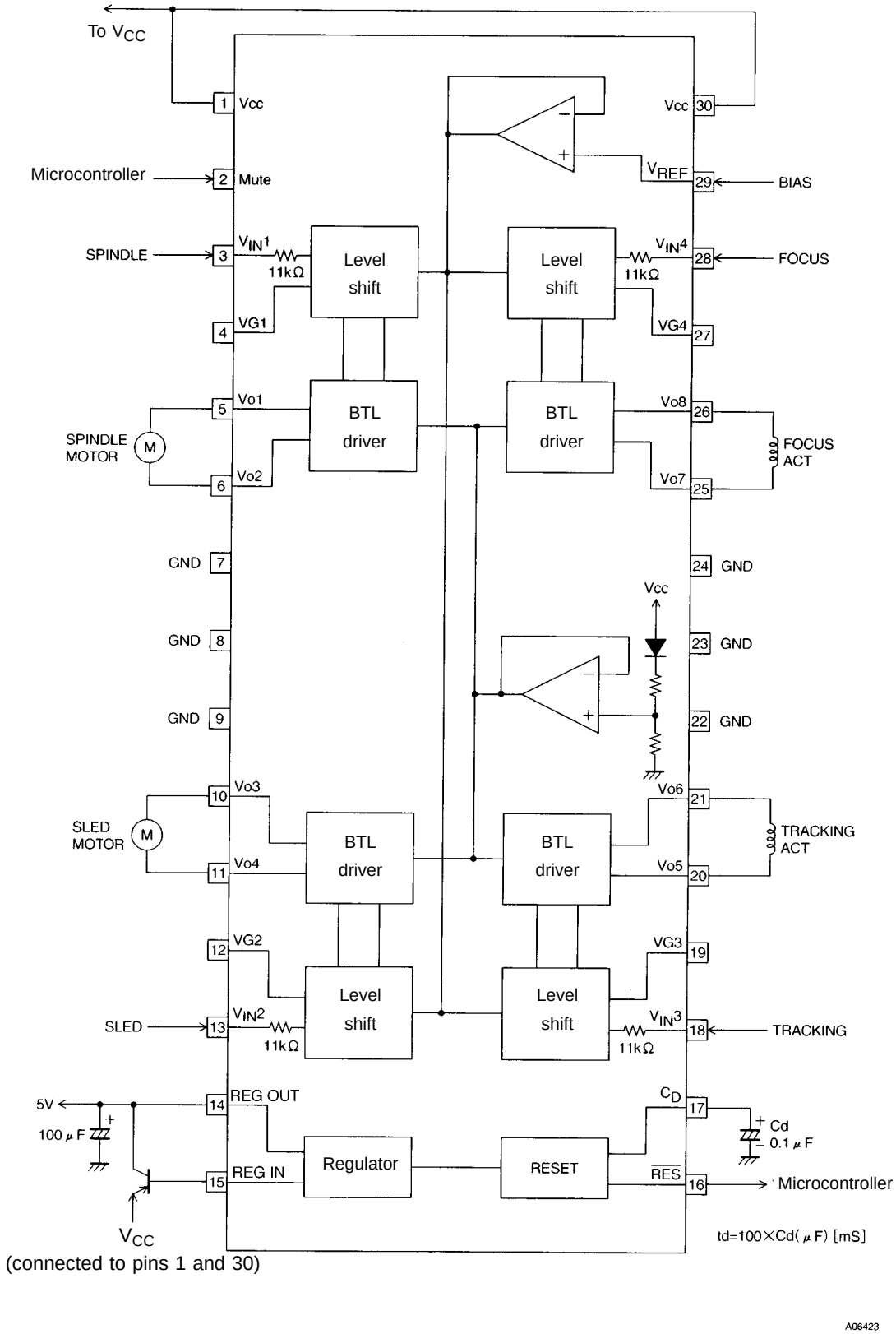
Pin No.	Pin Name	Description (Function)
1	V_{CC}	Power supply (shorted with pin 30)
2	Mute	ON/OFF control for all BTL AMP outputs
3	$V_{IN}1$	BTL AMP 1 input
4	VG1	BTL AMP 1 input (for gain control)
5	V_O1	BTL AMP 1 output (non-inverting side)
6	V_O2	BTL AMP 1 output (inverting side)
7	GND	GND (minimum electric potential)
8	GND	GND (minimum electric potential)
9	GND	GND (minimum electric potential)
10	V_O3	BTL AMP 2 output (inverting side)
11	V_O4	BTL AMP 2 output (non-inverting side)
12	VG2	BTL AMP 2 input (for gain control)
13	$V_{IN}2$	BTL AMP 2 input
14	REG OUT	Connection for collector of external transistor (PNP); 5 V supply output
15	REG IN	Connection for base of external transistor (PNP)
16	$\overline{RES}$	Reset output
17	C_D	Reset output delay time setting (with capacitor)
18	$V_{IN}3$	BTL AMP 3 input
19	VG3	BTL AMP 3 input (for gain control)
20	V_O5	BTL AMP 3 output (non-inverting side)
21	V_O6	BTL AMP 3 output (inverting side)
22	GND	GND (minimum electric potential)
23	GND	GND (minimum electric potential)
24	GND	GND (minimum electric potential)
25	V_O7	BTL AMP 4 output (inverting side)
26	V_O8	BTL AMP 4 output (non-inverting side)
27	VG4	BTL AMP 4 input (for gain control)
28	$V_{IN}4$	BTL AMP 4 input
29	V_{REF}	Reference voltage input for level shift circuit
30	V_{CC}	Power supply (shorted with pin 1)

Pin Assignment (Block Diagram)



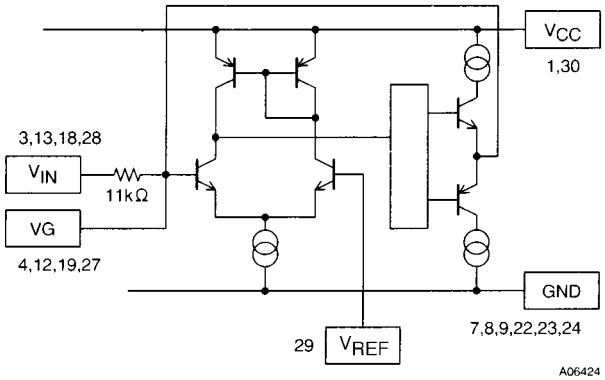
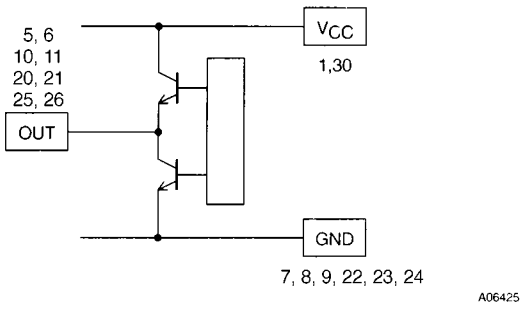
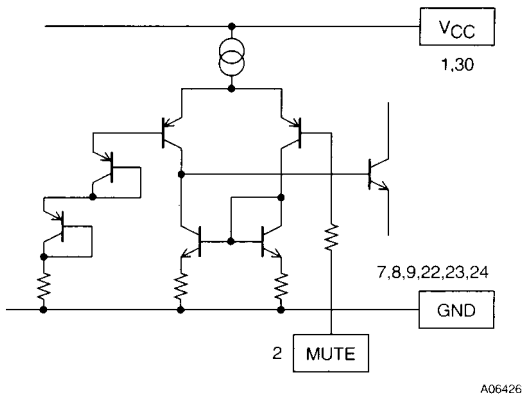
Top view

Sample Application Circuit



Note: Use a delay capacitor (Cd) whose capacitance does not change much according to the temperature.

Pin Functions

Pin	Name	Pin No.	Equivalent Circuit	Description
Input	$V_{IN}1$ $V_{IN}2$ $V_{IN}3$ $V_{IN}4$ VG1 VG2 VG3 VG4	3 13 18 28 4 12 19 27		Input pins
Output	V_O1, V_O2 V_O3, V_O4 V_O5, V_O6 V_O7, V_O8	5, 6 10, 11 20, 21 25, 26		Output pins
Mute	Mute	2		Output ON/OFF

Truth Table

Input	MUTE	CH1		CH2		CH3		CH4	
		V_O1 (Amp1)	V_O2 (Amp2)	V_O3 (Amp3)	V_O4 (Amp4)	V_O5 (Amp5)	V_O6 (Amp6)	V_O7 (Amp7)	V_O8 (Amp8)
H	H	H	L	L	H	H	L	L	H
	L	—	—	—	—	—	—	—	—
L	H	L	H	H	L	L	H	H	L
	L	—	—	—	—	—	—	—	—

* The "—" symbol means "undefined."

Reset Operation