TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74HCT273AP, TC74HCT273AF, TC74HCT273AFW

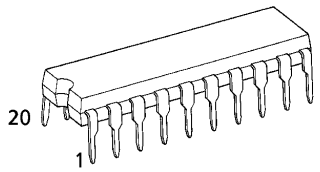
## OCTAL D-TYPE FLIP FLOP WITH CLEAR

(Note) The JEDEC SOP (FW) is not available in Japan.

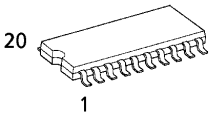
The TC74HCT273A is a high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate $C^2MOS$ technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.
When the $\overline{CLR}$ input is held "L", the Q outputs are at a low logic level independent of the other inputs.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

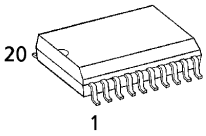
- High Speed ····· $f_{MAX}$ = 90MHz (typ.) at $V_{CC}$ = 5V
- Low Power Dissipation ····· $I_{CC}$ = 4$\mu$A (Max.) at Ta = 25°C
- Compatible with TTL outputs ··· $V_{IH}$ = 2.0V (Min.), $V_{IL}$ = 0.8V (Max.)
- Wide interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74LS273




P (DIP20-P-300-2.54A)
Weight : 1.30g (Typ.)

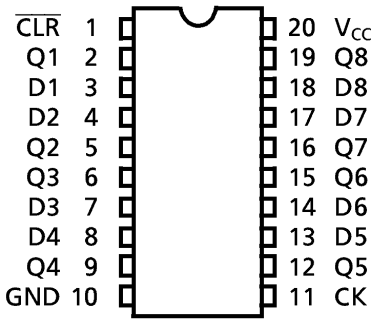



F (SOP20-P-300-1.27)
Weight : 0.22g (Typ.)




FW (SOL20-P-300-1.27)
Weight : 0.46g (Typ.)

## PIN ASSIGNMENT



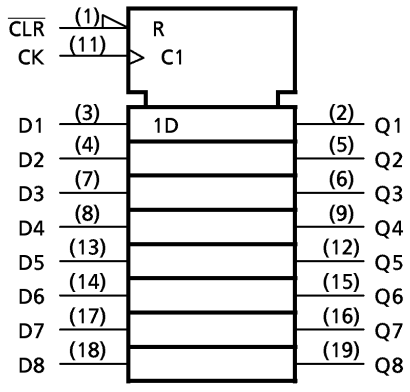

(TOP VIEW)

## TRUTH TABLE

| INPUTS | | | OUTPUTS | FUNCTION |
|---|---|---|---|---|
| $\overline{CLR}$ | D | CK | Q | |
| L | X | X | L | CLEAR |
| H | L | ↑ | L | — |
| H | H | ↑ | H | — |
| H | X | ↓ | $Q_n$ | No change |

X : Don't Care

## IEC LOGIC SYMBOL




980508EBA2

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | −0.5~7 | V |
| DC Input Voltage | $V_{IN}$ | −0.5~$V_{CC}$+0.5 | V |
| DC Output Voltage | $V_{OUT}$ | −0.5~$V_{CC}$+0.5 | V |
| Input Diode Current | $I_{IK}$ | ±20 | mA |
| Output Diode Current | $I_{OK}$ | ±20 | mA |
| DC Output Current | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$/Ground Current | $I_{CC}$ | ±50 | mA |
| Power Dissipation | $P_D$ | 500 (DIP)* / 180 (SOP) | mW |
| Storage Temperature | $T_{stg}$ | −65~150 | °C |

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5~5.5 | V |
| Input Voltage | $V_{IN}$ | 0~$V_{CC}$ | V |
| Output Voltage | $V_{OUT}$ | 0~$V_{CC}$ | V |
| Operating Temperature | $T_{opr}$ | −40~85 | °C |
| Input Rise and Fall Time | $t_r$, $t_f$ | 0~500 | ns |

## DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | | $V_{CC}$ (V) | Ta = 25°C | | | Ta = −40~85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN. | TYP. | MAX. | MIN. | MAX. | |
| High - Level Input Voltage | $V_{IH}$ | | | 4.5 ~ 5.5 | 2.0 | — | — | 2.0 | — | V |
| Low - Level Input Voltage | $V_{IL}$ | | | 4.5 ~ 5.5 | — | — | 0.8 | — | 0.8 | V |
| High - Level Output Voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −20 μA | 4.5 | 4.4 | 4.5 | — | 4.4 | — | V |
| | | | $I_{OH}$ = −4 mA | 4.5 | 4.18 | 4.31 | — | 4.13 | — | |
| Low - Level Output Voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 4.5 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | $I_{OL}$ = 4 mA | 4.5 | — | 0.17 | 0.26 | — | 0.33 | |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent Supply Current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 4.0 | — | 40.0 | μA |
| | $I_C$ | PER INPUT: $V_{IN}$ = 0.5V or 2.4V OTHER INPUT: $V_{CC}$ or GND | | 5.5 | — | — | 2.0 | — | 2.9 | mA |

**TIMING REQUIREMENTS ( Input $t_r = t_f = 6ns$ )**

| PARAMETER | SYMBOL | TEST CONDITION | $V_{CC}$ (V) | Ta = 25°C TYP. | Ta = 25°C LIMIT | Ta = −40~85°C LIMIT | UNIT |
|---|---|---|---|---|---|---|---|
| Minimum Pulse Width (CK) | $t_{W(L)}$<br>$t_{W(H)}$ | | 4.5<br>5.5 | —<br>— | 15<br>14 | 19<br>17 | ns |
| Minimum Pulse Width ($\overline{CLR}$) | $t_{W(L)}$ | | 4.5<br>5.5 | —<br>— | 15<br>14 | 19<br>17 | |
| Minimum Set−up Time | $t_s$ | | 4.5<br>5.5 | —<br>— | 10<br>10 | 13<br>13 | |
| Minimum Hold Time | $t_h$ | | 4.5<br>5.5 | —<br>— | 5<br>10 | 6<br>13 | |
| Minimum Removal Time ($\overline{CLR}$) | $t_{rem}$ | | 4.5<br>5.5 | —<br>— | 10<br>9 | 13<br>12 | |
| Clock Frequency | f | | 4.5<br>5.5 | —<br>— | 30<br>35 | 24<br>28 | MHz |

**AC ELECTRICAL CHARACTERISTICS ( $C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C, Input $t_r = t_f = 6ns$ )**

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Output Transition Time | $t_{TLH}$<br>$t_{THL}$ | | — | 4 | 8 | ns |
| Propagation Delay Time (CK−Q) | $t_{pLH}$<br>$t_{pHL}$ | | — | 15 | 25 | |
| Propagation Delay Time ($\overline{CLR}$−Q) | $t_{pHL}$<br>$t_{pHL}$ | | — | 18 | 28 | |
| Maximum Clock Frequency | $f_{MAX}$ | | 40 | 90 | — | MHz |

**AC ELECTRICAL CHARACTERISTICS ( $C_L = 50pF$, Input $t_r = t_f = 6ns$ )**

| PARAMETER | SYMBOL | TEST CONDITION | $V_{CC}$ (V) | Ta = 25°C MIN. | Ta = 25°C TYP. | Ta = 25°C MAX. | Ta = −40~85°C MIN. | Ta = −40~85°C MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Output Transition Time | $t_{TLH}$<br>$t_{THL}$ | | 4.5<br>5.5 | —<br>— | 9<br>8 | 15<br>14 | —<br>— | 19<br>18 | ns |
| Propagation Delay Time (CK−Q) | $t_{pLH}$<br>$t_{pHL}$ | | 4.5<br>5.5 | —<br>— | 19<br>17 | 30<br>27 | —<br>— | 38<br>34 | |
| Propagation Delay Time ($\overline{CLR}$−Q) | $t_{pLH}$<br>$t_{pHL}$ | | 4.5<br>5.5 | —<br>— | 22<br>18 | 32<br>29 | —<br>— | 40<br>36 | |
| Maximum Clock Frequency | $f_{MAX}$ | | 4.5<br>5.5 | 30<br>35 | 71<br>81 | —<br>— | 24<br>28 | —<br>— | MHz |
| Input Capacitance | $C_{IN}$ | | | — | 5 | 10 | — | 10 | pF |
| Power Dissipation Capacitance | $C_{PD}$ (1) | | | — | 29 | — | — | — | |

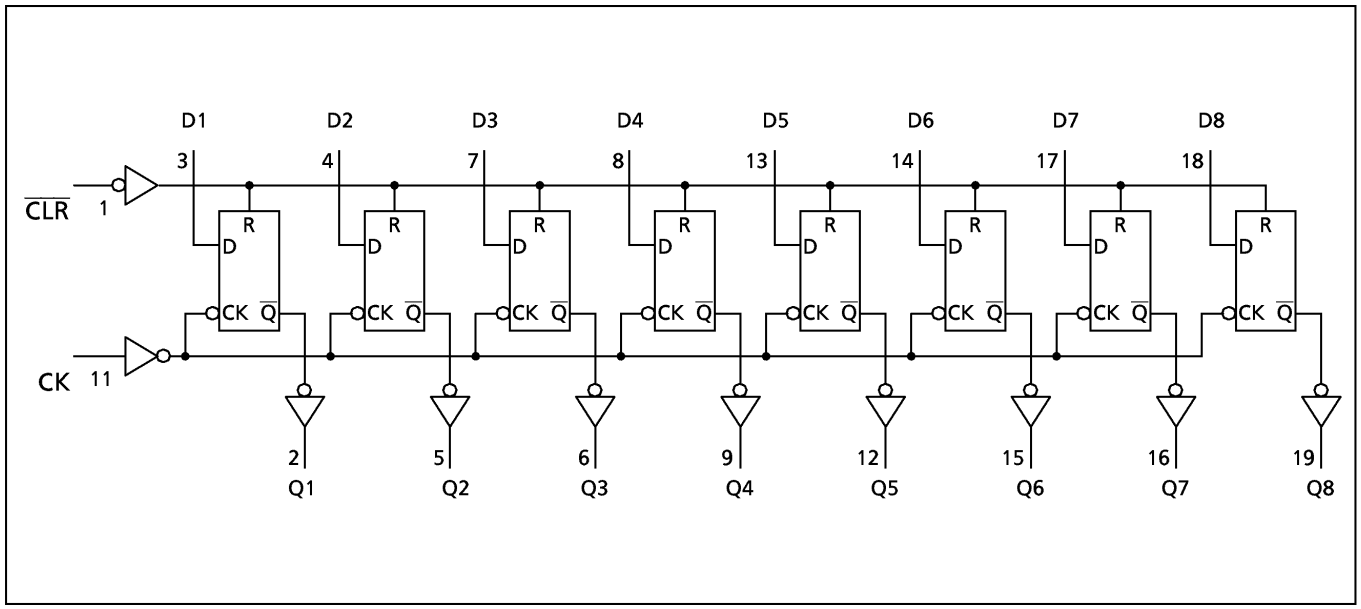
Note (1) $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ ( per Flip Flop )}$$

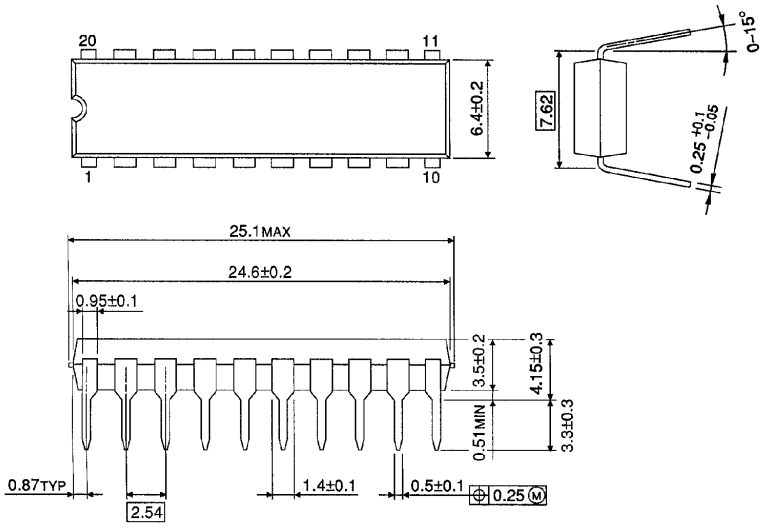
And the total $C_{PD}$ when n pcs. of Flip Flop operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 18 + 11 \cdot n$$

**SYSTEM DIAGRAM**

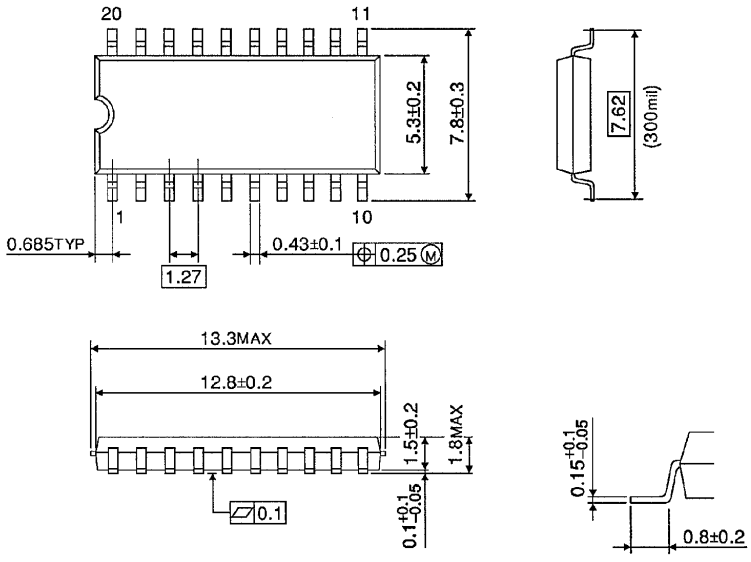


**DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)** Unit in mm




Weight : 1.30g (Typ.)

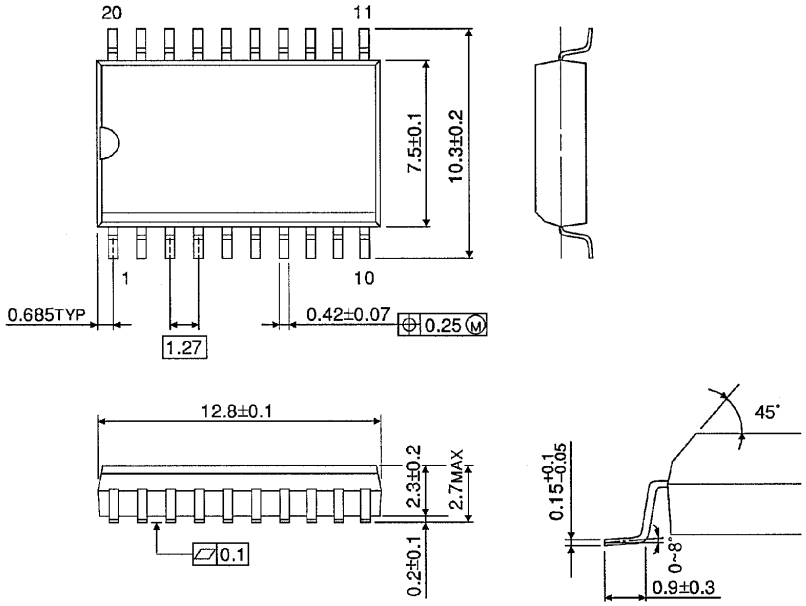
**SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)** Unit in mm




Weight : 0.22g (Typ.)

**SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27)** Unit in mm

(Note) This package is not available in Japan.




Weight : 0.46g (Typ.)