SONY

CXA3275Q

PLL/OSC/MIX IC for Digital Tuner

Description

The CXA3275Q is a monolithic tuner IC for single conversion system digital broadcast tuners. This IC integrates three sets of local oscillator and mixer circuits (VHF Low Band/ VHF High Band/UHF Band), an IF amplifier and a tuning PLL onto a single chip, enabling further miniaturization of the tuner.

Features

- Balanced oscillators with low-phase noise and excellent oscillation stability (UHF: 4 pins, VHF: 2 pins)
- High linearity mixer and IF amplifier
- IF output switchable between balanced and unbalanced
- Low-phase noise PLL synthesizer (3-wire bus format)
- Reference frequency programmable in 4 bits
- On-chip high voltage drive transistor for charge pump
- On-chip 4-output band switch (PNP transistor on/off)
- 40-pin QFP package

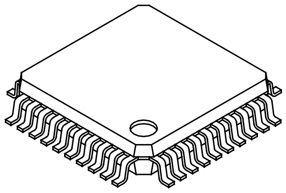
Applications

Digital CATV tuners

Structure

Bipolar silicon monolithic IC

40 pin QFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc, PLLVcc	–0.3 to +6.0	V
	IFVcc	–0.3 to +6.0	V
• Storage temperature			
	Tstg	–55 to +150	°C
• Allowable power dissipation			
	P_D	1.58	W

(when mounted on a printed circuit board)

Operating Conditions

• Supply voltage	Vcc, PLLVcc	4.5 to 5.5	V
	IFVcc	4.5 to 5.5	V
• Operating temperature			
	Topr	–40 to +80	°C

This IC has pins whose electrostatic discharge strength is weak as a high-frequency process is used for this IC.
Take care when handling the IC.

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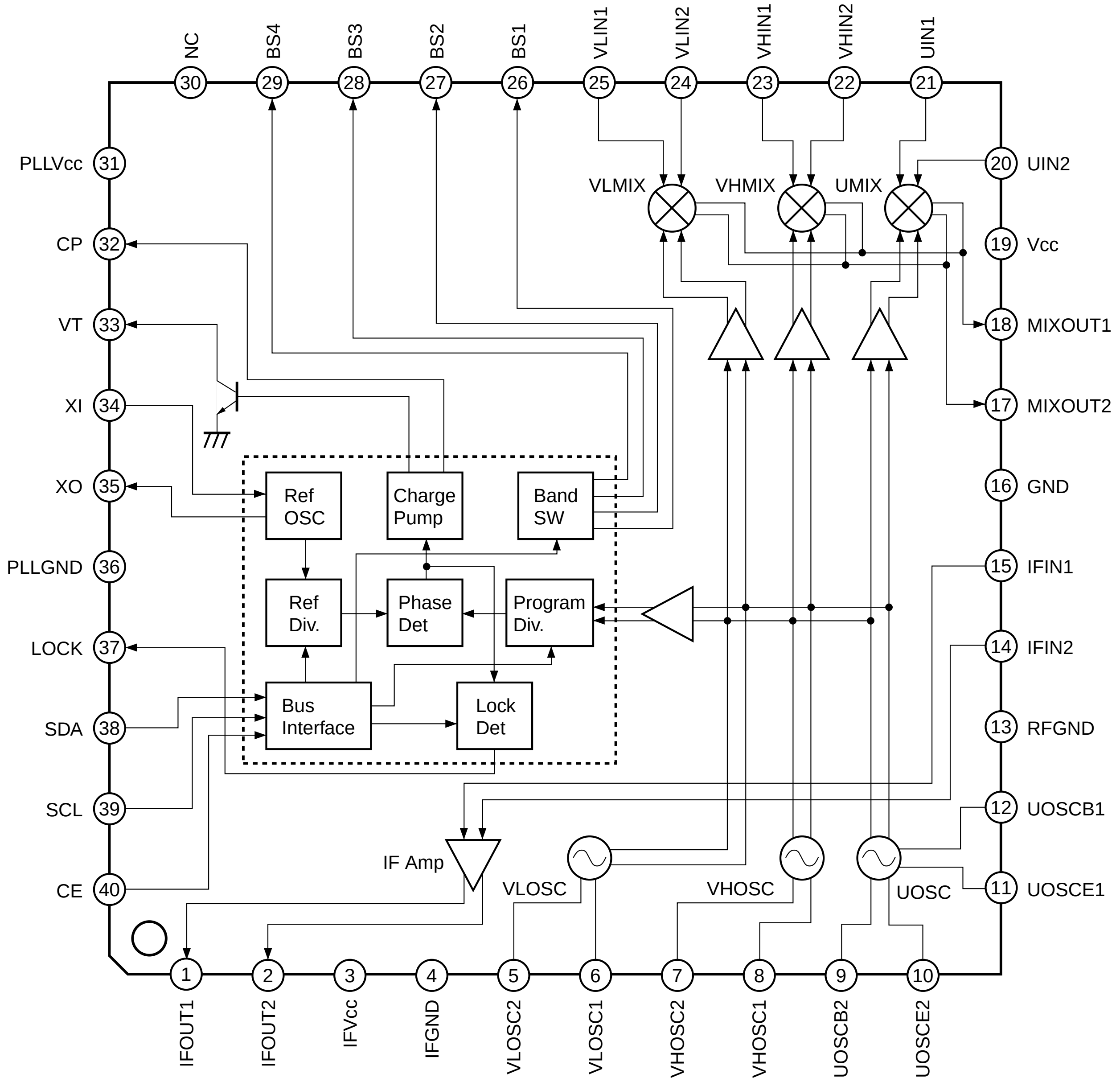
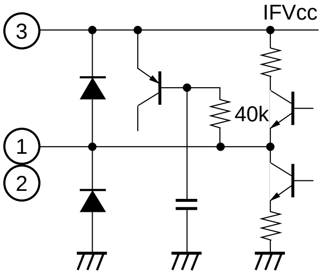
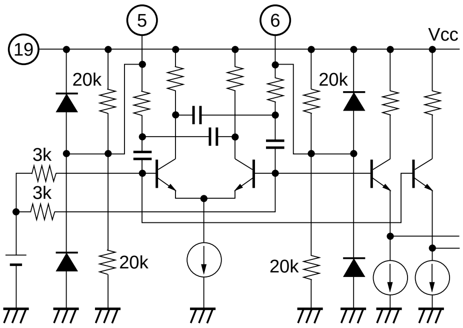
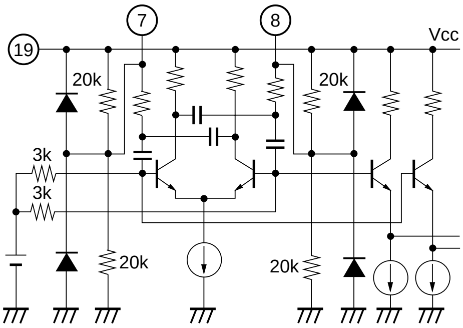
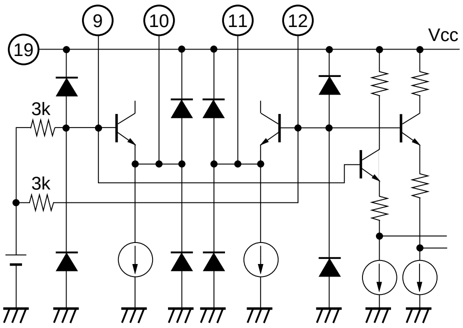
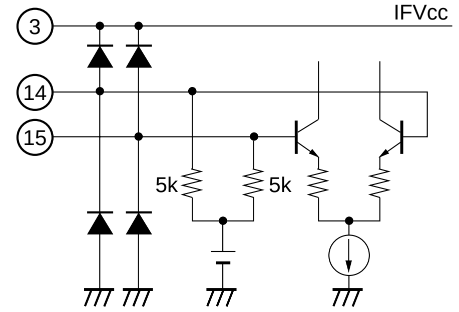
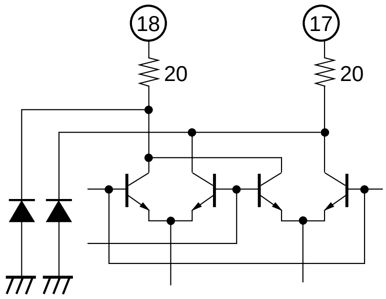
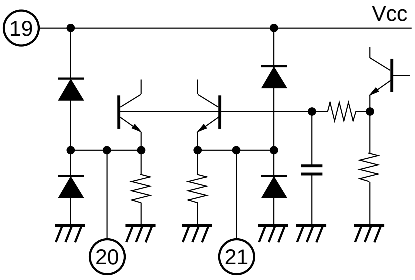
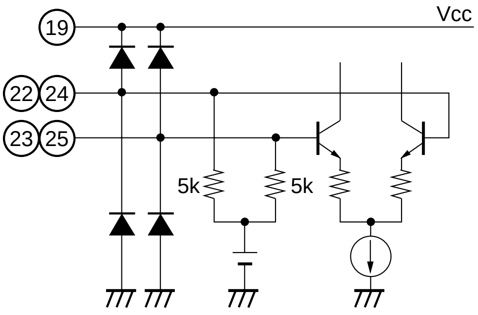
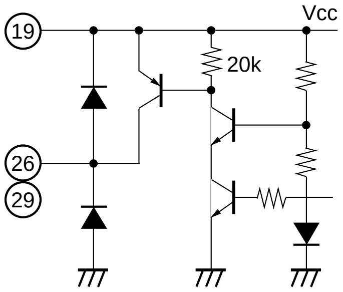
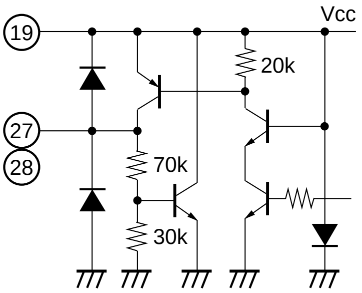
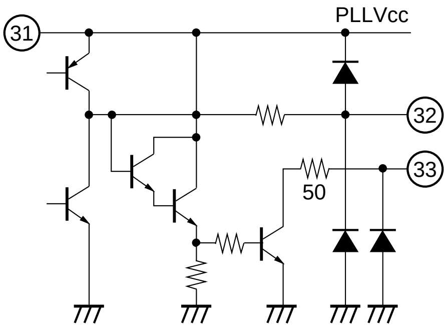
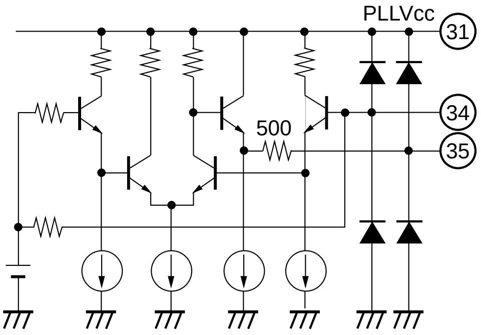
Block Diagram and Pin Configuration

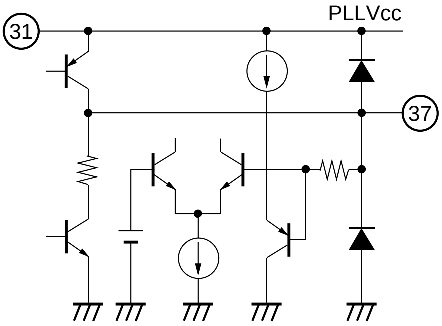
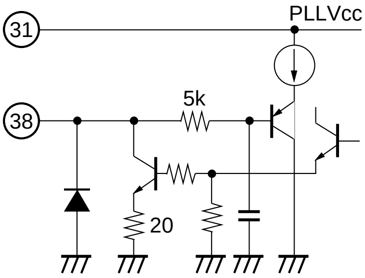
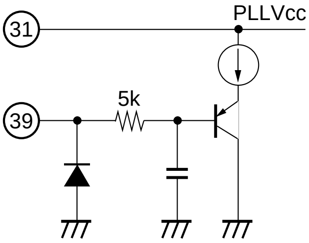
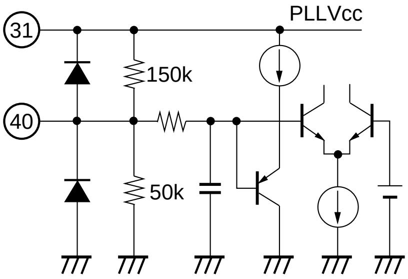

NC
BS4
BS3
BS2
BS1
VLIN1
VLIN2
VHIN1
VHIN2
UIN1
30
29
28
27
26
25
24
23
22
21
PLLVcc 31
CP 32
VT 33
XI 34
XO 35
PLLGND 36
LOCK 37
SDA 38
SCL 39
CE 40
20 UIN2
19 Vcc
18 MIXOUT1
17 MIXOUT2
16 GND
15 IFIN1
14 IFIN2
13 RFGND
12 UOSCB1
11 UOSCE1
VLMIX
VHMIX
UMIX
Ref OSC
Charge Pump
Band SW
Ref Div.
Phase Det
Program Div.
Bus Interface
Lock Det
IF Amp
VLOSC
VHOSC
UOSC
1
2
3
4
5
6
7
8
9
10
IFOUT1
IFOUT2
IFVcc
IFGND
VLOSC2
VLOSC1
VHOSC2
VHOSC1
UOSCB2
UOSCE2

Pin Description and Equivalent Circuit

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
1	IFOUT1	2.5	 3 IFVcc 40k 1 2	IF outputs. IFOUT1 and IFOUT2 output a balanced signal. When taking a signal as an unbalanced output, connect the pin not used for output to IFVcc. At this time the output stage current is saved.
2	IFOUT2			
3	IFVcc	—		IF amplifier power supply.
4	IFGND	—		IF amplifier GND.
5	VLOSC2	2.5	 5 6 19 Vcc 20k 20k 3k 3k 20k 20k	External resonance circuit connection for VL oscillator.
6	VLOSC1	2.5		
7	VHOSC2	2.5	 7 8 19 Vcc 20k 20k 3k 3k 20k 20k	External resonance circuit connection for VH oscillator.
8	VHOSC1	2.5		
9	UOSCB2	UHF: 2.2 VL/VH: 2.3	 9 10 11 12 19 Vcc 3k 3k	External resonance circuit connection for UHF oscillator.
10	UOSCE2	UHF: 1.5 VL/VH: –		
11	UOSCE1	UHF: 1.5 VL/VH: –		
12	UOSCB1	UHF: 2.2 VL/VH: 2.3		
13	RFGND	—		Analog GND.

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
14	IFIN2	2.7	 3 IFVcc 14 15 5k 5k	IF inputs.
15	IFIN1	2.7		
16	GND	0		GND
17	MIXOUT2	—		Mixer outputs.
18	MIXOUT1	—		
19	Vcc	—		Band switch, mixer and local oscillator circuit power supply.
20	UIN2	VL/VH: 0 UHF: 1.9		UHF inputs.
21	UIN1	VL/VH: 0 UHF: 1.9		
22	VHIN2	VH: 3 VL: 3.16 UHF: 3.24	 19 Vcc 22 24 23 25 5k 5k	VH and VL inputs.
23	VHIN1	VH: 3 VL: 3.16 UHF: 3.24		
24	VLIN2	VH: 3.16 VL: 3 UHF: 3.24		
25	VLIN1	VH: 3.16 VL: 3 UHF: 3.24		

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
26	BS1	ON: 4.9 OFF: 0		Pin 26: Band switch 1 output. Pin 29: Band switch 4 output. The pin corresponding to the band selected by the data goes High.
29	BS4			
27	BS2	ON: 4.9 OFF: 0		Pin 27: Band switch 2 output. Pin 28: Band switch 3 output. The pin corresponding to the band selected by the data goes High.
28	BS3			
30	NC	—		NC.
31	PLLVcc	—		PLL Vcc.
32	CP	—		Charge pump output. Connects the loop filter.
33	VT	—		Transistor open collector output for varicap diode drive. Connects the loop filter.
34	XI	3.1		External reference clock input. Connects the crystal when used as a reference oscillator.
35	XO	3.0		Connects the crystal when used as a reference oscillator.
36	PLLGND	—		PLL GND.

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
37	LOCK	5.0 (lock) 0.2 (unlock)	 31 PLLVcc 37	Lock detection. High when locked, Low when unlocked.
38	SDA	—	 31 PLLVcc 38 5k 20	Data input.
39	SCL	—	 31 PLLVcc 39 5k	Clock input.
40	CE	1.25 (when open)	 31 PLLVcc 40 150k 50k	Enable pin.

Electrical Characteristics (See the Electrical Characteristics Measurement Circuit.)

(Vcc = 5V, IFVcc = 5V, PLLVcc = 5V, Ta = 25°C)

Circuit Current

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Circuit current	Iccv1	During VHF operation Unbalanced output Band switch output open	80	113	145	mA
	Iccu1	During UHF operation Unbalanced output Band switch output open	85	120	151	mA
	Iccv2	During VHF operation Balanced output Band switch output open	91	130	170	mA
	Iccu2	During UHF operation Balanced output Band switch output open	100	137	177	mA

OSC/MIX/IF Amplifier Block

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Conversion gain 1 *1 (Unbalanced)	CG1-1	VL operation f_{RF} = 50MHz, f_{IF} = 39MHz	18.5	21.5	25	dB
	CG1-2	VL operation f_{RF} = 150MHz, f_{IF} = 39MHz	19	22	25.5	dB
	CG1-3	VH operation f_{RF} = 150MHz, f_{IF} = 39MHz	19	22	25.5	dB
	CG1-4	VH operation f_{RF} = 450MHz, f_{IF} = 39MHz	19	22	25.5	dB
	CG1-5	UHF operation f_{RF} = 450MHz, f_{IF} = 39MHz	23.5	26.5	30	dB
	CG1-6	UHF operation f_{RF} = 850MHz, f_{IF} = 39MHz	24.5	27.5	31	dB
Conversion gain 2 *1, *2 (Balanced)	CG2-1	VL operation f_{RF} = 50MHz, f_{IF} = 39MHz	25.5	28.5	32	dB
	CG2-2	VL operation f_{RF} = 150MHz, f_{IF} = 39MHz	26	29	32.5	dB
	CG2-3	VH operation f_{RF} = 150MHz, f_{IF} = 39MHz	26	29	32.5	dB
	CG2-4	VH operation f_{RF} = 450MHz, f_{IF} = 39MHz	26	29	32.5	dB
	CG2-5	UHF operation f_{RF} = 450MHz, f_{IF} = 39MHz	30.5	33.5	37	dB
	CG2-6	UHF operation f_{RF} = 850MHz, f_{IF} = 39MHz	31.5	34.5	38	dB
Noise figure *1, *3 (Unbalanced)	NF1	VL operation f_{RF} = 50MHz, f_{IF} = 39MHz		15.5	18.5	dB
	NF2	VL operation f_{RF} = 150MHz, f_{IF} = 39MHz		15	18	dB
	NF3	VH operation f_{RF} = 150MHz, f_{IF} = 39MHz		15	18	dB
	NF4	VH operation f_{RF} = 450MHz, f_{IF} = 39MHz		15	18	dB
	NF5	UHF operation f_{RF} = 450MHz, f_{IF} = 39MHz		10.5	13.5	dB
	NF6	UHF operation f_{RF} = 850MHz, f_{IF} = 39MHz		10.5	13.5	dB

OSC/MIX/IF Amplifier Block (cont.)

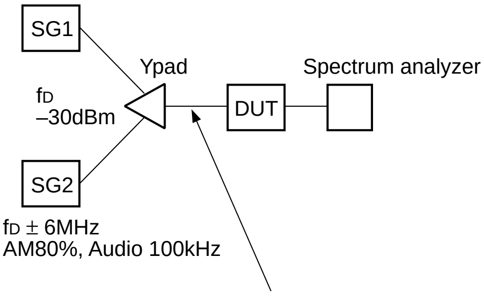
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
*1, *4 1% cross modulation 1 (Unbalanced)	CM1-1	VL operation f_D = 50MHz, f_{IF} = 39MHz, f_{UD} = ±6MHz (80% AM)	83.5	87.5		dBµ
	CM1-2	VL operation f_D = 150MHz, f_{IF} = 39MHz, f_{UD} = ±6MHz (80% AM)	83.5	87.5		dBµ
	CM1-3	VH operation f_D = 150MHz, f_{IF} = 39MHz, f_{UD} = ±6MHz (80% AM)	83	87		dBµ
	CM1-4	VH operation f_D = 450MHz, f_{IF} = 39MHz, f_{UD} = ±6MHz (80% AM)	83	87		dBµ
	CM1-5	UHF operation f_D = 450MHz, f_{IF} = 39MHz, f_{UD} = ±6MHz (80% AM)	78	82		dBµ
	CM1-6	UHF operation f_D = 850MHz, f_{IF} = 39MHz, f_{UD} = ±6MHz (80% AM)	77	81		dBµ
*1, *5 1% cross modulation 2 (Unbalanced)	CM2-1	VL operation f_D = 50MHz, f_{IF} = 39MHz, f_{UD} = ±12MHz (40% AM)	91.5	95.5		dBµ
	CM2-2	VL operation f_D = 150MHz, f_{IF} = 39MHz, f_{UD} = ±12MHz (40% AM)	91.5	95.5		dBµ
	CM2-3	VH operation f_D = 150MHz, f_{IF} = 39MHz, f_{UD} = ±12MHz (40% AM)	90	94		dBµ
	CM2-4	VH operation f_D = 450MHz, f_{IF} = 39MHz, f_{UD} = ±12MHz (40% AM)	89	93		dBµ
	CM2-5	UHF operation f_D = 450MHz, f_{IF} = 39MHz, f_{UD} = ±12MHz (40% AM)	85	89		dBµ
	CM2-6	UHF operation f_D = 850MHz, f_{IF} = 39MHz, f_{UD} = ±12MHz (40% AM)	84	88		dBµ
Maximum output power	Pomax	50Ω load, saturation output, f_{IF} = 45MHz	+10	+13		dBm
Phase noise 1 *6	PN 1	1kHz offset Phase comparison frequency = 218.75kHz Charge pump current: 900µA		73		dBc/Hz
Phase noise 2 *6	PN 2	10kHz offset Phase comparison frequency = 218.75kHz Charge pump current: 900µA		90		dBc/Hz
*6, *7 Oscillator phase noise	C/N	50kHz offset Phase comparison frequency = 218.75kHz Charge pump current variable	60	70		dBc

[*1] Value measured with the untuned input.

[*2] Value compensated for the loss due to the external parts connected to Pins 1 and 2, and converted to the IC output pin amplitude.

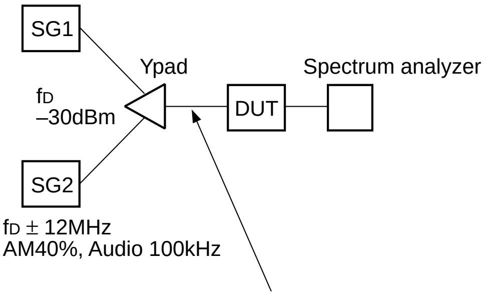
[*3] Noise figure is the direct-reading value of NF meter in DSB.

[*4]


SG1
Ypad
Spectrum analyzer
fD
–30dBm
DUT
SG2
fD ± 6MHz
AM80%, Audio 100kHz

Input value (SG2, 50Ω termination) when S/I = 46dB with the spectrum analyzer

[*5]


SG1
Ypad
Spectrum analyzer
fD
–30dBm
DUT
SG2
fD ± 12MHz
AM40%, Audio 100kHz

Input value (SG2, 50Ω termination) when S/I = 46dB with the spectrum analyzer

[*6] Value when 14MHz (300mVp-p) is SG (Hewlett-Packard Japan, Ltd.: 8644A) input as the external REF CLOCK.

[*7] The spectrum analyzer is set for SPAN:100kHz, RBW:3kHz and VBW:100Hz.

PLL Block

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Lock-up time 1	LUT1	fosc 89MHz ⟷ fosc 479MHz		10		ms
Lock-up time 2	LUT2	fosc 479MHz ⟷ fosc 889MHz		10		ms
Reference leak	REFL	Phase comparison frequency = 218.75kHz		65		dBc
CL and DA input						
"H" level input voltage	V_{IH}		3		Vcc	V
"L" level input voltage	V_{IL}		GND		1.5	V
"H" level input current	I_{IH}	V_{IH} = Vcc		0	–0.1	µA
"L" level input current	I_{IL}	V_{IL} = GND		–0.2	–4	µA
CE input						
"H" level input voltage	V_{IH}		3		Vcc	V
"L" level input voltage	V_{IL}		GND		1	V
"H" level input current	I_{IH}	V_{IH} = Vcc		100	200	µA
"L" level input current	I_{IL}	V_{IL} = GND		–35	–100	µA
CPO (charge pump)						
Output current 1	I_{CPO2}	When 300µA is selected	±210	±300	±420	µA
Output current 2	I_{CPO4}	When 900µA is selected	±600	±900	±1215	µA
VT (VC voltage output)						
Maximum output voltage	V_{TH}				33	V
Minimum output voltage	V_{TL}	Sink current = 1mA		0.3	0.8	V
REFOSC						
Oscillation frequency range	F_{XTOSC}		3	4	5	MHz
Drive frequency	REFIN1		3	14	20	MHz
Drive level	REFIN2	External reference clock: sine wave	250	350	500	mVp-p
Band SW						
Output current	I_{BS}	When ON			–5	mA
Saturation voltage	V_{SAT}	When ON Source current = 5mA		150	300	mV
Leak current	$Leak_{BS}$	When OFF IFV_{CC} = 5.5V		0.5	3	µA
LOCK						
"H" output voltage	VLOCKH	When locked	Vcc – 1	Vcc – 0.3	Vcc	V
"L" output voltage	VLOCKH	When unlocked	0	0.1	0.5	V

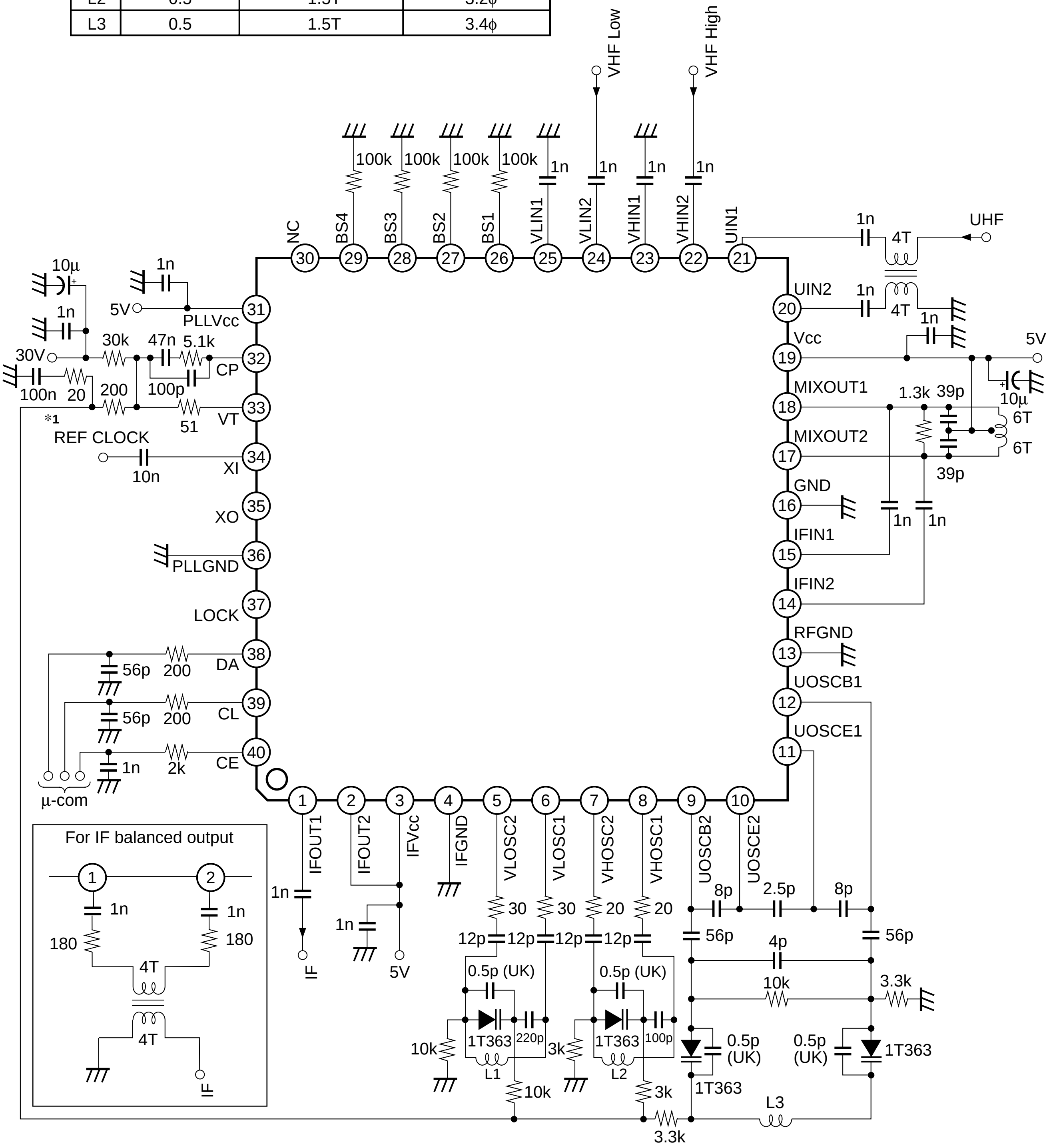
PLL Block (cont.)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Bus timing (3-wire bus)						
Data setup time	t_{SD}		300			ns
Data hold time	t_{HD}		600			ns
Enable waiting time	t_{WE}		300			ns
Enable setup time	t_{SE}		300			ns
Enable hold time	t_{HE}		600			ns

Electrical Characteristics Measurement Circuit

Inductance Constants

	Wire diameter	Number of windings	Winding diameter
L1	0.5	7.5T	3.2ϕ
L2	0.5	1.5T	3.2ϕ
L3	0.5	1.5T	3.4ϕ


VHF Low
VHF High
100k
100k
100k
100k
1n
1n
1n
1n
NC
BS4
BS3
BS2
BS1
VLIN1
VLIN2
VHIN1
VHIN2
UIN1
30
29
28
27
26
25
24
23
22
21
1n
4T
UHF
UIN2
1n
4T
1n
20
Vcc
5V
19
MIXOUT1
1.3k
39p
18
10μ
6T
MIXOUT2
17
6T
39p
GND
16
1n
1n
IFIN1
15
IFIN2
14
RFGND
13
UOSCB1
12
UOSCE1
11
10μ
1n
1n
5V
PLLVcc
31
30V
30k
47n
5.1k
32
CP
100n
20
200
100p
*1
51
VT
33
REF CLOCK
34
10n
XI
35
XO
36
PLLGND
37
LOCK
38
56p
200
DA
39
56p
200
CL
40
1n
2k
CE
μ-com
1
2
3
4
5
6
7
8
9
10
IFOUT1
IFOUT2
IFVcc
IFGND
VLOSC2
VLOSC1
VHOSC2
VHOSC1
UOSCB2
UOSCE2
1n
IF
1n
5V
30
30
20
20
12p
12p
12p
12p
0.5p (UK)
0.5p (UK)
10k
1T363
220p
L1
10k
3k
1T363
100p
L2
3k
3.3k
8p
2.5p
8p
56p
4p
56p
10k
3.3k
0.5p
(UK)
1T363
0.5p
(UK)
1T363
L3
For IF balanced output
1
2
1n
1n
180
180
4T
4T
IF

*1: 14MHz, sine wave, 300mVp-p input (Hewlett-Packard Japan, Ltd.: 8644A)

Description of Operation

The CXA3275Q is a tuner IC which frequency converts 55 to 860MHz cable digital broadcasts to IF.
In addition to the mixer, local oscillation and IF amplifier circuits required for frequency conversion to IF, this IC also integrates a PLL circuit for local oscillation frequency control onto a single chip.
The functions of the various circuits are described below.

1. Mixer circuit

This circuit outputs the frequency difference between the signal input to VLIN, VHIN or UIN and the local oscillation signal.
There are three sets of mixer circuits for VHF Low Band, VHF High Band and UHF Band.
VHF Low and VHF High are common emitter type mixer input circuits, and UHF is a common base type mixer input circuit.

2. Local oscillation circuit

A VCO is formed by externally connecting an LC resonance circuit composed of a varicap diode and inductance.
There are three sets of oscillation circuits for VHF Low Band, VHF High Band and UHF Band.
VHF Low and VHF High are 2-pin fully differential oscillation circuits and UHF is a 4-pin fully differential oscillation circuit.

3. IF amplifier circuit

This circuit amplifies the mixer IF output, and consists of an amplifier stage and low impedance output stage.
IF output is low impedance (emitter follower output), and can be selected from balanced and unbalanced output.
When unbalanced output is selected, the output stage current can be saved by connecting the pin not used for output to IFVcc.

4. PLL circuit

This PLL circuit controls the local oscillation frequency.
It consists of a programmable divider, phase comparator, charge pump and reference oscillator.
The control format supports the 3-wire bus format.

5. Band switch circuit

The MT58A has four sets of built-in PNP transistors which can be controlled by the bus data.
These outputs switch the on-chip mixer and oscillator circuits, and the relationship with the control data is as shown in the table below.

Relationship between the Band Switch Data and Mixer/Oscillator Operation

Band switch data				Mixer circuit			Oscillation circuit		
BS1	BS2	BS3	BS4	VHF Low	VHF High	UHF	VHF Low	VHF High	UHF
*	1	0	*	O	X	X	O	X	X
*	0	1	*	X	O	X	X	O	X
*	0	0	*	X	X	O	X	X	O

*: Don't care
O: Operating
X: Not operating

Description of PLL Block

The CXA3275Q supports the 3-wire bus control format.
Serial data is transferred using the DA pin (DATA), CL pin (CLOCK) and CE pin (ENABLE) inputs. Data is loaded to the shift register at the falling edge of the clock signal, and is latched at the falling edge of the enable signal.
The clocks during the enable period are counted, and 28 bits of data as counted from the rising edge of the enable signal are loaded as valid data.
The MT58A has the power-on reset function and the register data become all "0" after the power is turned on.
The threshold value of the power-on reset is approximately 3.0V.

The VCO lock frequency is obtained according to the following formula.

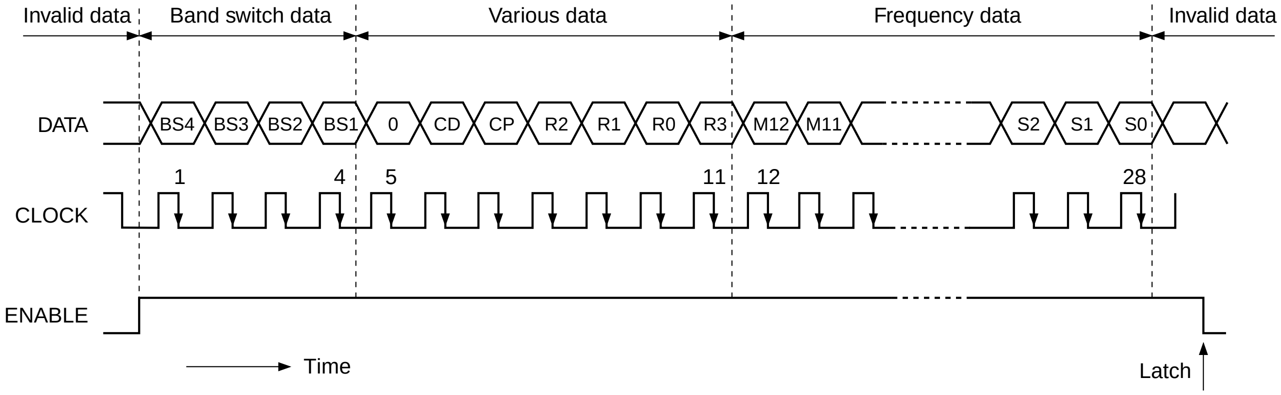
$f_{osc} = f_{ref} \times (16M + S)$ fosc: Local oscillator frequency fref: Phase comparison frequency
M: Main divider frequency division ratio S: Swallow counter frequency division ratio

The variable frequency division ranges of M and S are as follows, and are set as binary.

$S < M \leq 8191$

$0 \leq S \leq 15$

The control format is as shown below.
Serial data (total 28 bits): Band data (4 bits) + various settings (3 bits)
+ reference frequency data (4 bits) + frequency data (17 bits)



M0 to:	Main divider frequency division ratio setting
S0 to:	Swallow counter frequency division ratio setting
CD:	Charge pump OFF and varicap output OFF (when "1")
CP:	Charge pump current switching (See the Charge Pump Current Table.)
BS1 to BS4:	Band switch control (Output PNP transistor ON when "1". See the Band Switch Output Table.)
R0 to R3:	Reference divider frequency division ratio setting. (See the Reference Divider Frequency Division Ratio Table.)

Charge Pump Current Table

Charge pump current	CP
300µA	0
900µA	1

Reference Divider Frequency Division Ratio Table

R3	R2	R1	R0	Frequency division ratio
0	0	0	0	2
0	0	0	1	4
0	0	1	0	8
0	0	1	1	16
0	1	0	0	32
0	1	0	1	64
0	1	1	0	128
0	1	1	1	256
1	0	0	0	512
1	0	0	1	6
1	0	1	0	12
1	0	1	1	24
1	1	0	0	48
1	1	0	1	96
1	1	1	0	192
1	1	1	1	384

Band Switch Output Table

Band switch data				Band switch pins				Operating mode (MIX/OSC)
BS1	BS2	BS3	BS4	BS1	BS2	BS3	BS4	
1	0	0	0	ON	OFF	OFF	OFF	UHF
0	1	0	0	OFF	ON	OFF	OFF	VL
0	0	1	0	OFF	OFF	ON	OFF	VH
0	0	0	1	OFF	OFF	OFF	ON	UHF

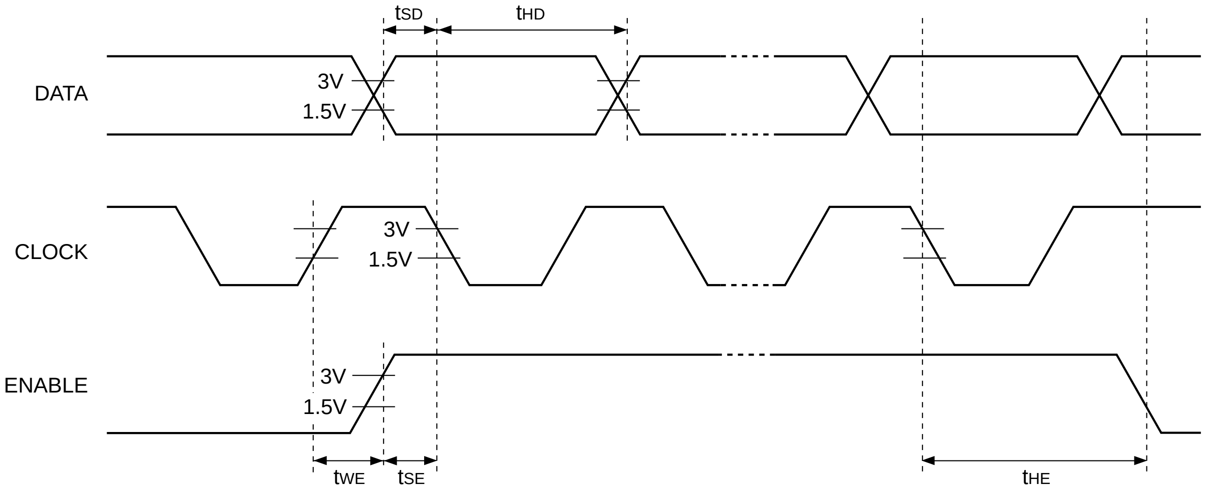
<Supplement>

- Operation for Power On

  When the data transfer is not performed after the power on, both the mixer and oscillator blocks operate in UHF as the register data are all "0" by the power-on reset.

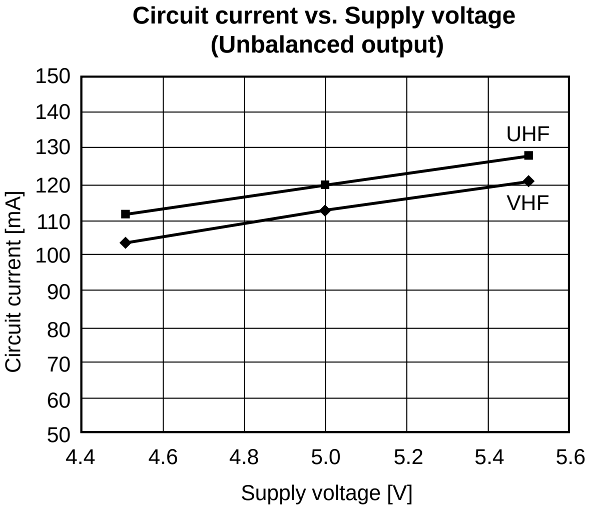
  At this time, the Pin 33 (VT) voltage becomes the value equal to the varicap diode supply voltage (30V) when the external clock is input to Pin 34 (XI) or when the crystal is connected to this pin for self-oscillation. When the external clock is not input simultaneously with the power-on or the crystal is not connected, the Pin 33 voltage becomes unstable.

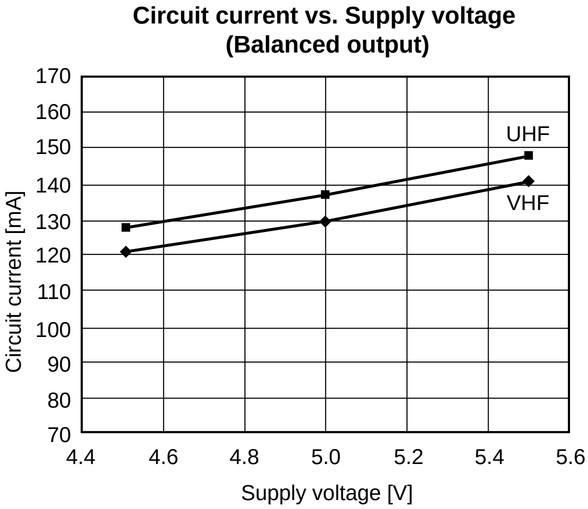
3-wire Bus Timing Chart

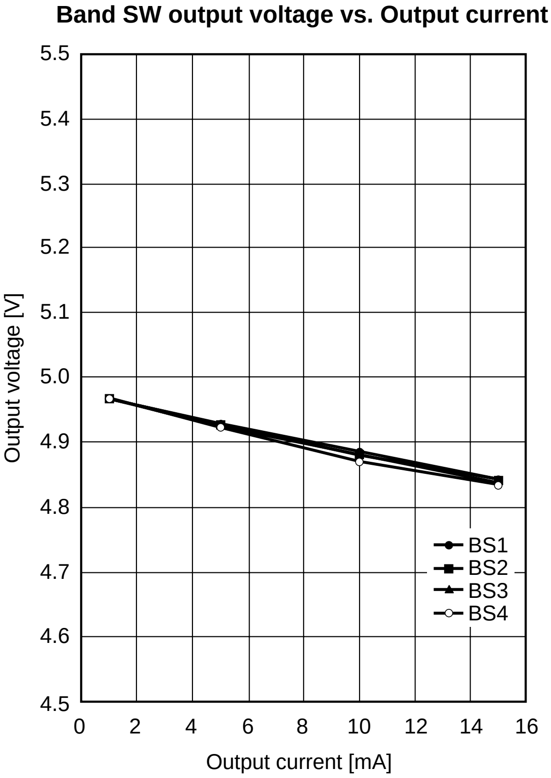

tSD
tHD
DATA
3V
1.5V
CLOCK
3V
1.5V
ENABLE
3V
1.5V
tWE
tSE
tHE

tSD: Data setup time	tHE: Enable hold time
tHD: Data hold time	tWE: Enable waiting time
tSE: Enable setup time	

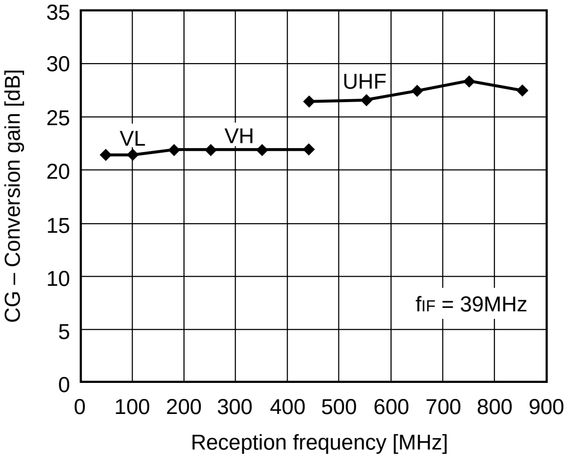
Characteristics Graphs



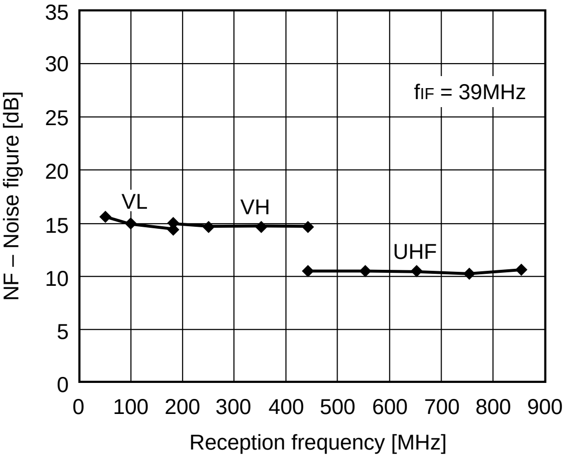




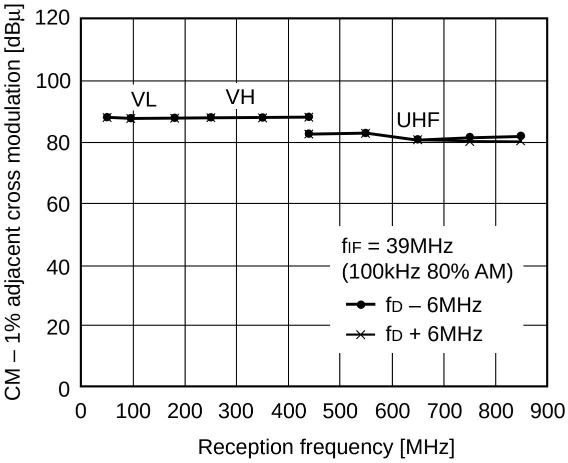
Conversion gain vs. Reception frequency (Untuned input)



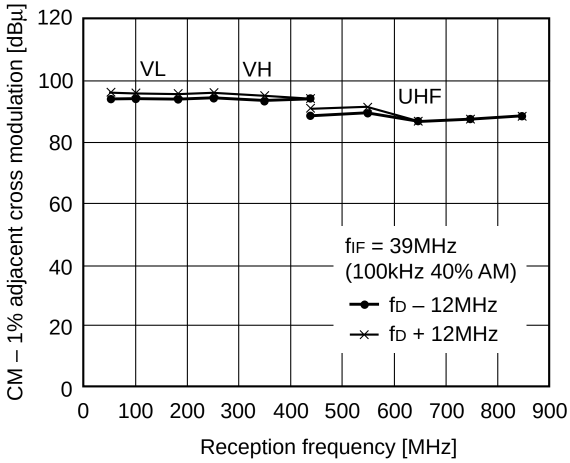
Noise figure vs. Reception frequency (Untuned input, in DSB)



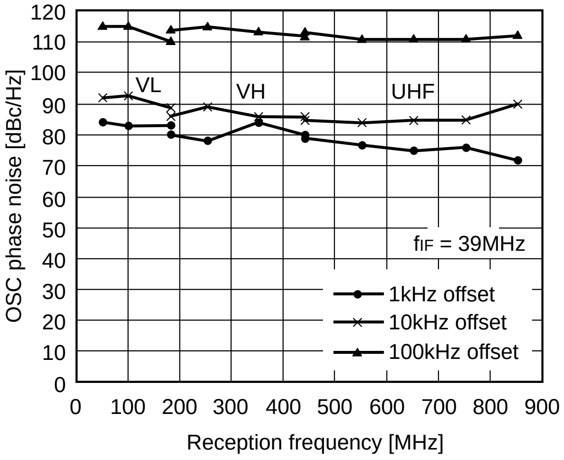
1% adjacent cross modulation vs. Reception frequency (Untuned input)



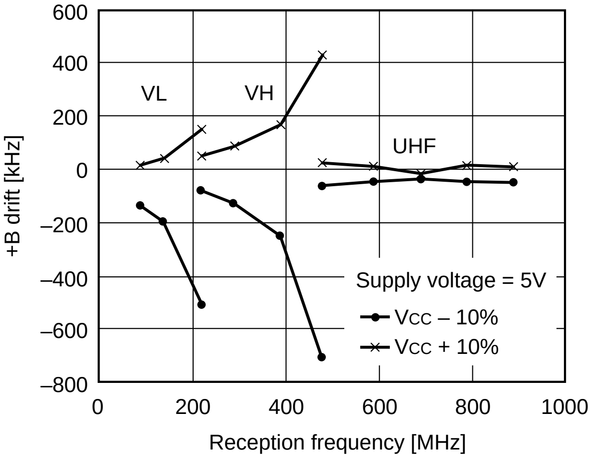
1% adjacent cross modulation vs. Reception frequency (Untuned input)



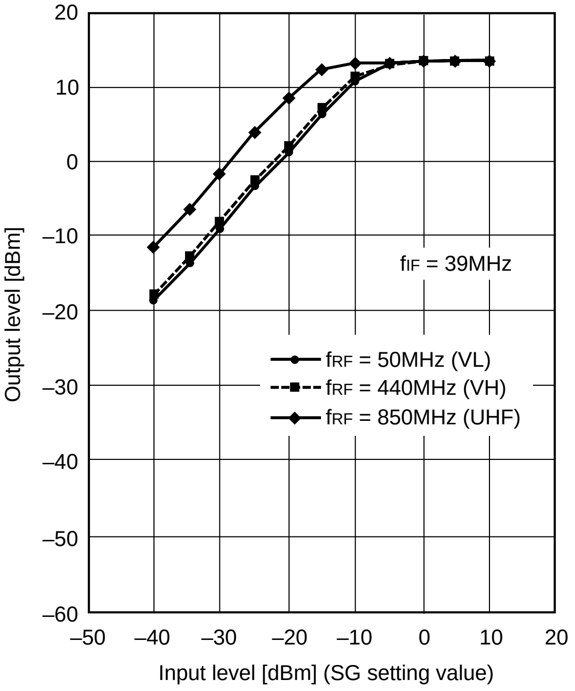
OSC phase noise vs. Reception frequency (Untuned input)



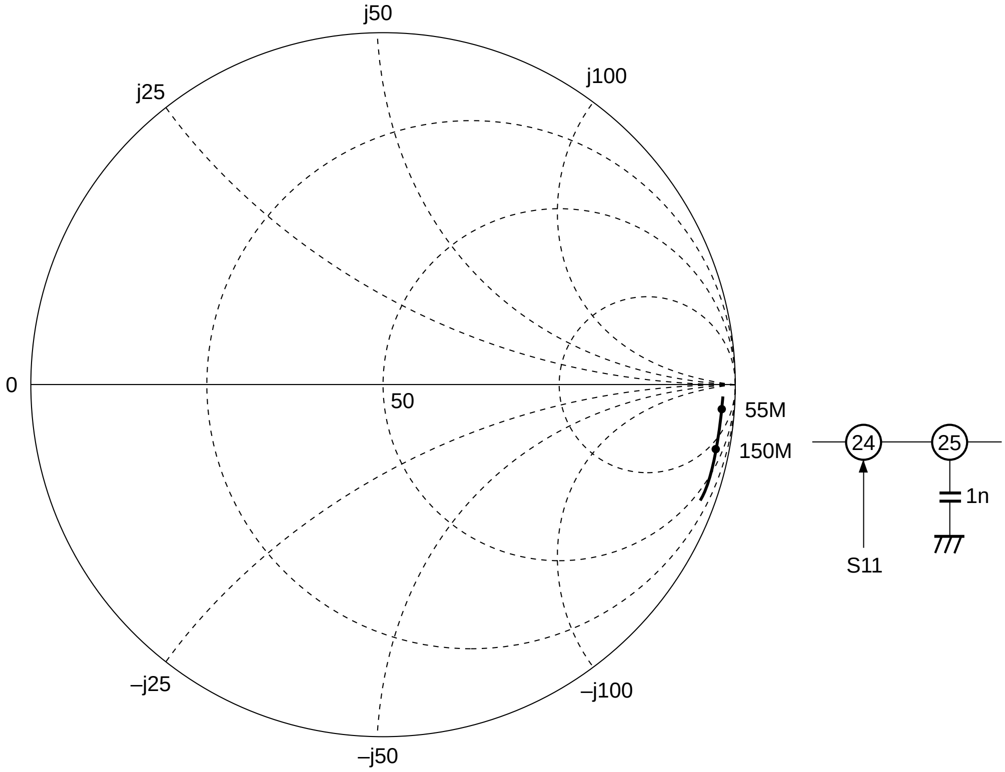
Oscillation frequency supply voltage fluctuation (PLL off)



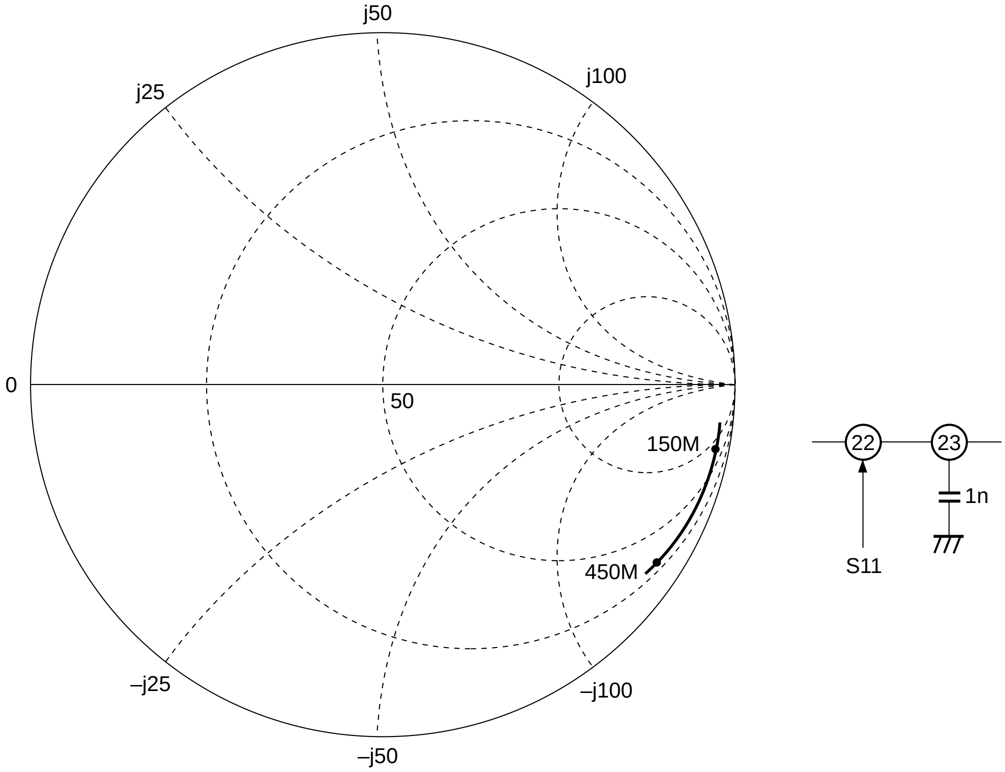
Input/output characteristics (Untuned input)



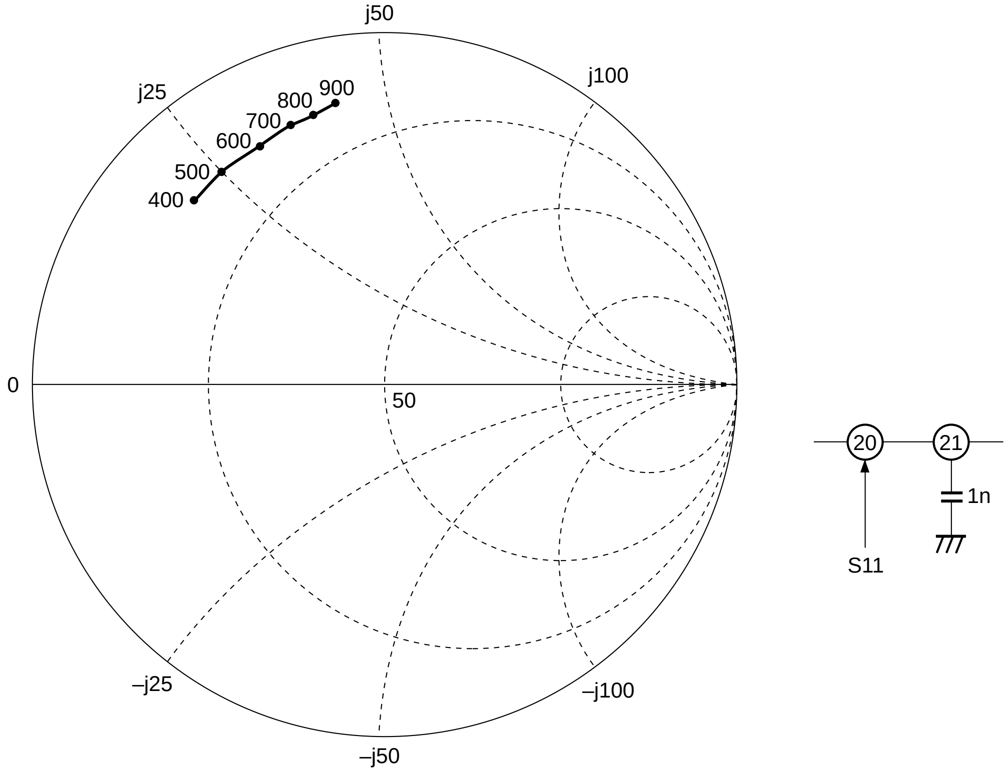
VHF Low Input Impedance



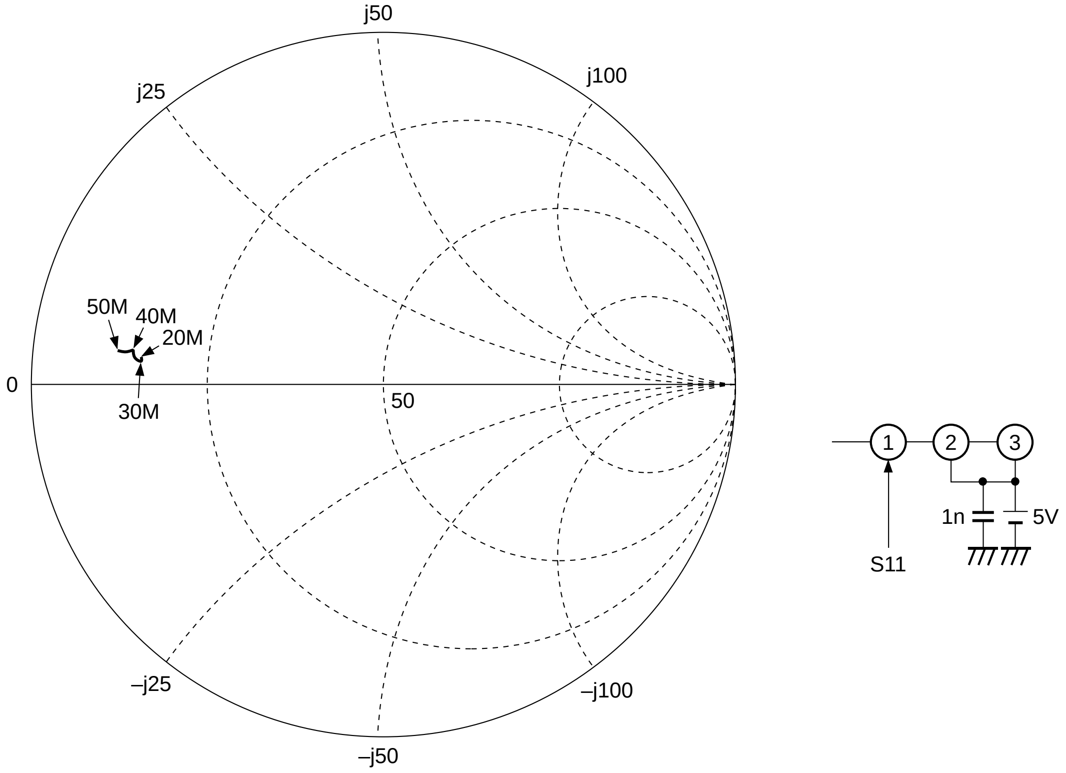
VHF High Input Impedance



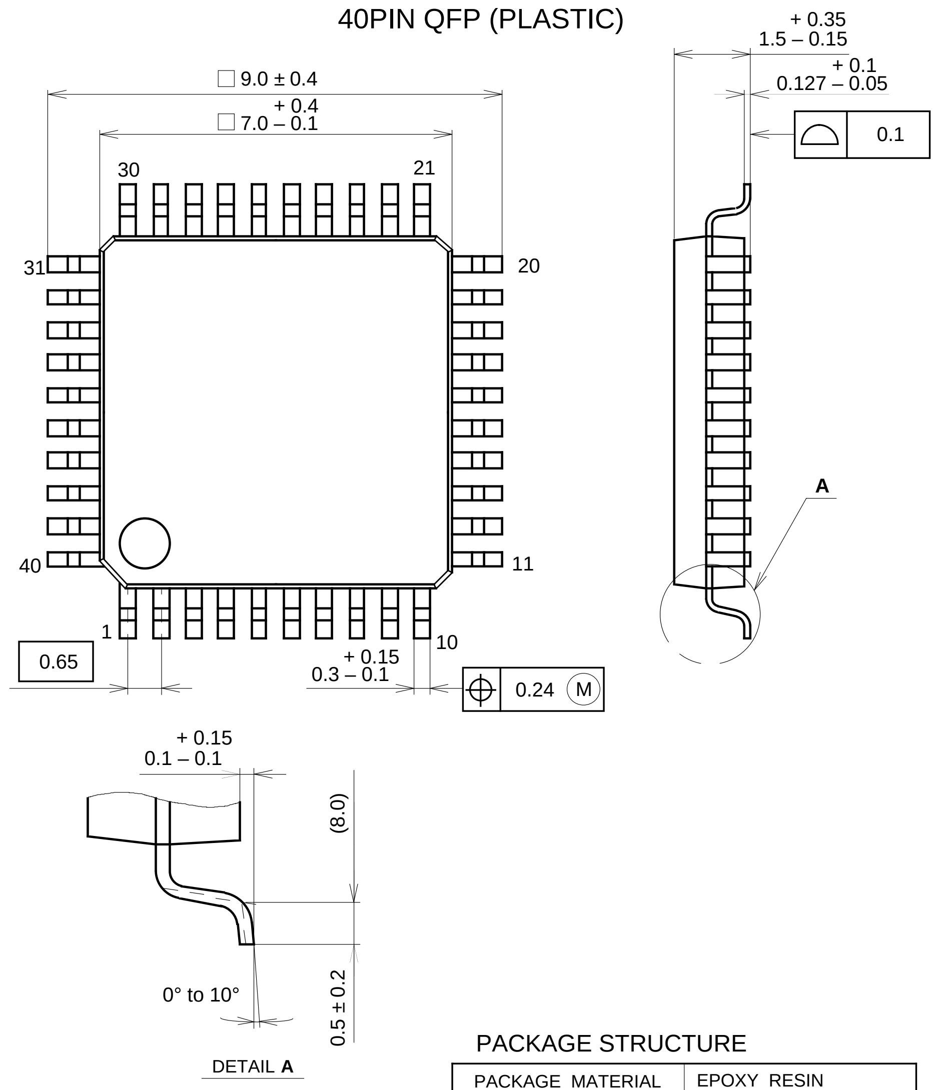
UHF Input Impedance



IF Output Impedance



Package Outline Unit: mm


40PIN QFP (PLASTIC)
□ 9.0 ± 0.4
□ 7.0 + 0.4 – 0.1
1.5 + 0.35 – 0.15
0.127 + 0.1 – 0.05
0.1
30
21
31
20
40
11
1
10
A
0.65
0.3 + 0.15 – 0.1
0.24 M
0.1 + 0.15 – 0.1
(8.0)
0.5 ± 0.2
0° to 10°
DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-40P-L01
EIAJ CODE	QFP040-P-0707
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).