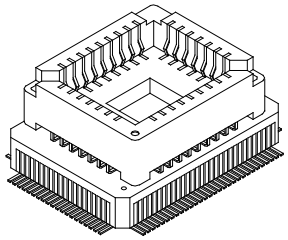
SONY

CXP82800

CMOS 8-bit Single Chip Microcomputer

Piggyback/evaluator

100 pin PQFP (Ceramic)



Description

The CXP82800 is a CMOS 8-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP82832/82840/82852/82860.

Features

- Wide-range instruction system (213 instructions) to cover various types of data
  - 16-bit operation/multiplication and division/ Boolean bit operation instructions
- Minimum instruction cycle 400ns at 10MHz operation
  122µs at 32kHz operation
- Applicable EPROM LCC type 27C512 (Maximum 60K bytes are available.)
- Incorporated RAM capacity 1536 bytes (Including fluorescent display data area)
- Peripheral functions

— A/D converter	8-bit, 8-channel, successive approximation method (Conversion time of 32µs/10MHz)
— Serial interface	Incorporated 8-bit, 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel 8-bit clock sync type, 1 channel
— Timers	8-bit timer 8-bit timer/counter 19-bit time base timer 16-bit capture timer/counter 32kHz timer/counter
— Fluorescent display panel controller/driver	Supports the universal grid fluorescent display panel. High voltage drive output port of 56 pins (40V) Maximum of 640 segments display possible Display timing number of 1 to 20 Dimmer function Incorporated pull-down resistor (Mask option) Hardware key scan function (Maximum 16 × 8 key matrix compatible)
— Remote control receiving circuit	8-bit pulse measurement counter with on-chip 6-stage FIFO
— PWM output	14 bits, 1 channel

- Interruption 16 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 100-pin ceramic PQFP

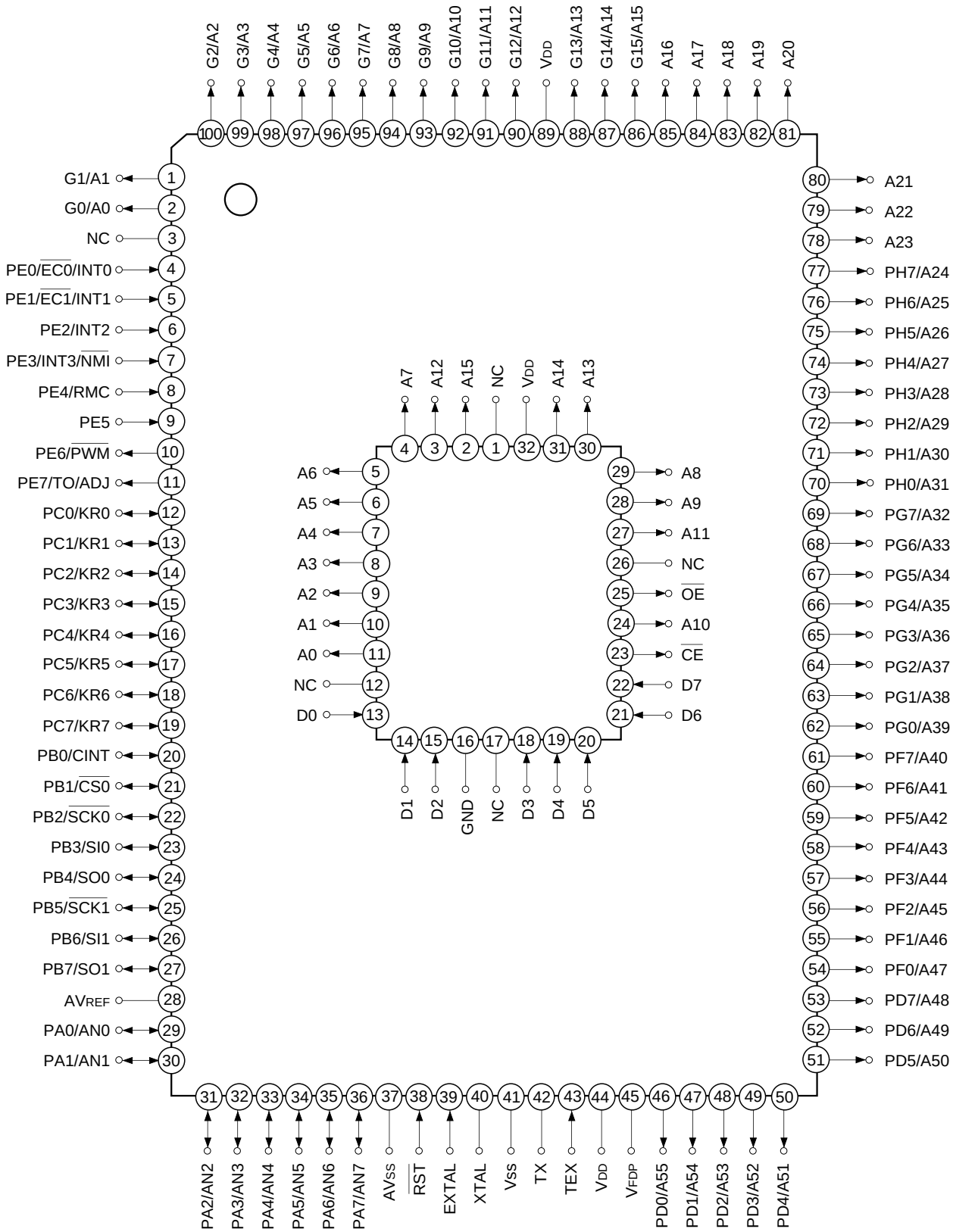
Note) Mask option depends on the type of the CXP82800. Refer to the Products List for details.

Structure

Silicon gate CMOS IC

E96529-ST

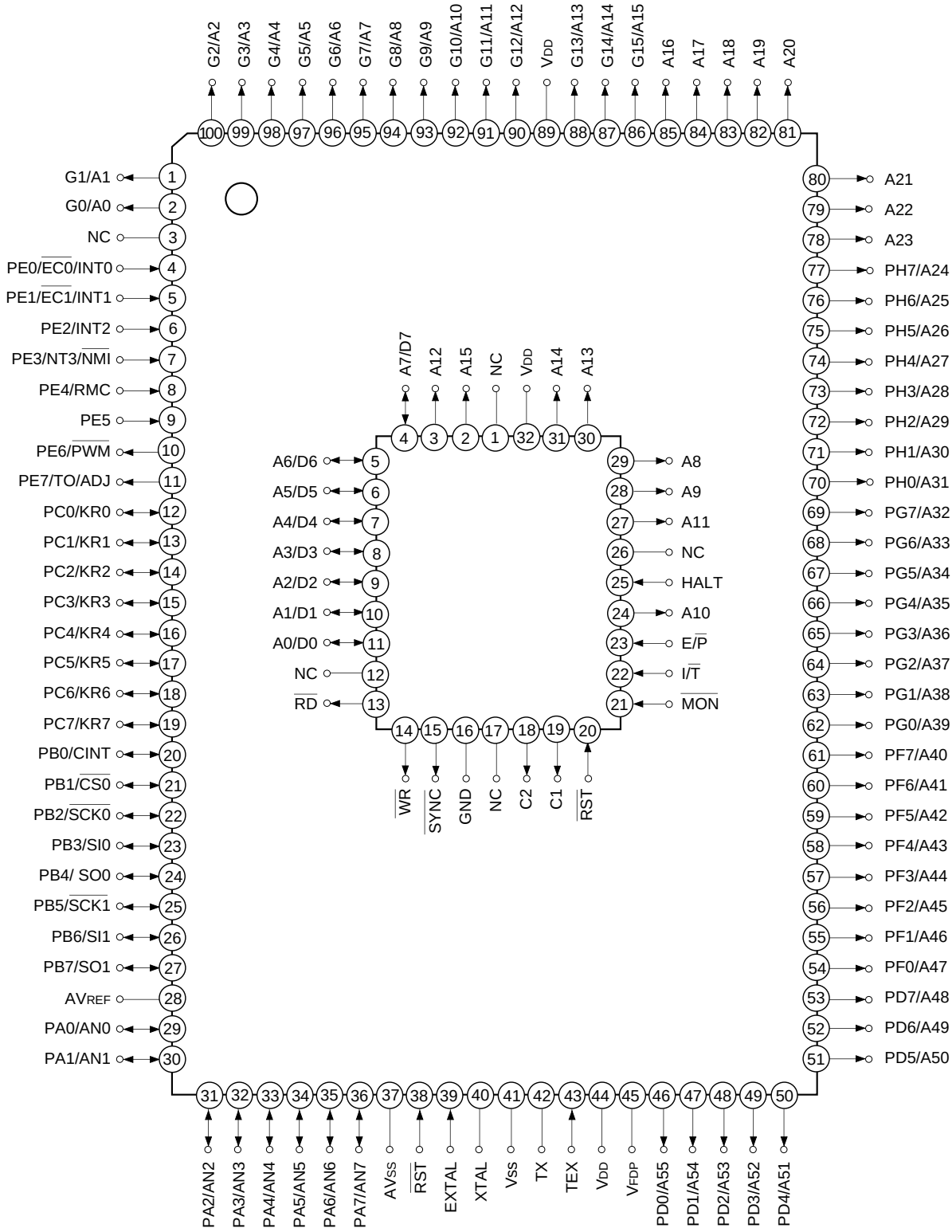
Pin Configuration in Piggyback Mode



Note) 1. NC (Pin 3) is always connected to V_{DD}.

2. V_{DD} (Pins 44 and 89) are both connected to V_{DD}.

Pin Configuration in Evaluator Mode

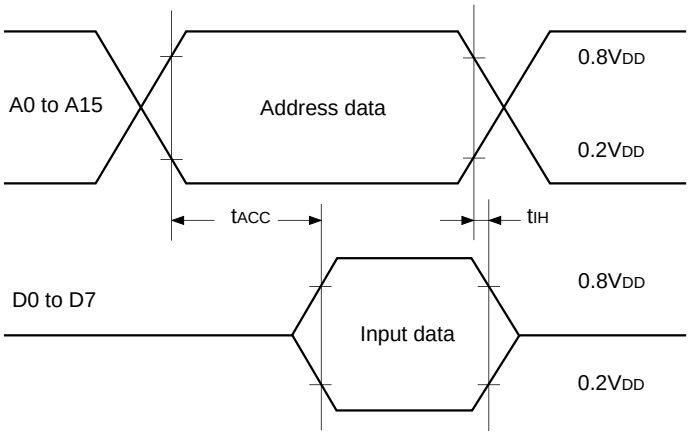


Note) 1. NC (Pin 3) is always connected to V_{DD}.
2. V_{DD} (Pins 44 and 89) are both connected to V_{DD}.

EPROM Read Timing

(Ta = –20 to +75°C, Vcc = 4.5 to 5.5V, Vss = 0V reference)

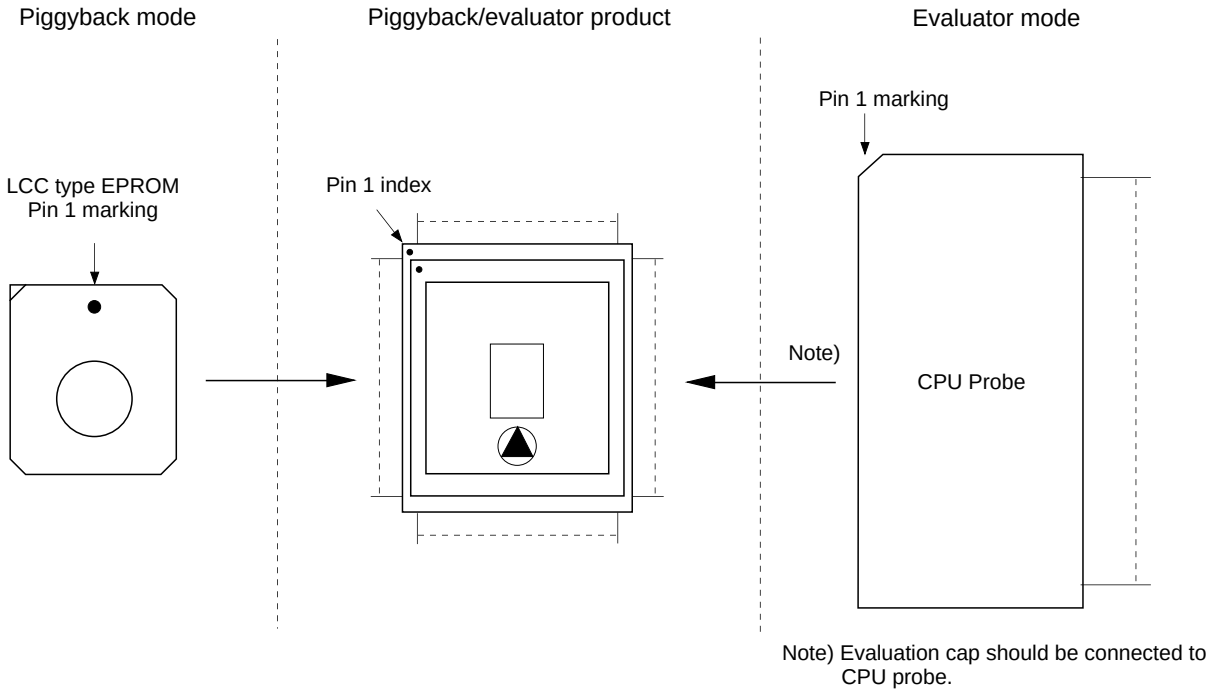
Item	Symbol	Pins	Min.	Max.	Unit
Address → Data input delay time	t_{ACC}	A0 to A15 D0 to D7		120	ns
Address → Data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns



Products List

Option item	Products				
	Mask				Piggyback/evaluator
	CXP82832	CXP82840	CXP82852	CXP82860	CXP82800-U01Q
Package	100-pin plastic QFP				100-pin ceramic PQFP
ROM capacitance	32K bytes	40K bytes	52K bytes	60K bytes	EPROM 60K bytes
Pull-up resistance for reset pin	Existent/Non-existent				Existent
Pull-down resistance for high voltage drive pin	Existent/Non-existent				Existent: G0/A0 to A23 Non-existent: PD0/A55 to PH7/A24

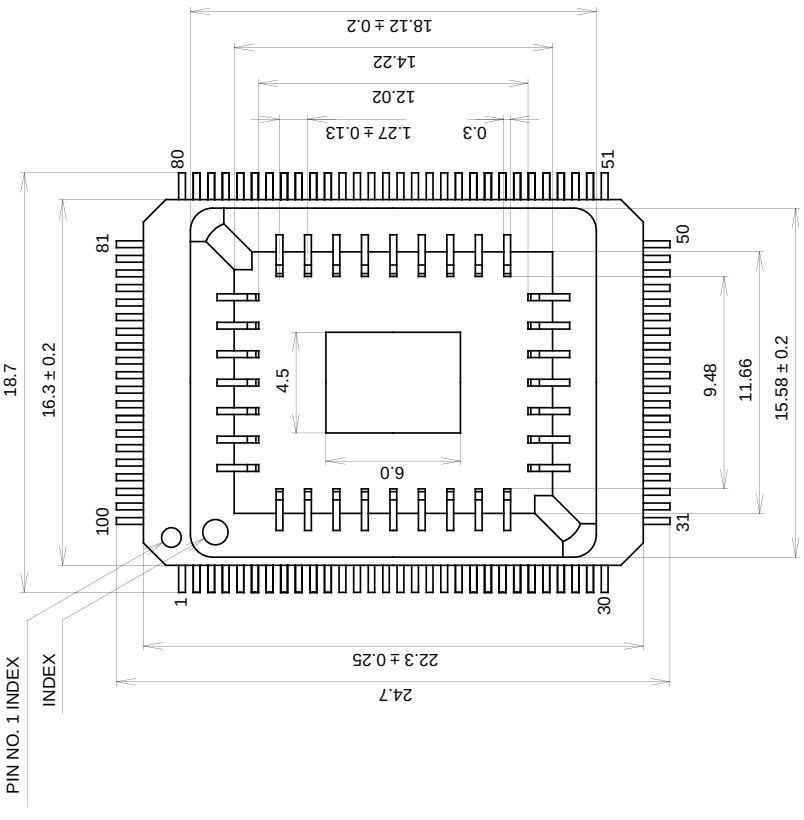
Piggyback mode/evaluator mode can be switched as shown below.

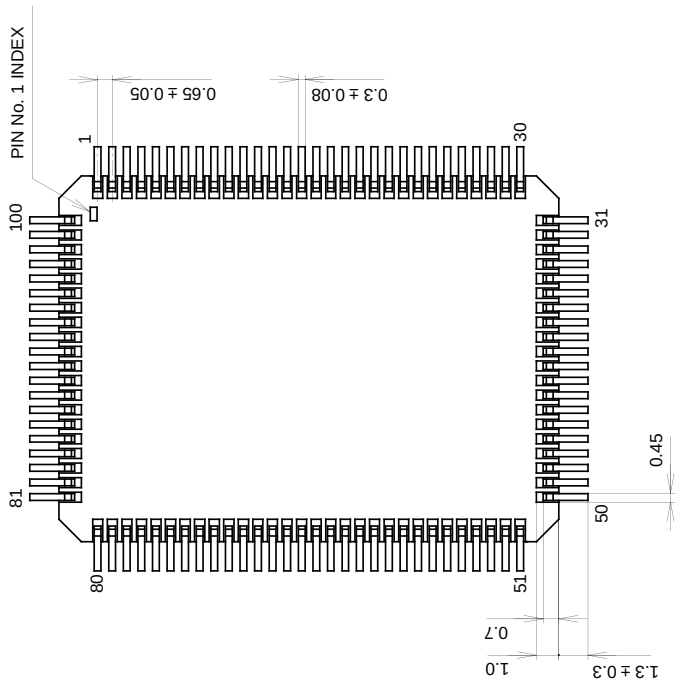


Note) Evaluation cap should be connected to CPU probe.

Package Outline Unit: mm

100PIN PQFP (CERAMIC)





PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	————