SONY

# CXA1386P/K

## 8-bit 75MSPS Flash A/D Converter

### Description

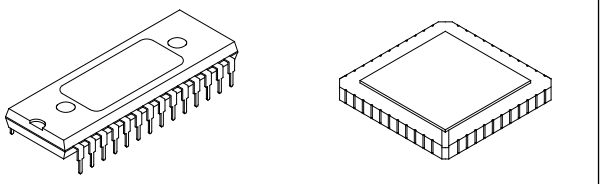
The CXA1386P/K are 8-bit high-speed flash A/D converter ICs capable of digitizing analog signals at the maximum rate of 75MSPS. The digital I/O levels of these A/D converters are compatible with the ECL 100K/10KH/10K.

The CXA1386P/K is pin-compatible with the earlier models CXA1056P/K, CXA1016P/K, respectively. They can be replaced by the CXA1386P/K without any design changes, in most cases. Compared with the earlier models, these new models have been greatly improved in performance, by incorporating advanced process, new circuit design and carefully considered layout.

### Features

- Differential linearity error: ±1/2LSB or less
- Integral linearity error: ±1/2LSB or less
- High-speed operation with maximum conversion rate of 75MSPS (Min.)
- Wide analog input bandwidth: 150MHz (Min. for full-scale input)
- Low Power consumption: 580mW (Typ.)
- Single power supply: –5.2V
- Low input capacitance: 17pF (Typ.)
- Built-in integral linearity conpensation circuit
- Low error rate
- Operable at 50% clock duty cycle
- Good temperature characteristics
- Capable of driving 50Ω loads

| CXA1386P | CXA1386K |
|---|---|
| 28 pin DIP (Plastic) | 44 pin LCC (Ceramic) |



### Structure

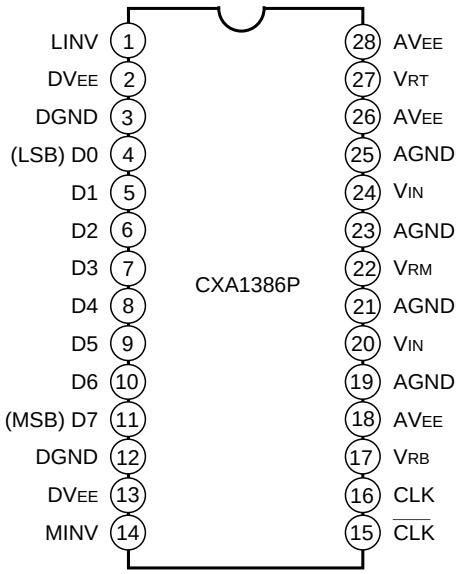
Bipolar silicon monolithic IC

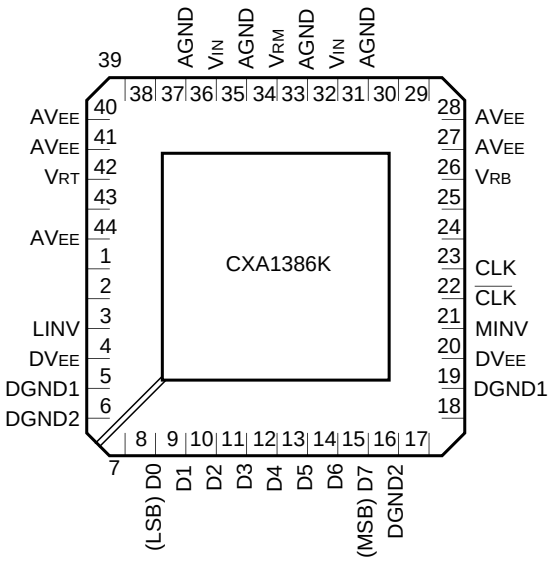
### Applications

- Digital oscilloscopes
- HDTV (high-definition TVs)
- Other apparatus requiring high-speed A/D conversion

### Pin Configuration

Pins with name are NC pins (not connected).







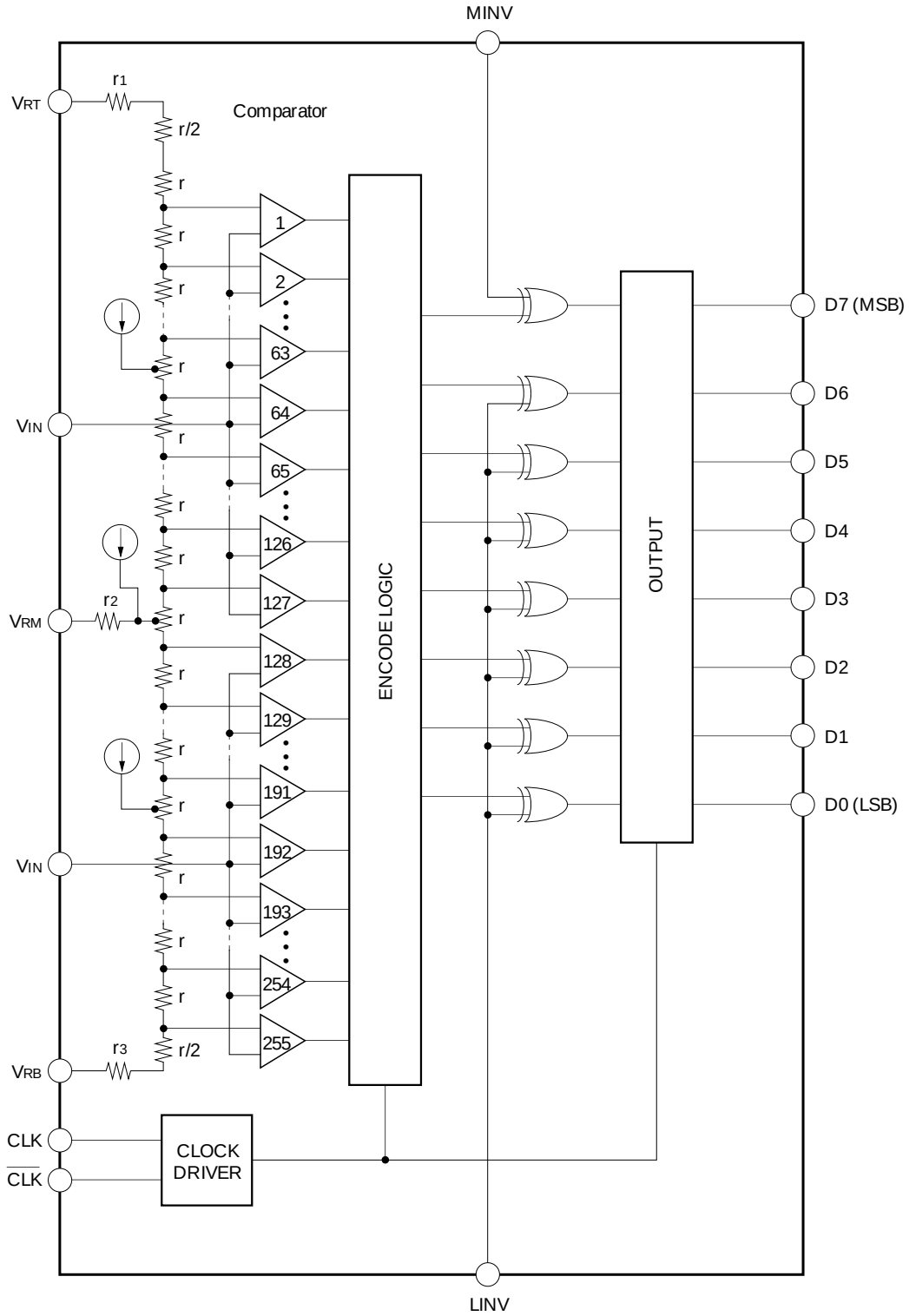

E90114C54-ST

**Absolute Maximum Ratings** (Ta = 25°C)

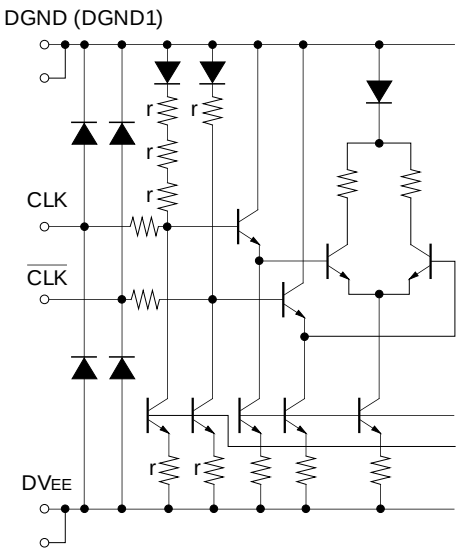
| | | | |
|---|---|---|---|
| • Supply voltage | $AV_{EE}$, $DV_{EE}$ | –7 to +0.5 | V |
| • Analog input voltage | $V_{IN}$ | –2.7 to +0.5 | V |
| • Reference input voltage | $V_{RT}$, $V_{RB}$, $V_{RM}$ | –2.7 to +0.5 | V |
| | I $V_{RT}$ – $V_{RB}$ I | 2.5 | V |
| • Digital input voltage | CLK, $\overline{CLK}$, MINV, LINV | –4 to +0.5 | V |
| | I CLK – $\overline{CLK}$ I | 2.7 | V |
| • $V_{RM}$ pin input current | $I_{VRM}$ | –3 to +3 | mA |
| • Digital output current | $ID_0$ to $ID_7$ | –30 to 0 | mA |
| • Storage temperature | Tstg | –65 to +150 | °C |

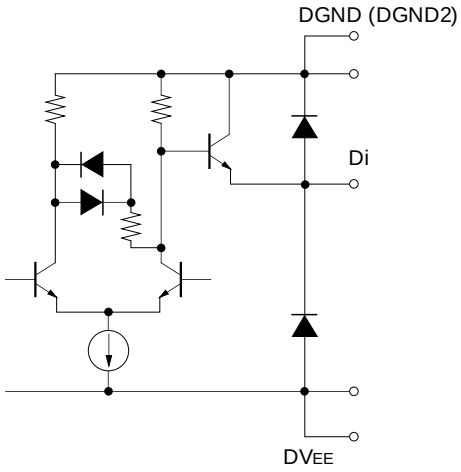
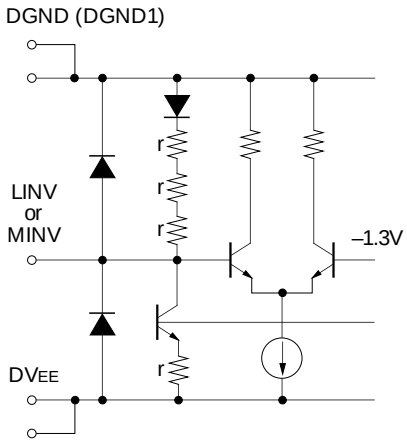
| **Recommended Operating Conditions** | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| • Supply voltage | $AV_{EE}$, $DV_{EE}$ | –5.5 | –5.2 | –4.95 | V |
| | $AV_{EE}$ – $DV_{EE}$ | –0.05 | 0 | +0.05 | V |
| | AGND – DGND | –0.05 | 0 | +0.05 | V |
| • Reference input voltage | $V_{RT}$ | –0.1 | 0 | +0.1 | V |
| | $V_{RB}$ | –2.2 | –2.0 | –1.8 | V |
| • Analog input voltage | $V_{IN}$ | $V_{RB}$ | | $V_{RT}$ | |
| • Pulse width of clock | $T_{PW1}$ | 6.6 | | | ns |
| | $T_{PW0}$ | 6.6 | | | ns |
| • Operating temperature | Tc (CXA1386K) | –20 | | +100 | °C |
| | Ta (CXA1386P) | –20 | | +75 | °C |

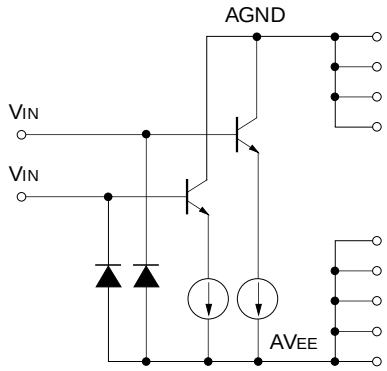
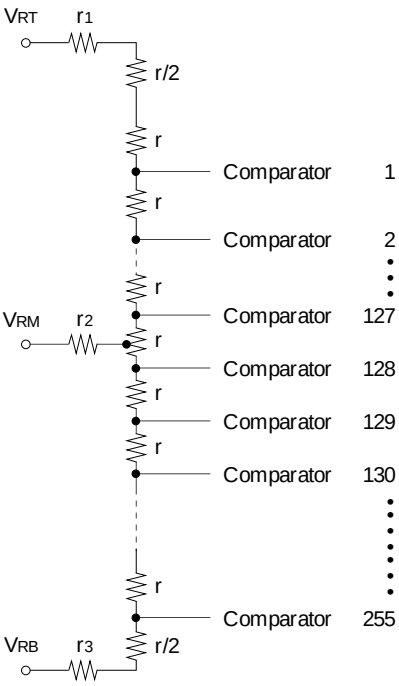
## Block Diagram



**Pin Description and I/O pin Equivalent circuit**

| Pin No | | Symbol | I/O | Standard voltage level | Equivalent circuit | Description |
|---|---|---|---|---|---|---|
| LCC | DIP | | | | | |
| 31, 33, 35, 37 | 19, 21, 23, 25 | AGND | — | 0V | | Anlog GND.<br>Used as GND for input buffers and latches of comparators.<br>Isolated from DGND or DGND 1/2. |
| 27, 28, 40, 41, 44 | 18, 26, 28 | $AV_{EE}$ | — | –5.2V | | Analog $V_{EE}$<br>–5.2V (Typ.).<br>Internally connected with $DV_{EE}$ (resistance: 4 to 6Ω).<br>Ceramic chip capacitors of at least 0.1µF should be used to connect to AGND and be placed near the pins. |
| 23 | 16 | CLK | I | ECL |  | CLK input |
| 22 | 15 | $\overline{CLK}$ | | | | Input complementary to CLK.<br>With open connection, kept at threshold voltage (–1.3V).<br>Device is operable without $\overline{CLK}$ input, but use of complementary inputs of CLK and $\overline{CLK}$ is recommended to obtain the stable high-speed operation. |
| — | 3, 12 | DGND | — | 0V | | Digital GND (Used for internal circuits and output transistors) |
| 5, 19 | — | DGND1 | — | 0V | | Digital GND (Used for internal circuits) |
| 6, 16 | — | DGND2 | — | 0V | | Digital GND (Used for output buffers) |

| Pin No | | Symbol | I/O | Standard voltage level | Equivalent circuit | Description |
|---|---|---|---|---|---|---|
| LCC | DIP | | | | | |
| 4, 20 | 2, 13 | $DV_{EE}$ | — | –5.2V | | Digital $V_{EE}$<br>Internally connected with $AV_{EE}$ (resistance: 4 to 6Ω)<br>Ceramic chip capacitors of at least 0.1µF should be used to connect to DGND and be placed near the pins. |
| 8 | 4 | D0 | O | ECL |  | LSB of data outputs.<br>External pull-down resistor is required. |
| 9 | 5 | D1 | | | | Data outputs.<br>External pull-down resistors are required. |
| 10 | 6 | D2 | | | | |
| 11 | 7 | D3 | | | | |
| 12 | 8 | D4 | | | | |
| 13 | 9 | D5 | | | | |
| 14 | 10 | D6 | | | | |
| 15 | 11 | D7 | | | | MSB of data outputs.<br>External pull-down resistor is required. |
| 3 | 1 | LINV | I | ECL |  | Input pin for D0 (LSB) to D6 output polarity inversion (see output code table).<br>With open connection, kept at "L" level. |
| 21 | 14 | MINV | I | ECL | | Input pin for D7 (MSB) output polarity inversion (see output code table).<br>With open connection, kept at "L" level. |

| Pin No. LCC | Pin No. DIP | Symbol | I/O | Standard voltage level | Equivalent circuit | Description |
|---|---|---|---|---|---|---|
| 32, 36 | 20, 24 | $V_{IN}$ | I | $V_{RT}$ to $V_{RB}$ |  | Analog input pins. These two pins must be connected externally, since they are not internally connected. See Application Note for precautions. |
| 26 | 17 | $V_{RB}$ | I | –2V |  | Reference voltage (bottom) Typically –2V A ceramic capacitor of at least 0.1µF and a tantalus capacitor of at least 10µF should be used to connect to AGND and be placed near the pins. |
| 34 | 22 | $V_{RM}$ | I | $V_{RB}/2$ | | Reference voltage mid point be used as a pin for integral linearity compensation |
| 42 | 27 | $V_{RT}$ | I | 0V | | Reference voltage (top) Typically 0V When a voltage different from AGND is applied to this pin, a ceramic capacitor of at least 0.1µF and a tantalus capacitor of at least 10µF should be used to connect to AGND and be placed near the pins. |
| 1, 2, 7, 17, 18, 24, 25, 29, 30, 38 39, 43 | | NC | — | — | | Unused pins No internal connections have been made to these pins. Connecting them to AGND or DGND on PC board is recommended. |

**Electrical Characteristics** (Ta = 25°C, $AV_{EE}$ = $DV_{EE}$ = –5.2V, $V_{RT}$ = 0V, $V_{RB}$ = –2V)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Resolution | n | | | 8 | | bits |
| DC characteristics | | | | | | |
| Integral linearity error | $E_{IL}$ | Fc = 75MSPS | | ±0.3 | ±0.5 | LSB |
| Differential linearity error | $E_{DL}$ | Fc = 75MSPS | | ±0.3 | ±0.5 | LSB |
| Analg input | | | | | | |
| Analog input capacitance | $C_{IN}$ | $V_{IN}$ = –1V + 0.07Vrms | | 17 | | pF |
| Analog input resistance | $R_{IN}$ | | | 390 | | kΩ |
| Input bias current | $I_{IN}$ | $V_{IN}$ = –1V | | | 200 | µA |
| Reference inputs | | | | | | |
| Reference resistance | $R_{REF}$ | | 75 | 110 | 155 | Ω |
| Offset voltage $V_{RT}$ | $E_{OT}$ | | 8 | 18 | 32 | mV |
| $V_{RB}$ | $E_{OB}$ | | 0 | 10 | 24 | mV |
| Digital inputs | | | | | | |
| Logic H level | $V_{IH}$ | | –1.13 | | | V |
| Logic L level | $V_{IL}$ | | | | –1.50 | V |
| Logic H current | $I_{IH}$ | Input connected to –0.8V | 0 | | 50 | µA |
| Logic L current | $I_{IL}$ | Input connected to –1.6V | –50 | | 50 | µA |
| Input capacitance | | | | 7 | | pF |
| Switching characteristics | | | | | | |
| Maximum conversion rate | Fc | Error rate $10^{-9}$ TPS*1 | 75 | | | MSPS |
| Aperture jitter | Taj | | | 10 | | ps |
| Sampling delay | Tds | | | 3.0 | | ns |
| Output delay | Tdo | | 4.0 | 6.5 | 9.0 | ns |
| H pulse width of clock | $T_{PW1}$ | | 6.6 | | | ns |
| L pulse width of clock | $T_{PW0}$ | | 6.6 | | | ns |
| Digital outputs | | | | | | |
| Logic H level | $V_{OH}$ | $R_L$ = 620Ω to $DV_{EE}$ | –1.03 | | | V |
| Logic L level | $V_{OL}$ | $R_L$ = 620Ω to $DV_{EE}$ | | | –1.62 | V |
| Output rising time | Tr | $R_L$ = 620Ω to $DV_{EE}$, 20% to 80% | | 0.9 | | ns |
| Output falling time | Tf | $R_L$ = 620Ω to $DV_{EE}$, 80% to 20% | | 2.1 | | ns |
| Dynamic characteristics | | | | | | |
| Input bandwidth | | $V_{IN}$ = 2Vp-p<br>Input frequency at –3dB | 150 | | | MHz |
| S/N ratio | | Input = 1MHz, FS<br>Clock = 75MHz | | 46 | | dB |
| | | Input = 18.75MHz, FS<br>Clock = 75MHz | | 40 | | dB |
| Error rate | | Input = 18.749MHz, FS<br>Error > 16LSB<br>Clock = 75MHz | | | $10^{-9}$ | TPS*1 |
| Differential gain error | DG | NTSC 40IRE mod. ramp,<br>Fc = 75MSPS | | 1.0 | | % |
| Differential phase error | DP | | | 0.5 | | deg |
| Power supply | | | | | | |
| Supply current | $I_{EE}$ | | –150 | –104 | | mA |
| Power consumption*2 | Pd | | | 580 | | mW |

*1 TPS: Times Per Sample

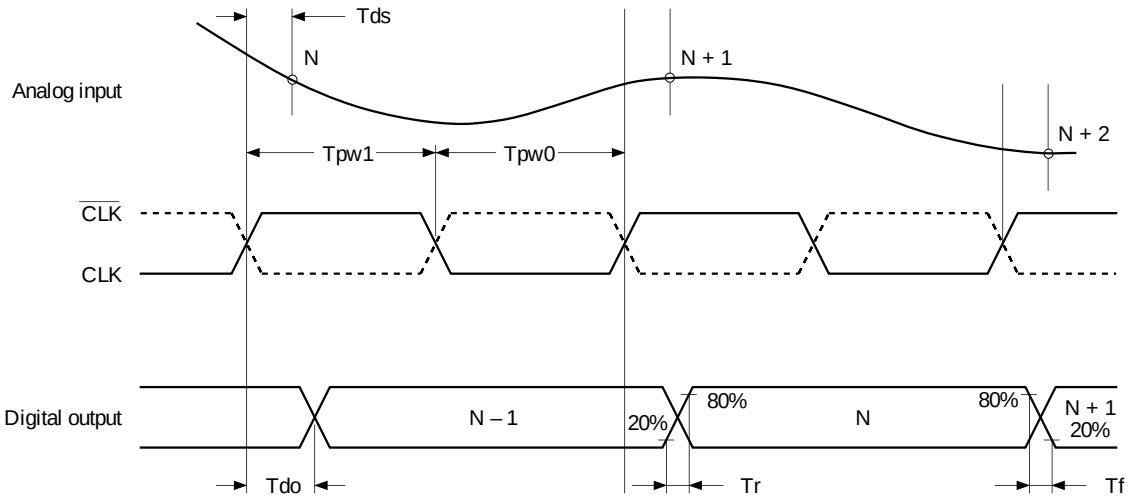
*2 $Pd = I_{EE} \cdot V_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$

**Output Code Table**

| $V_{IN}$* | Step | MINV 1<br>LINV 1 | 0<br>1 | 1<br>0 | 0<br>0 |
|---|---|---|---|---|---|
| | | D7 D0 | D7 D0 | D7 D0 | D7 D0 |
| 0V | | 0 0 0 ····· 0 0 | 1 0 0 ····· 0 0 | 0 1 1 ····· 1 1 | 1 1 1 ····· 1 1 |
| | 0 | 0 0 0 ····· 0 0 | 1 0 0 ····· 0 0 | 0 1 1 ····· 1 1 | 1 1 1 ····· 1 1 |
| | 1 | 0 0 0 ····· 0 1 | 1 0 0 ····· 0 1 | 0 1 1 ····· 1 0 | 1 1 1 ····· 1 0 |
| | | : | : | : | : |
| | | : | : | : | : |
| –1V | 127 | 0 1 1 ····· 1 1 | 1 1 1 ····· 1 1 | 0 0 0 ····· 0 0 | 1 0 0 ····· 0 0 |
| | 128 | 1 0 0 ····· 0 0 | 0 0 0 ····· 0 0 | 1 1 1 ····· 1 1 | 0 1 1 ····· 1 1 |
| | | : | : | : | : |
| | | : | : | : | : |
| | 254 | 1 1 1 ····· 1 0 | 0 1 1 ····· 1 0 | 1 0 0 ····· 0 1 | 0 0 0 ····· 0 1 |
| | 255 | 1 1 1 ····· 1 1 | 0 1 1 ····· 1 1 | 1 0 0 ····· 0 0 | 0 0 0 ····· 0 0 |
| –2V | | 1 1 1 ····· 1 1 | 0 1 1 ····· 1 1 | 1 0 0 ····· 0 0 | 0 0 0 ····· 0 0 |

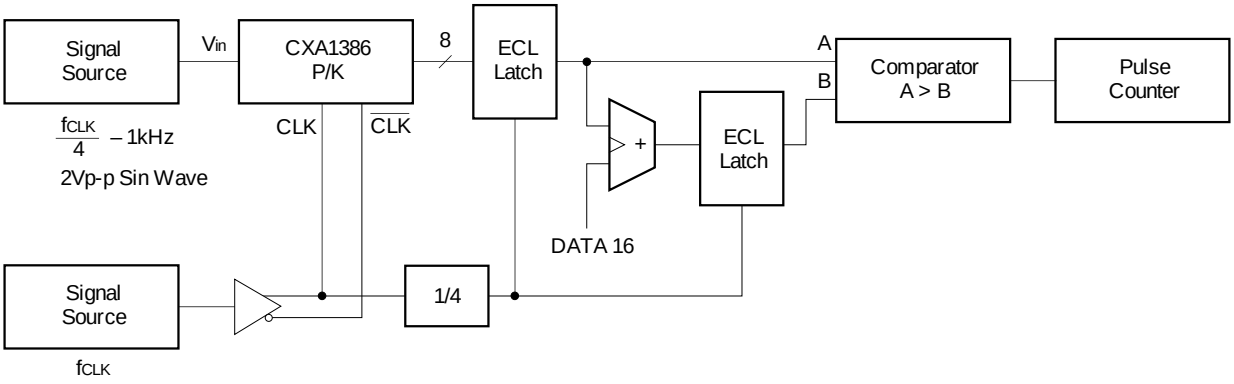
* $V_{RT}$ = 0V, $V_{RB}$ = –2V

**Timing diagram**

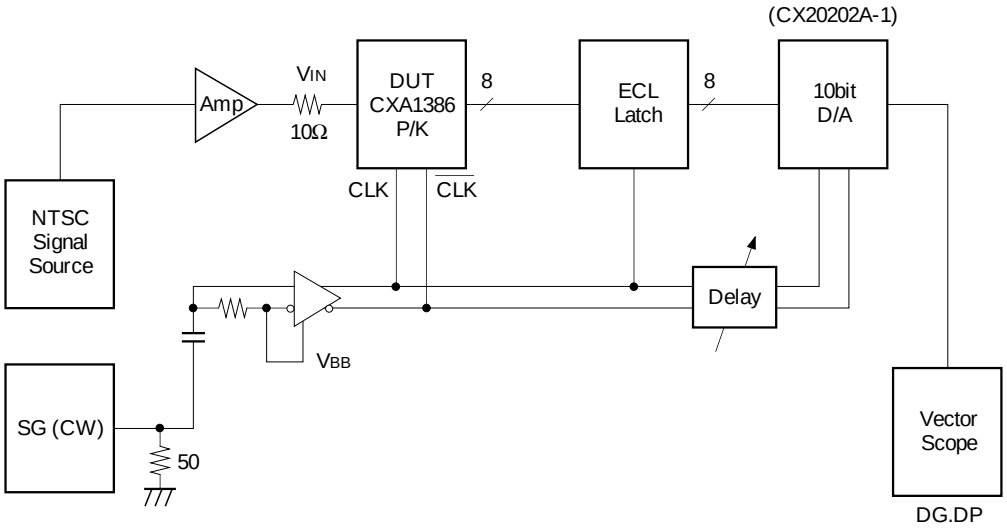


## Electrical Characteristics Test Circuit

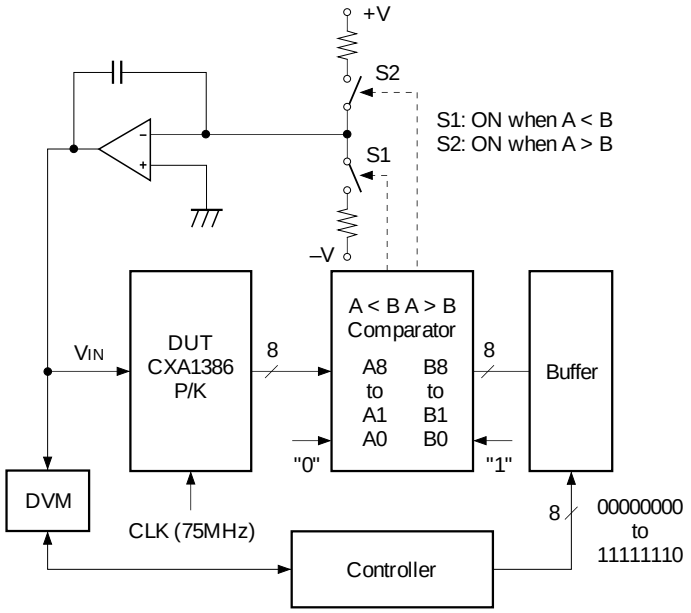
### Maximum conversion rate test circuit



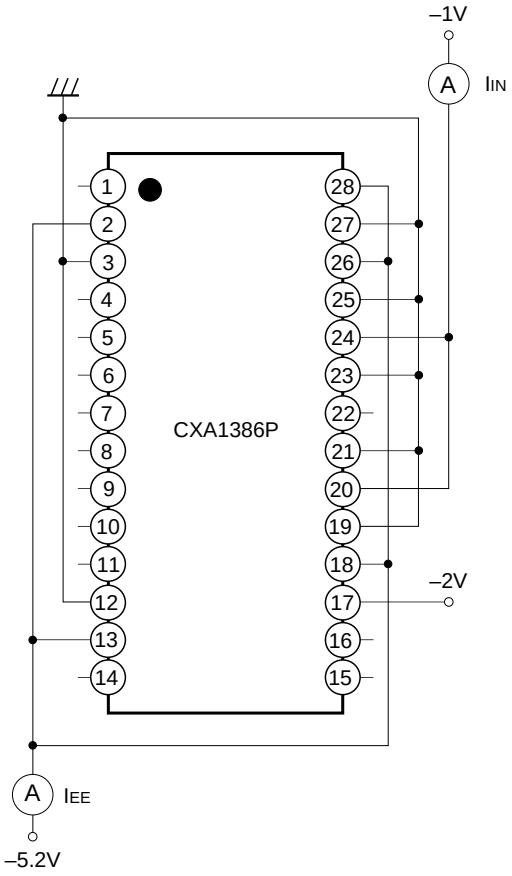

### Differential gain error test circuit
### Differential phase error test circuit

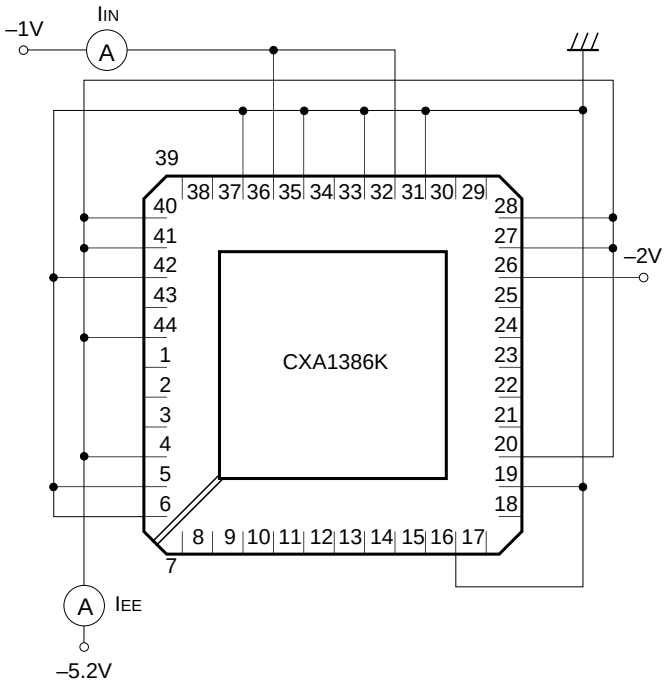



### Integral linearity error test circuit
### Differential linearity error test circuit

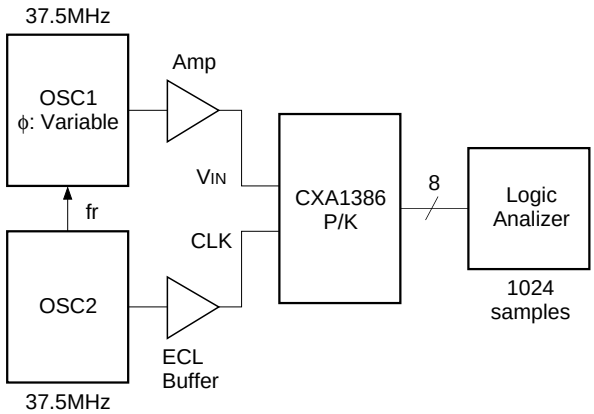


**Power Supply Current Test Circuit**
**Analog input bias current test circuit**

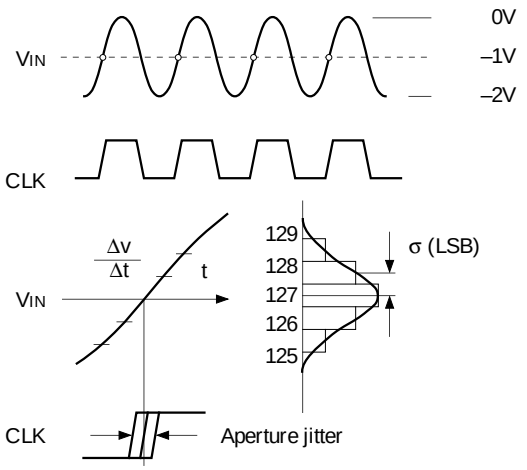



**Sampling delay test circuit**
**Aperture jitter test circuit**




**Aperture jitter test method**




Aperture jitter is defined as follows:

$$Taj = \sigma / \frac{\Delta \upsilon}{\Delta t} = \sigma / \left( \frac{256}{2} \times 2\pi f \right),$$

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

**8bit 75MSPS ADC and DAC Evaluation Board**

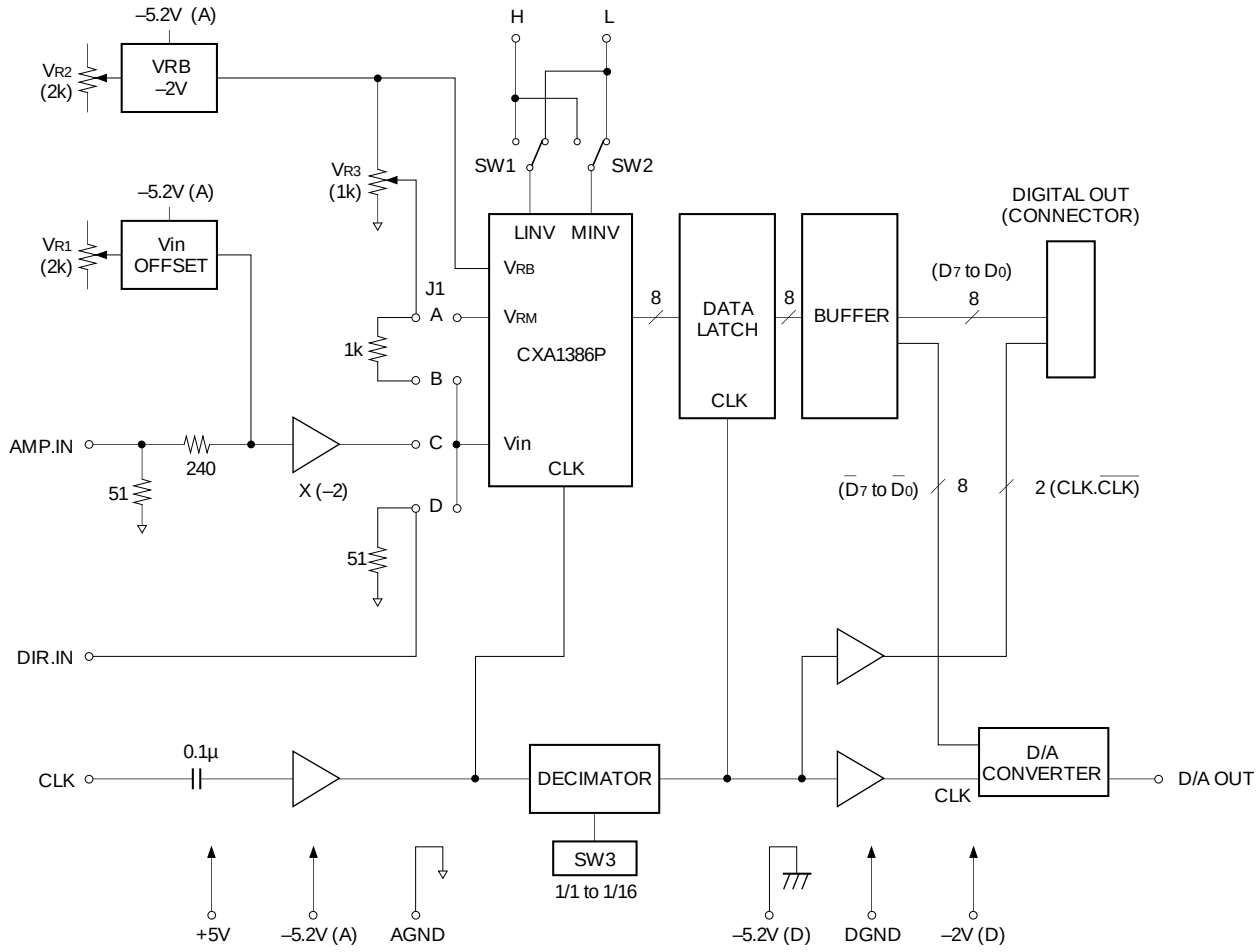
It is necessary to equip "the CXA1396D/P EVALUATION BOARD WITH DAC" with "A1396D – A1386P ADAPTER" in order to evaluate CXA1386P.

In addition to indispensable features such as the reference voltage generator, this tool equips two sets of analog inputs (the direct input and the buffer amplifier input), the input voltage offset generator, the clock decimator, the output data latches, the 10-bit high-speed DAC, and the 20-pin cable connector for digital outputs. This evaluation board provides full performance of the CXA1386P and it is designed to facilitate evaluation.

**Features**

Resolution: 8bits
Maximum conversion rate: 75MSPS
Supply voltage: +5.0V, –5.2V, –2.0V
Two analog inputs (Direct input, buffer amplifier input)
Clock level converter: Sine wave to ECL level signal
Reference voltage adjustment circuit for the A/D converter
Built-in clock frequency decimation circuit: (1/1 to 1/16)

**Fig. 1. Block Diagram**



**Supply Current**

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| –5.2V | | 0.85 | 1.0 | A |
| +5.0V | | 15 | 30 | mA |
| –2.0V | | 0.45 | 0.6 | A |

(**Note:** Supply current –2.0V is the value when Rn10, Rn11 and Rn12 are not mounted.)

**Analog Input (DIR. IN, AMP. IN)**

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input voltage (DIR. IN) | –2.0 | | 0 | V |
| (AMP. IN)*1 | –0.5 | | +0.5 | V |
| Input impedance | | 50 | | Ω |

(*1: Adjustable by VR1)

**Clock Input (CLK)**

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input voltage (Peak to Peak) | | 2.0 | | Vp-p |
| Input impedance | | 50 | | Ω |

**Digital Output (D0 to D7)**

ECL 10KH level

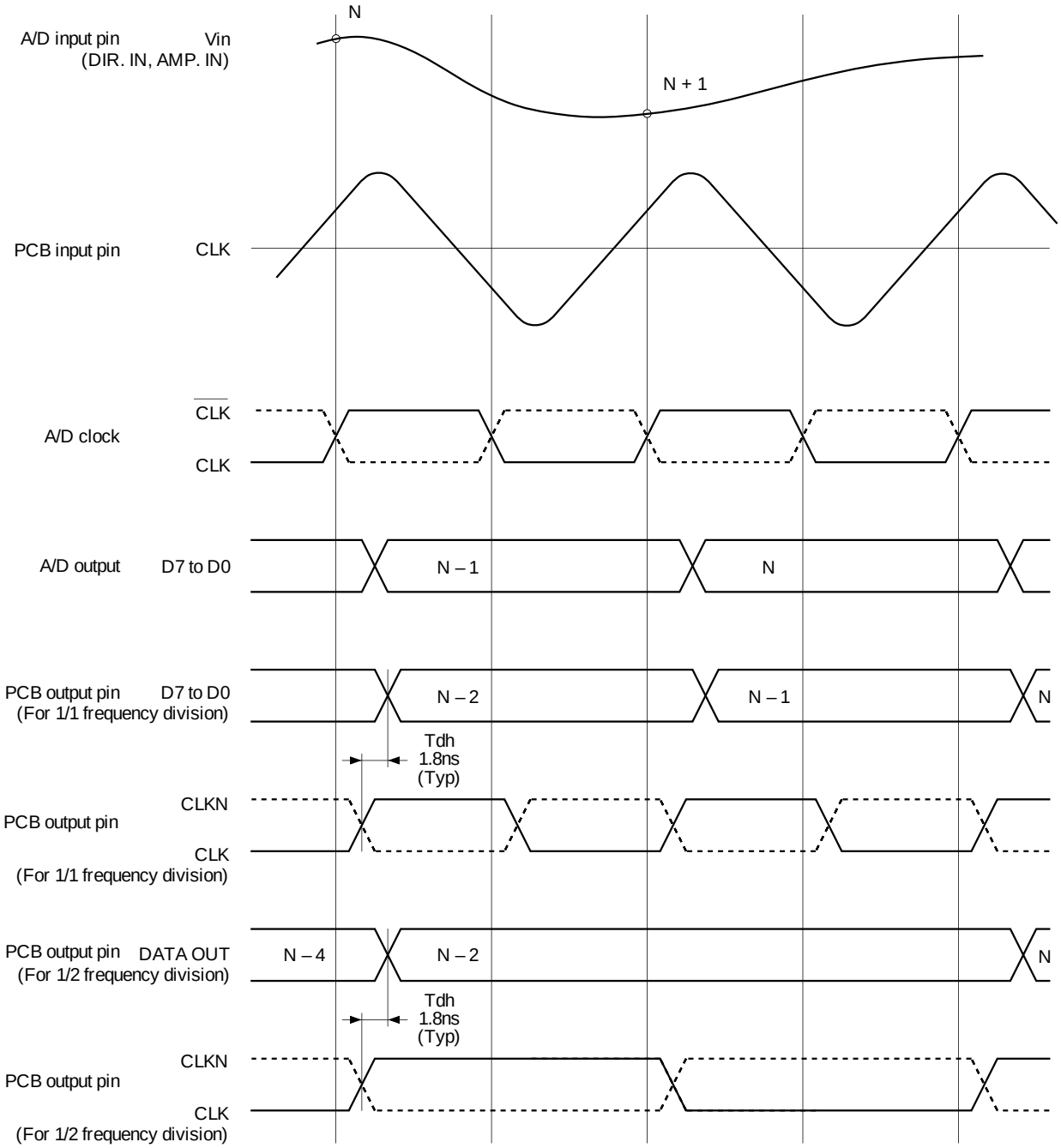
**Clock Output**

ECL 10KH level, complementary output

**Output Code Table**

| | MINV<br>LINV | 0<br>0 | 0<br>1 | 1<br>0 | 1<br>1 |
|---|---|---|---|---|---|
| $V_{IN}$ | 0V | 1 1 1 ····· 1 1 | 1 0 0 ····· 0 0 | 0 1 1 ····· 1 1 | 0 0 0 ····· 0 0 |
| | : | 1 1 1 ····· 1 0 | 1 0 0 ····· 0 1 | 0 1 1 ····· 1 0 | 0 0 0 ····· 0 1 |
| | : | : | : | : | : |
| | : | : | : | : | : |
| | : | 1 0 0 ····· 0 0 | 1 1 1 ····· 1 1 | 0 0 0 ····· 0 0 | 0 1 1 ····· 1 1 |
| | : | 0 1 1 ····· 1 1 | 0 0 0 ····· 0 0 | 1 1 1 ····· 1 1 | 1 0 0 ····· 0 0 |
| | : | : | : | : | : |
| | : | : | : | : | : |
| | : | 0 0 0 ····· 0 1 | 0 1 1 ····· 1 0 | 1 0 0 ····· 0 1 | 1 1 1 ····· 1 0 |
| | –2V | 0 0 0 ····· 0 0 | 0 1 1 ····· 1 1 | 1 0 0 ····· 0 0 | 1 1 1 ····· 1 1 |

**Fig. 2. Timing Chart**




**Adjustment Methods and Notes on Operation**

1) Vin Offset (VR1)
   The volume to adjust the signal range (0V center assumed) with the A/D converter input range when a waveform is input through AMP. IN.

2) A/D Full Scale (VR2)
   The volume to adjust A/D converter VRB voltage.

3) Linearity (VR3)
   The volume to adjust VRM (linearity) voltage.

4) D/A Full Scale (VR4)
The volume to adjust D/A output full scale (–1V)

5) J1 (input selection)
A: Shorts to adjust VRM voltage.
B: Shorts to supply DC voltage to Vin.
C: Shorts to select AMP.IN input.
D: Shorts to select DIR. IN input.

[Jumper Poisition at shipment]

J1
A ○○
B ○○
C ○○
D ○○

6) SW1
The switch for LINV High/Low

7) SW2
The switch for MINV High/Low

8) SW3 (Decimation)
The switch to select clock frequency decimation.
Switch position: decimation ratio
0: 1/1
1: 1/2
2: 1/4
3: 1/8
4: 1/16

9) SW4 (D/A INV)
The switch for D/A converter output inversion.

10) Rn10, Rn11 and Rn12 are not mounted at shipment. They are not required during evaluation.

11) Waveform probe pins P5 and P8 through P28 are devised to facilitate GND connection in order to reduce the distortion. As shown in the diagram below, the distance between the probe point and the GND is 300 mils, and there is ϕ1.2mm throughhole at each. The signal and GND locations are suit for a Tektronix GND tip (part number 013-1185-00).

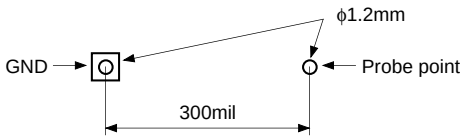



**Fig. 3.**

12) D/A converter (IC13) input data (waveform probe pins P21 through P28) are the complementary signals of the decimated A/D converter outputs. Those are inverted again in the D/A converter so that the direction of reproduced waveform can agree with the A/D input signal converter.

13) The part number of the digital output connector is KEL 8830E-020-170S. A corresponding connector and cable assembly is JUNKOSHA KB0020MCG50BI.

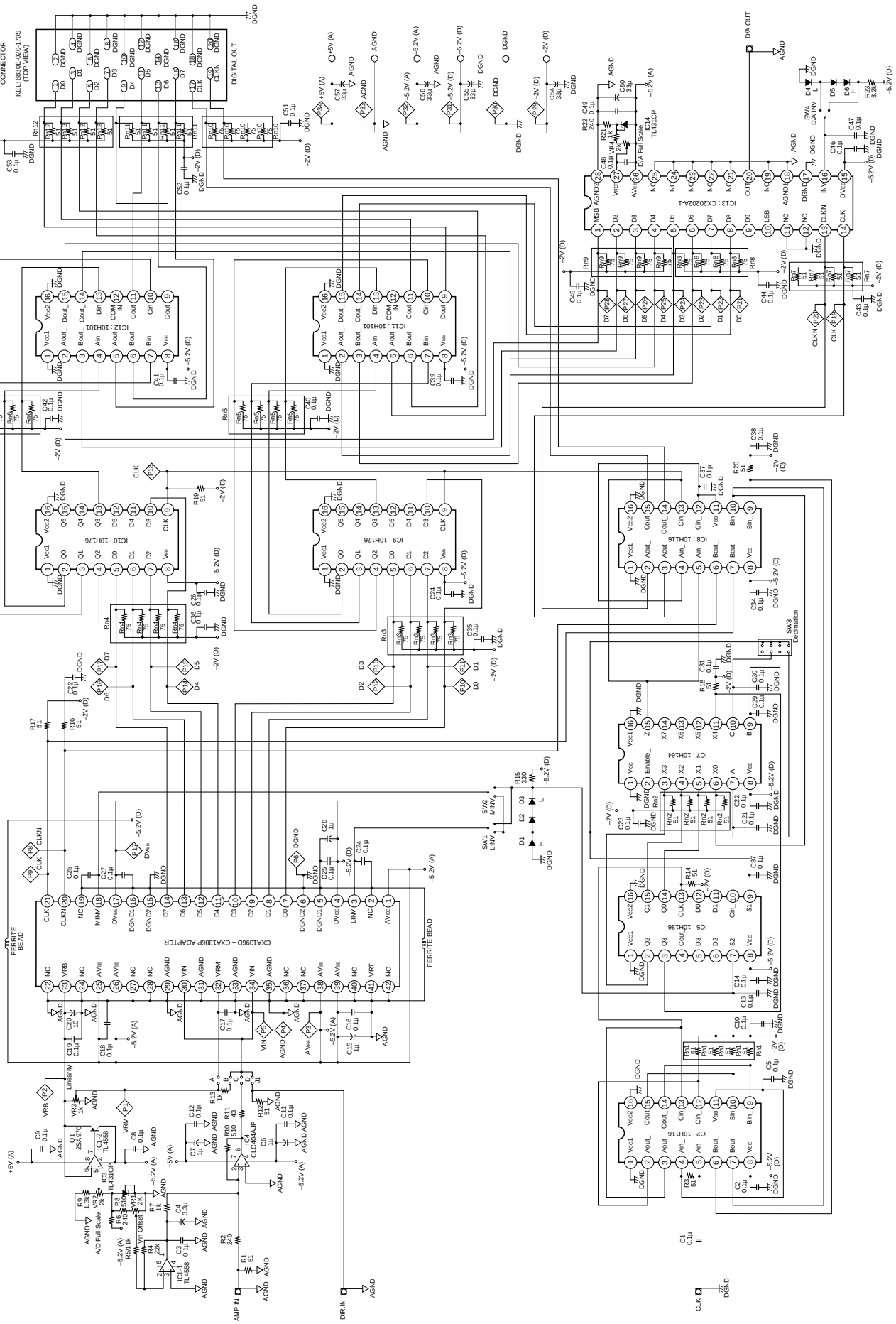


**Fig. 4. PCB Circuit Schematic**

## Characteristics Graphs

**Fig 5. CXA1386P SNR vs. Input Frequency**

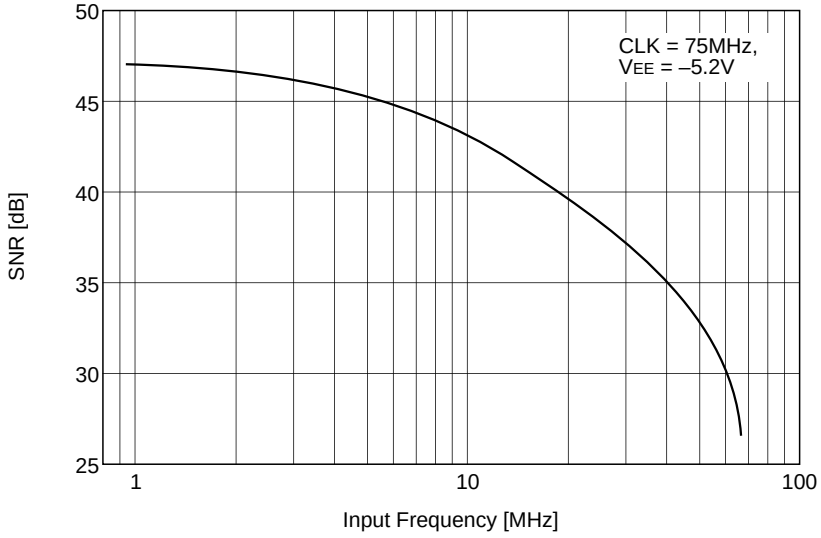



**Fig. 6. CXA1386P Effective Bits vs. Input Frequency**

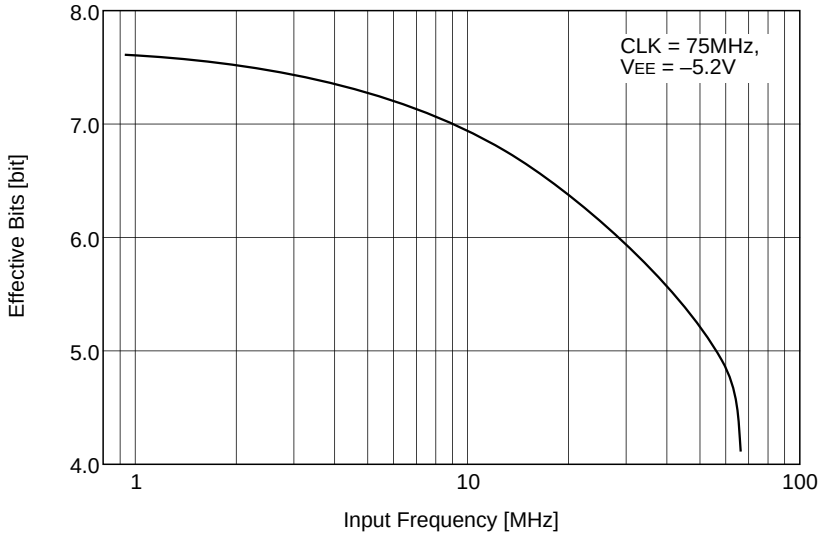
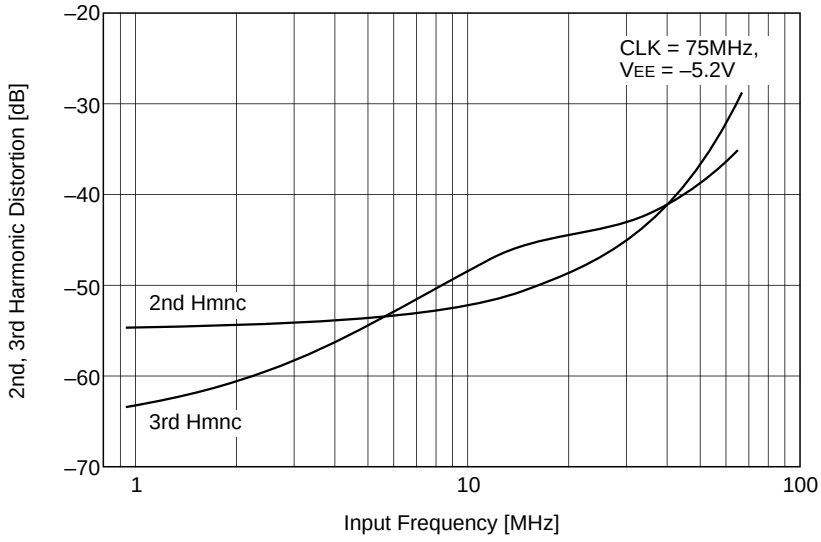
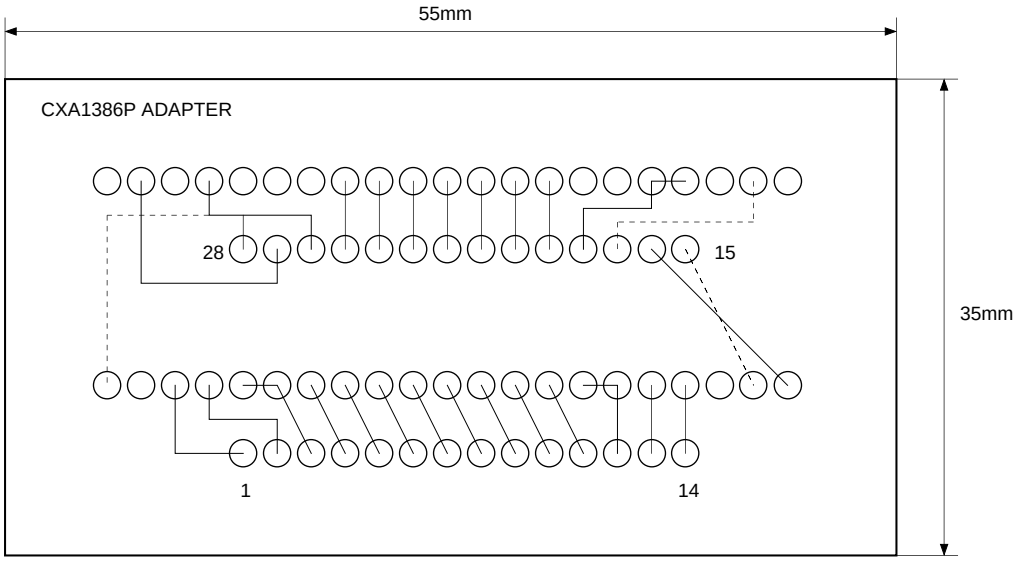



**Fig. 7. CXA1386P 2nd, 3rd Harmonic Distortion vs. Input Frequency**

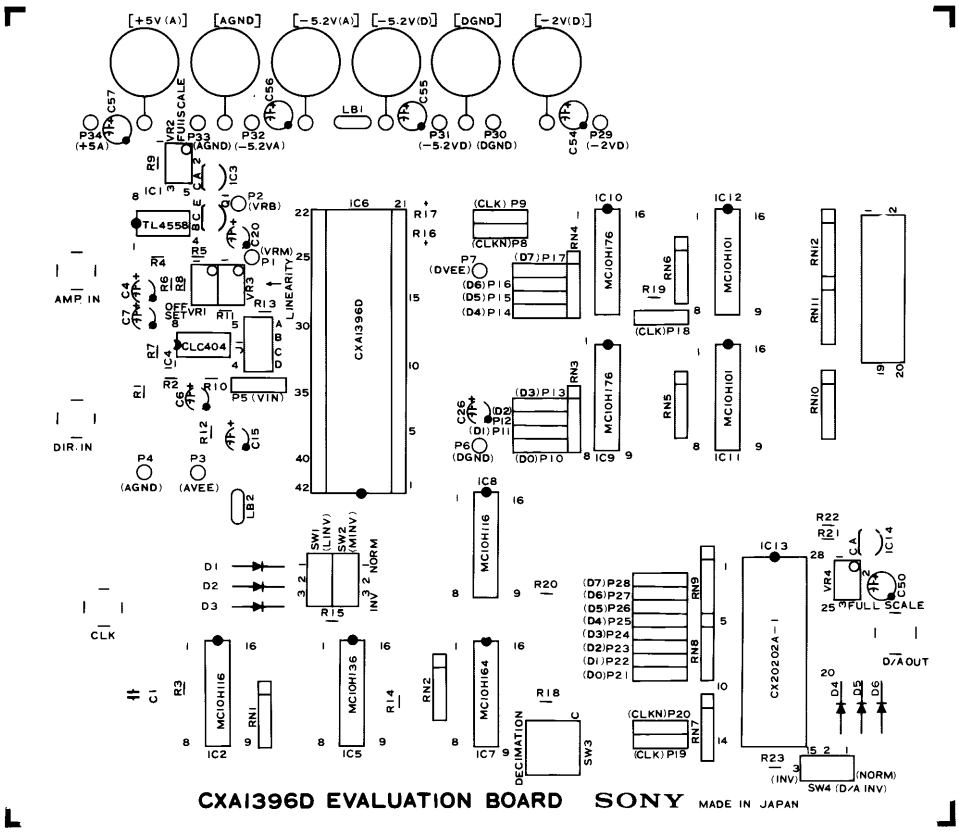


**CXA1396D – CXA1386P ADAPTER** (SCALE = 2/1)

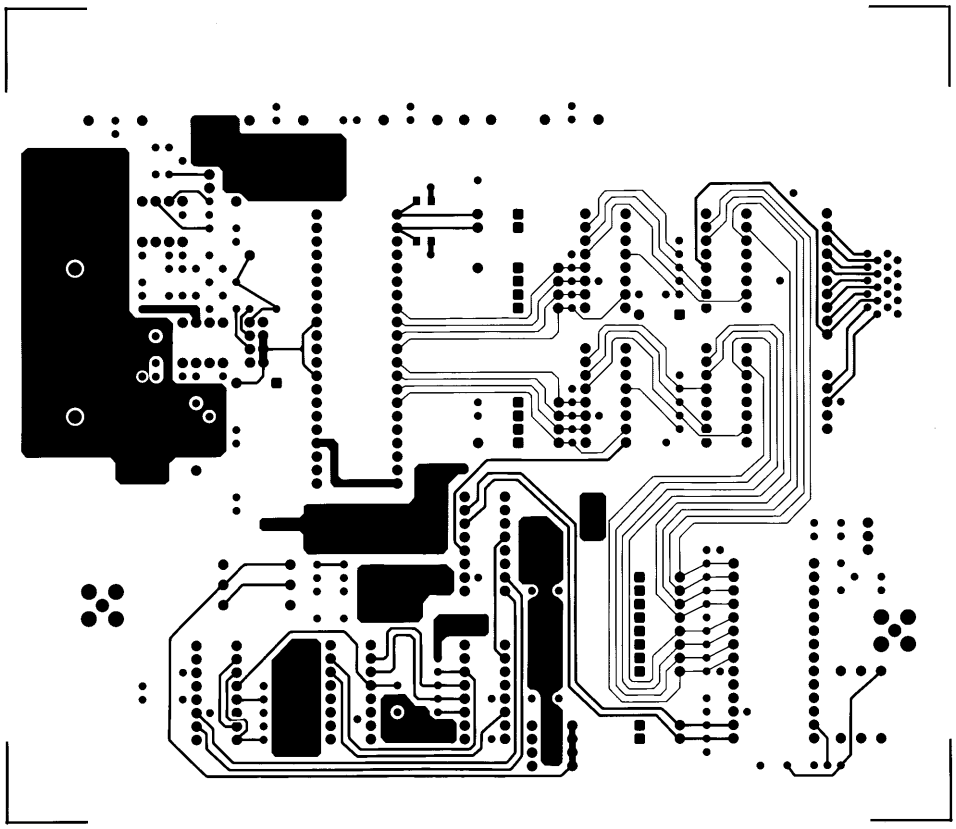



TOP VIEW

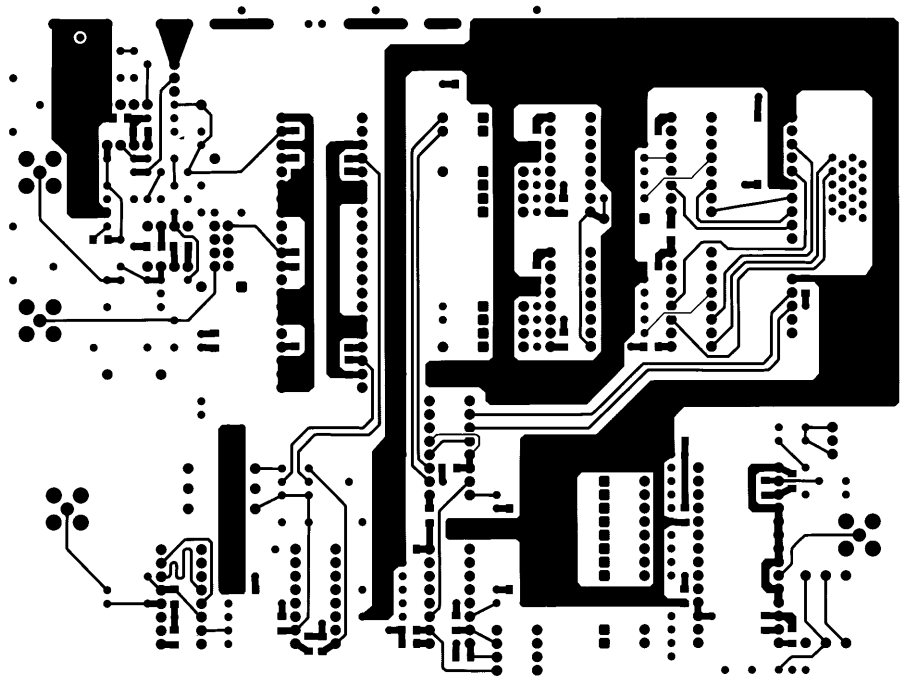
## Parts Layout



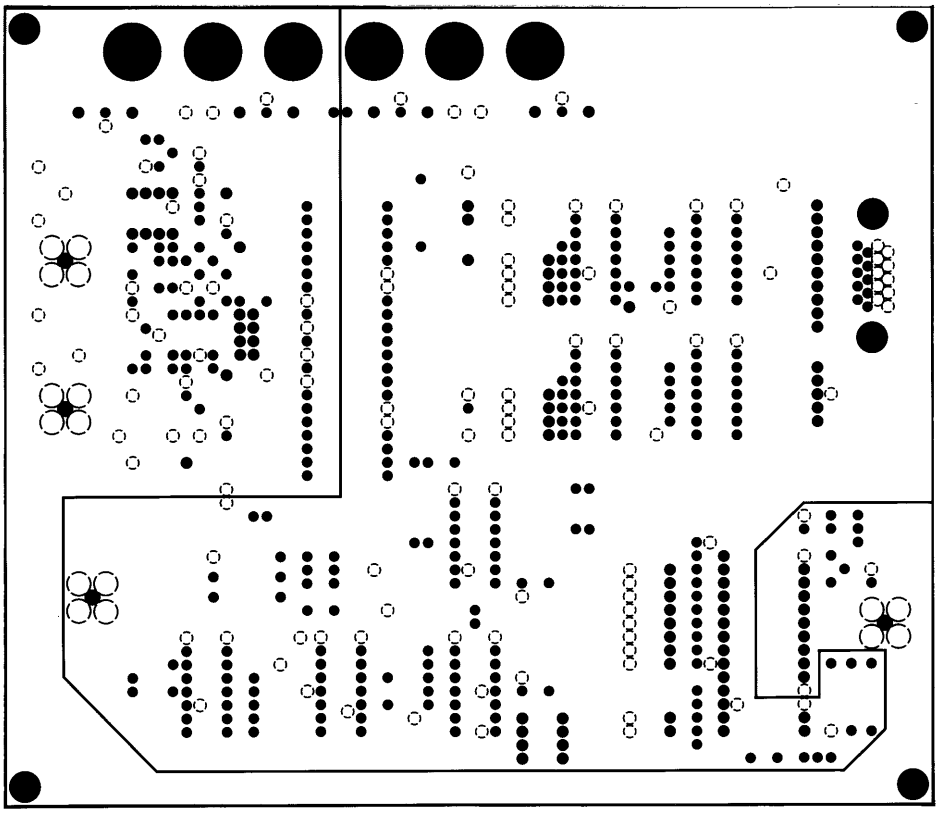
**Printed Pattern**



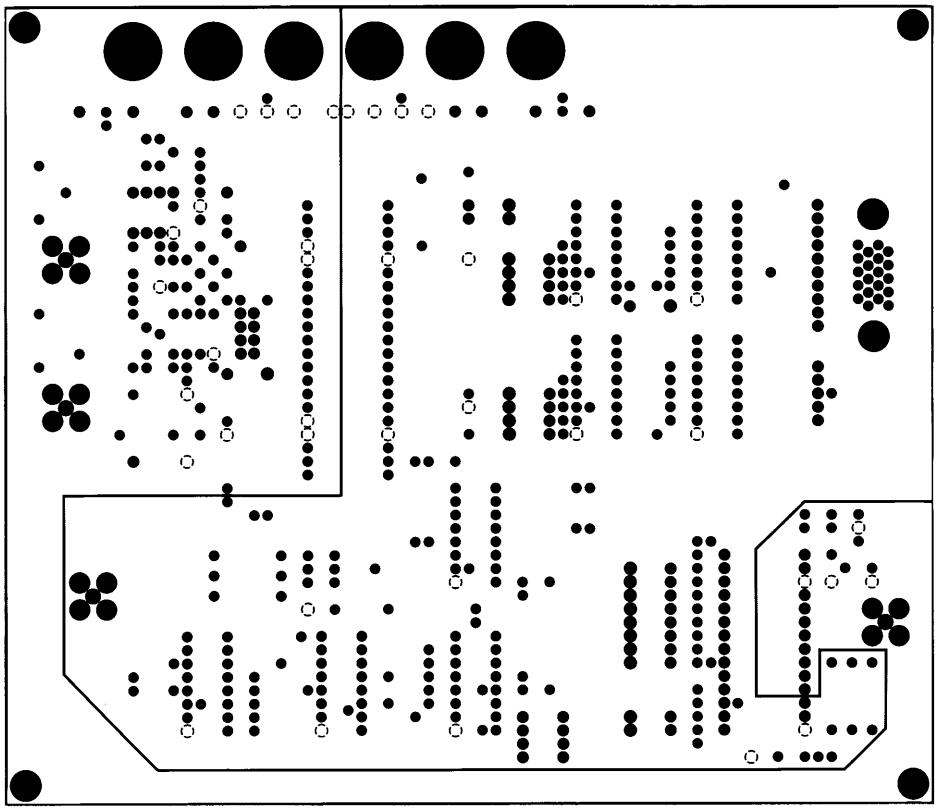
**1st layer Component plane (Top View)**



**4th layer Solder plane (Top view)**



**2nd layer GND plane (Top View)**

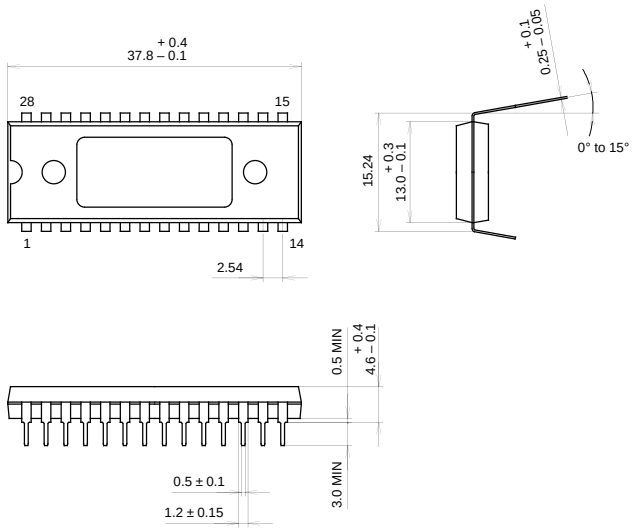


**3rd layer Power supply plane (Top View)**

**Package Outline** Unit: mm

CXA1386P

28PIN DIP (PLASTIC) 600mil



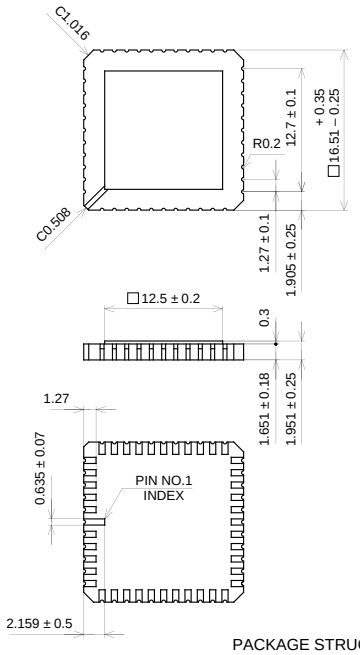

| | |
|---|---|
| SONY CODE | DIP-28P-03 |
| EIAJ CODE | *DIP028-P-0600-C |
| JEDEC CODE | |

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | COPPER |
| PACKAGE WEIGHT | 4.2g |

CXA1386K

44PIN LCC (CERAMIC) 1.8g




| | |
|---|---|
| SONY CODE | LCC-44C-01 |
| EIAJ CODE | *QFN044-C-S650-A |
| JEDEC CODE | |

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | CERAMIC |
| LEAD TREATMENT | GOLD PLATING |
| LEAD MATERIAL | |
| PACKAGE WEIGHT | 1.8g |