CMOS 4-BIT MICROCONTROLLER

TMP47C460AN
TMP47C460AF

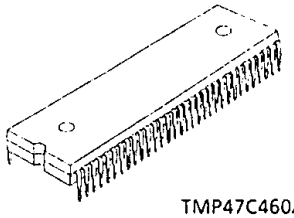
The 47C460A is a high speed and high performance 4-bit single chip microcomputer based on the TLCS-47 CMOS series with expansion input and output ports.

PART No.	ROM	RAM	PACKAGE	PIGGY BACK
TMP47C460AN	4096 × 8-bit	256 × 4-bit	SDIP64	TMP47C960AE
TMP47C460AF			QFP67	-

FEATURES

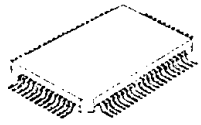
- ◆4-Bit single chip microcomputer
- ◆Instruction execution time : 1.9μs (at 4.2MHz)
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available
- ◆I/O port (58 pins)
  - Input 2 ports 5 pins
  - Output 4 ports 16 pins
  - I/O 10 ports 37 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Serial Interface with 4-bit buffer
  External/internal clock, and leading/trailing edge shift mode
- ◆High current outputs
  LED direct drive capability (typ.20mA × 8bits)
- ◆Hold function
  Battery/Capacitor back-up
- ◆Real Time Emulator : BM4721A + BM4724A

SDIP64



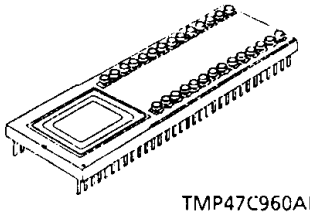
TMP47C460AN

QFP67



TMP47C460AF

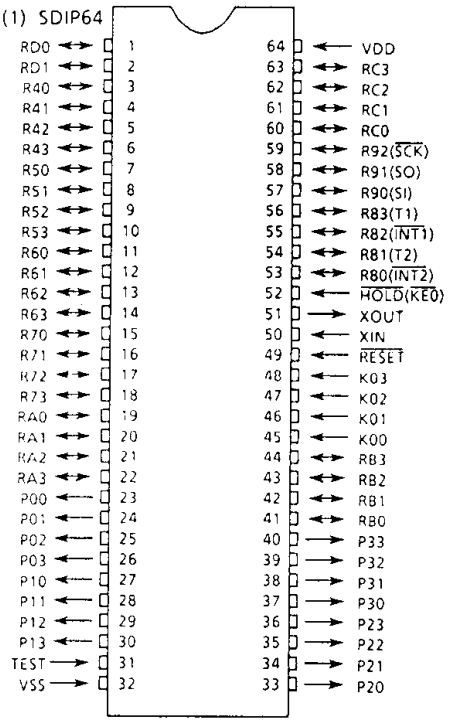
SDIC64



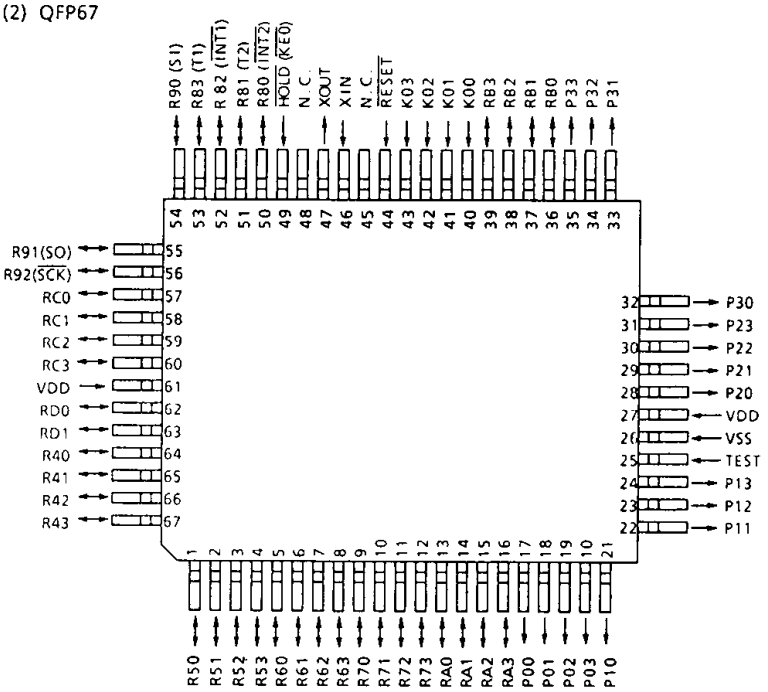
TMP47C960AE

PIN ASSIGNMENTS (TOP VIEW)

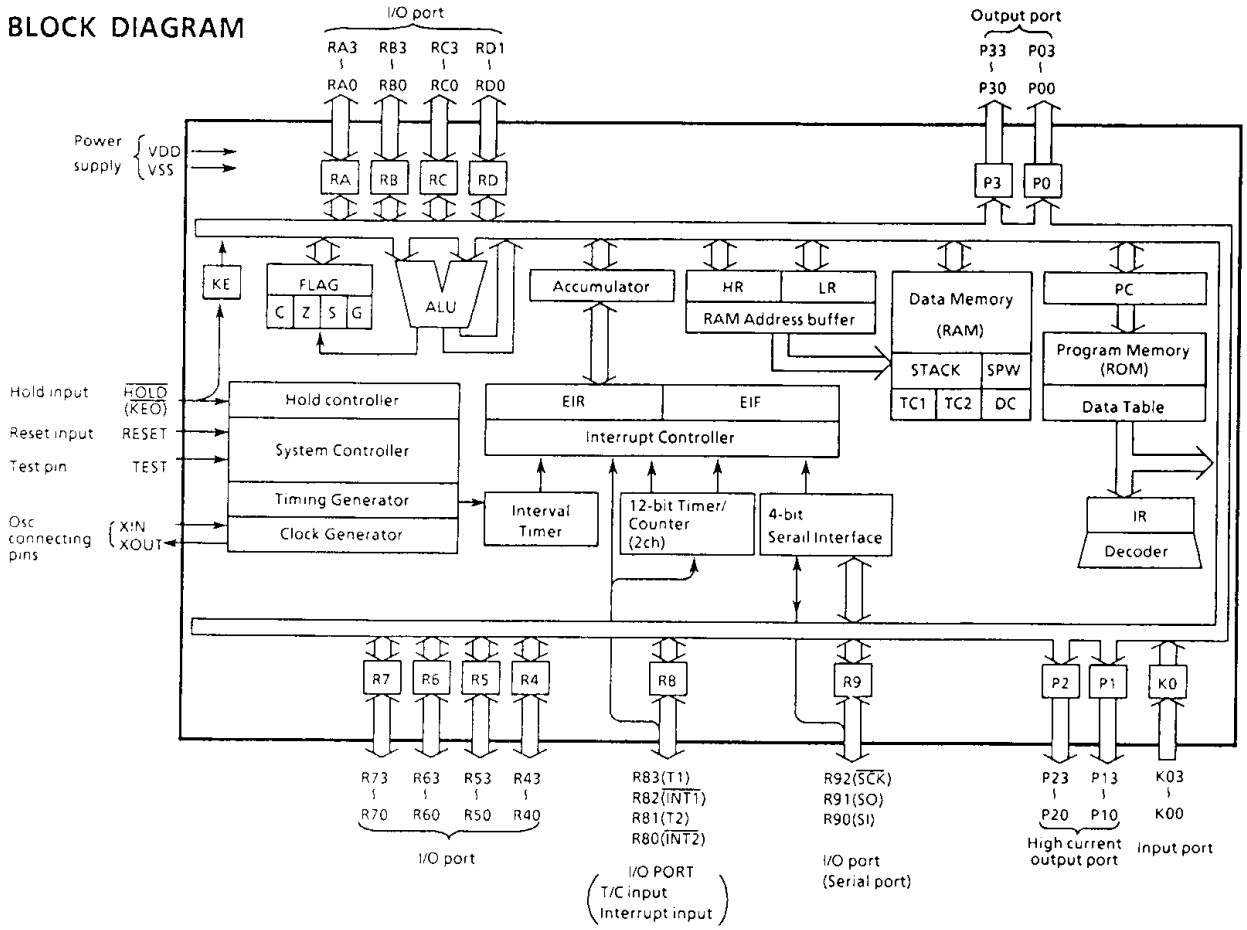
(1) SDIP64



(2) QFP67



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
P03 - P00	Output	4-bit output port with latch.	
P13 - P10 P23 - P20	Output	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
P33 - P30	Output	4-bit output port with latch	
R43 - R40 R53 - R50 R63 - R60 R73 - R70	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1". Every bit data is possible to be set, cleared and tested by the manipulation of the L-register indirect addressing.	
RA3 - RA0 RB3 - RB0 RC3 - RC0 RD1 - RD0	I/O	4-bit I/O port with latch (RD port has only 2-bit). When used as input port, the latch must be set to "1".	
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 (INT1)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KEO}$)	Input (Input)	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level	
VDD	Power supply	+ 5V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

The 47C460A functions similarly to the 47C400A except the expansion I/O ports, the technical data sheets for the 47C400A shall also be referred to.

1. I/O PORTS

The 47C460A has 15 I/O ports (57 pins) each as folows :

①	K0	; 4-bit input
②	P0, P3	; 4-bit output
③	P1, P2	; 4-bit output
④	R4, R5, R6, R7	; 4-bit input/output
⑤	R8	; 4-bit input/output (shared by external interrupt request input and timer/counter input)
⑥	R9	; 3-bit input/output (shared by serial port)
⑦	RA, RB, RC	; 4-bit input/output
⑧	RD	; 2-bit input/output
⑨	KE	; 1-bit sense input (shared by hold request / release signal input)

This section describes ports of ②, ⑦ and ⑧ which are changed from the 47C400A.
Table 1.1 lists the port address assignments and the I/O instructions that can access the port.

(1) Ports P0 (P03 - P00) and P3 (P33 - P30)

The 4-bit output port with latch. The latch is initialized to "0" during reset.
When an input instruction is executed, the latch data are read as the port P3 but the port P0.

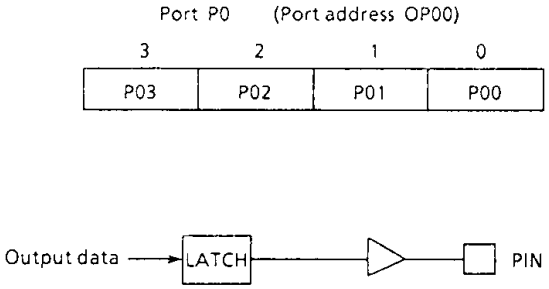


Figure1-1. Port P0

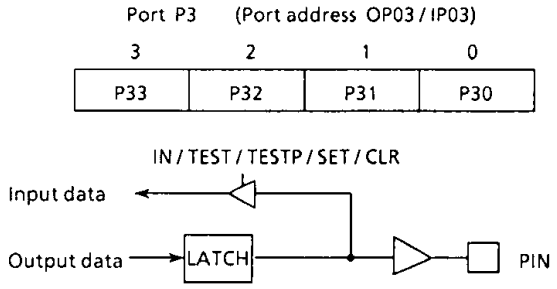


Figure1-2. Port P3

(2) Ports RA (RA3 - RA0), RB (RB3 - RB0), RC (RC3 - RC0), RD (RD1, RD0)

The 4-bit I/O ports with latch (port RD has only 2-bit). The latch is initialized to "1" during reset.
When used as input port, the latch should be set to "1". The 47C460A has no RD2 and RD3 pins.
However, when an input instruction is executed, the data "1" are read as RD2 and RD3 pins.

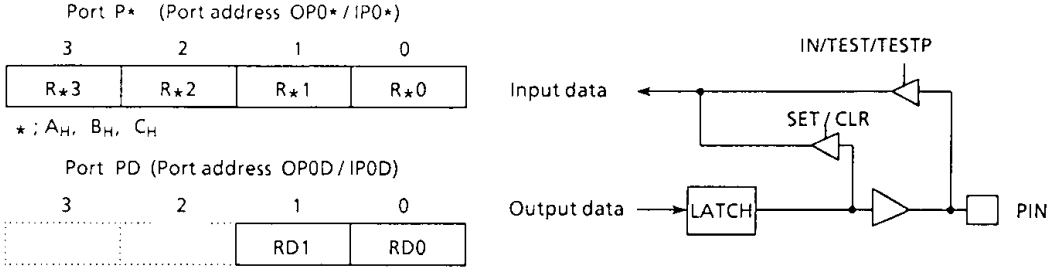


Figure1-3. Ports RA through RD

Port address ($_{**}$)	Port		Input/Output instruction						
	Input (IP_{**})	Output (OP_{**})	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	P0 output port	○	○	○	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note 2)	○	○	–
02	P2 output latch	P2 output port	○	○	○	○ (Note 2)	○	○	–
03	P3 output latch	P3 output port	○	○	○	–	○	○	–
04	R4 input port	R4 output port	○	○	○	–	○	○	–
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RA input port	RA output port	○	○	○	–	○	○	–
0B	RB input port	RB output port	○	○	○	–	○	○	–
0C	RC input port	RC output port	○	○	○	–	○	○	–
0D	RD input port	RD output port	○	○	○	–	○	○	–
0E	SIO Hold status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	——	–	–	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval Timer interrupt	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note 1. "——" means the reserved state. Unavailable for the user programs.

Note 2. The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Note 3. As concerns the port address "00", IN and TEST instructions operate port K0, and OUT instruction operates port P0.

Table 1-1. Port Address Assignments and Available I/O Instructions

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.5 to 7	V
Input Voltage	V_{IN}		− 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin	− 0.5 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1 and P2	30	mA
	I_{OUT2}	Ports P0, P3, R4-R9, RA-RD	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1 and P2	120	mA
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal operating mode	4.5	6.0	V
			in the HOLD operating mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	4.2	MHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the HOLD operating mode.

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	–	–	± 2	μA
	I_{IN2}	Open drain output ports					
Input Low Current	I_{IL}	Push-pull output ports	V_{DD} = 5.5V, V_{IN} = 0.4V	–	–	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Open drain output ports	V_{DD} = 5.5V, V_{OUT} = 5.5V	–	–	2	μA
Output High Voltage	V_{OH}	Push-pull output ports	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	–	–	V
Output Low Voltage	V_{OL2}	Except XOUT and ports P1 and P2 ports	V_{DD} = 4.5V, I_{OL} = 1.6mA	–	–	0.4	V
Output Low Current	I_{OL1}	Ports P1 and P2	V_{DD} = 4.5V, V_{OL} = 1.0V	–	20	–	mA
Supply Current (in the Normal operating mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	–	3	6	mA
Supply Current (in the HOLD operating mode)	I_{DDH}		V_{DD} = 5.5V	–	0.5	10	μA

Note 1. *Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.*

Note 2. *Input Current I_{IN1} : The current through resistor is not included, when the pull-up/pull-down resistor is contained.*

Note 3. *Supply Current : V_{IN} = 5.3V / 0.2V*

The port K0 with the pull-up/pull-down resistor is open. The voltage applied to the port R4-R9 is within the range V_{IL} or V_{IH}.

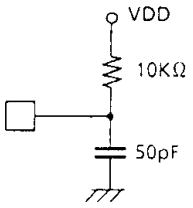
A. C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = V_{HH} = 4.5 to 5.5V, T_{opr} = − 30 to 70°C)

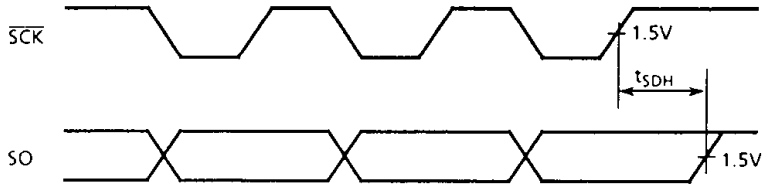
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	−	20	μs
High level Clock pulse Width	t_{WCH}	For external clock operation	80	−	−	ns
Low level Clock pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		$0.5t_{cy}$ − 300	−	−	ns

Note. Shift data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = V_{HH} = 4.5 to 5.5V, T_{opr} = − 30 to 70°C)

(1) 4MHz

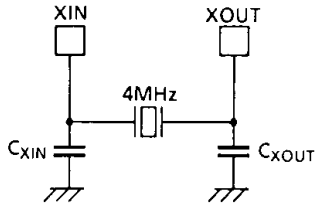
Ceramic Resonator

CSA 4.00MG (MURATA) C_{XIN} = C_{XOUT} = 30pF

KBR - 4 .00MS (KYOCERA) C_{XIN} = C_{XOUT} = 30pF

Crystal Oscillator

204B - 6F 4.0000 (TOYOCOM) C_{XIN} = C_{XOUT} = 20pF

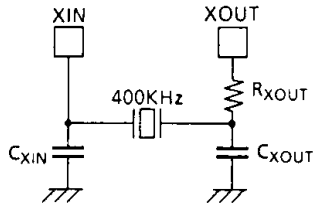


(2) 400KHz

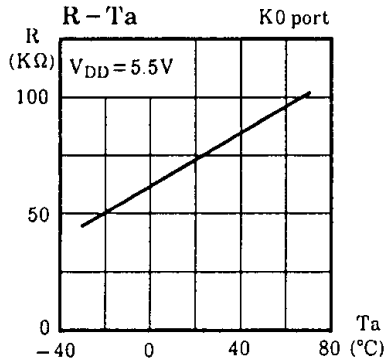
Ceramic Resonator

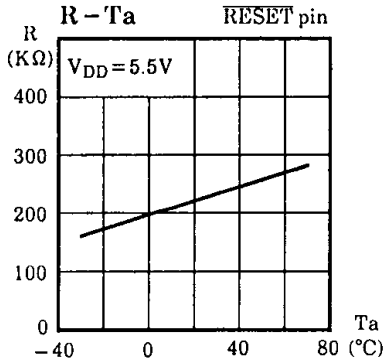
CSB400B (MURATA) C_{XIN} = C_{XOUT} = 220pF, R_{XOUT} = 6.8KΩ

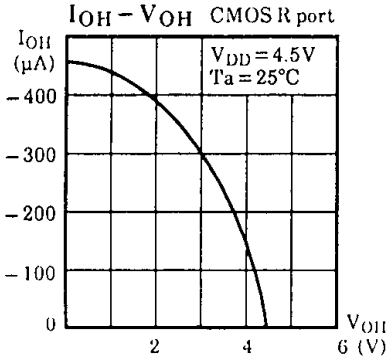
KBR-400B (KYOCERA) C_{XIN} = C_{XOUT} = 100pF, R_{XOUT} = 10KΩ

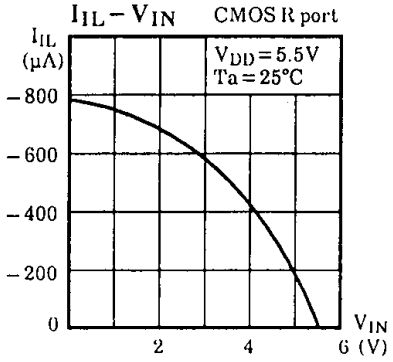


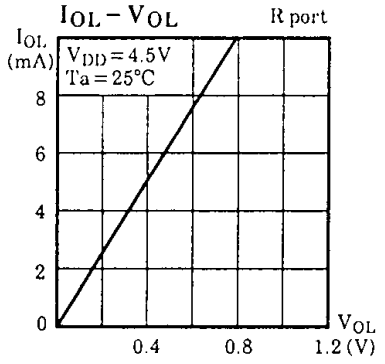
TYPICAL CHARACTERISTICS

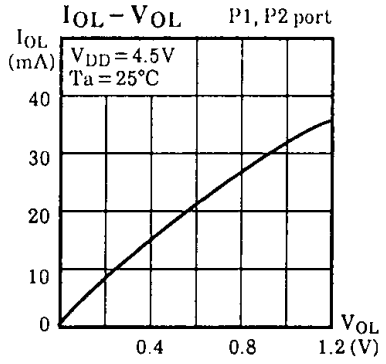


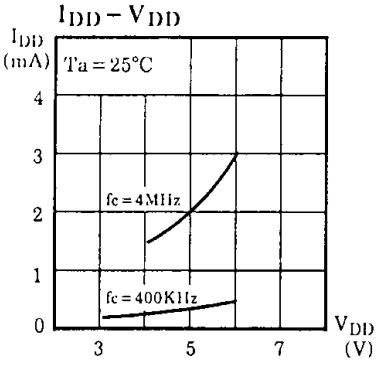


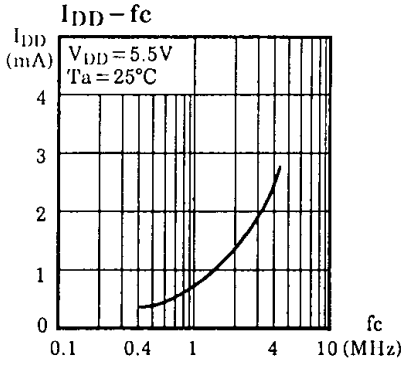












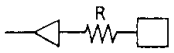
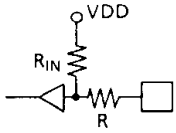
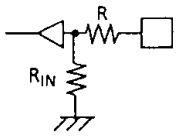
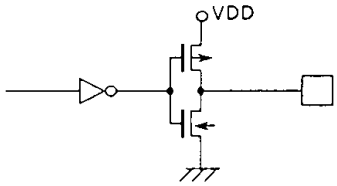
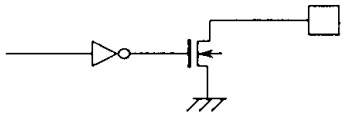
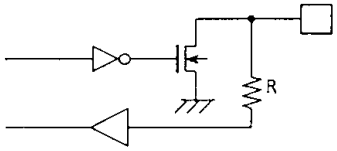
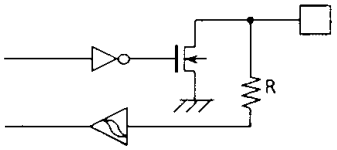
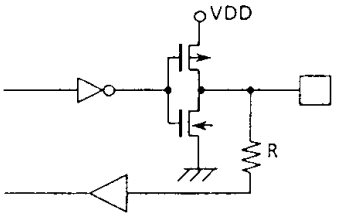
INPUT/OUTPUT CIRCUITRIES

(1) Control pins

Input /Output circuitries of the 47C460A control pins are similar to that of the 47C400A.

(2) I/O ports

I/O ports are shown below any one of the circuitries can be chosen by a code (IA-IC) as a mask option.

Port	I/O	INPUT / OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input	IA:  IB:  IC: 	Pull-up / Pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
P0 P3	Output		Push-pull output Initial "Low"
P1 P2	Output		Sink open drain output Initial "Hi-Z" High current I_{OL} = 20mA (typ.)
R4 R5 R6 R7	I/O		Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.)
R8 R9	I/O		Sink open drain output Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)
RA RB RC RD	I/O		Push-pull output Initial "High" R = 1KΩ (typ.)

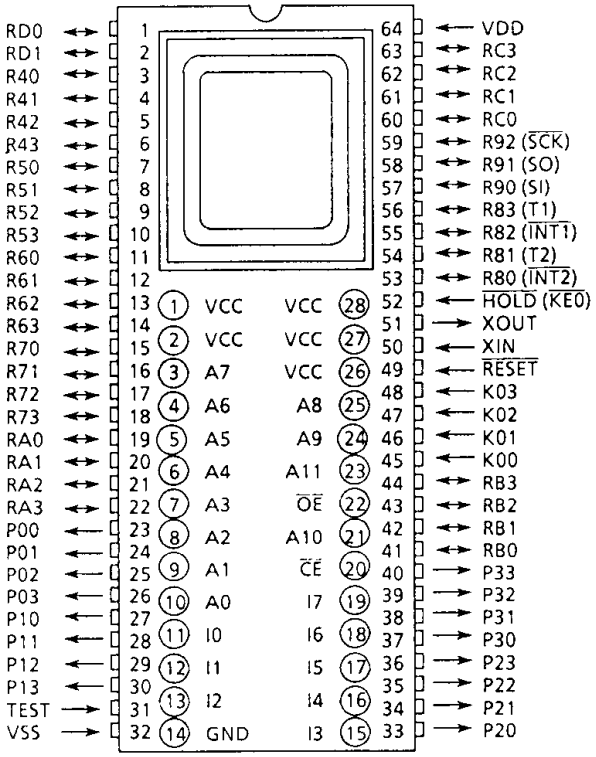
CMOS 4-BIT MICROCONTROLLER

TMP47C960AE

The 47C960A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C460A application systems (programs).
The 47C960A is pin compatible with the 47C460A which are mask-programed ROM devices. The 47C960A can be used as evaluator chip for 4746 (TLCS-47 NMOS series).

PIN ASSIGNMENT (TOP VIEW)

SDIC64



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 ~ A0	Output	Program memory address output
I7 ~ I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
OE		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 4.5 to 6.0V C_L = 100pF Topr = – 30 to 70°C	–	–	150	ns
Data Setup Time	t_{IS}		150	–	–	ns
Data Hold Time	t_{IH}		50	–	–	ns

NOTES FOR USE

(1) Program memory

The program area is as shown in Figure 1.

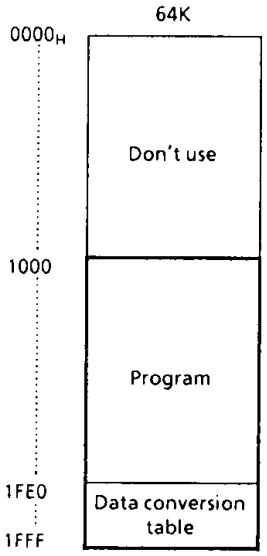


Figure 1. Program area

(2) When the 47C960A is used as the 4746 system evaluator chip, caution is required concerning the following points.

① The memory hold function cannot be supported.

② Use with the VDD and $\overline{HOLD}$ pins connected.

③ The following electrical characteristics differ:

a. Input high voltages (VIH1, VIH2)

b. Input low voltages (VIL1, VIL2)

c. Power supply current

(3) I/O ports

Input/Output circuitries of I/O ports in the 47C960A are similar to the code IA of the 47C460A.

When this chip is used as evaluator with other I/O code, it is nacessary to provide the external resistors.

Figure 2. I/O code and external circuitry