IR3Y30M/M1

CCD Signal Processors for B/W CCD Cameras

DESCRIPTION

The IR3Y30M/M1 are bipolar single-chip signal processing ICs with built-in low-pass filter and delay line for B/W video cameras. They realize both downsizing and cost reduction of the finished set.

FEATURES

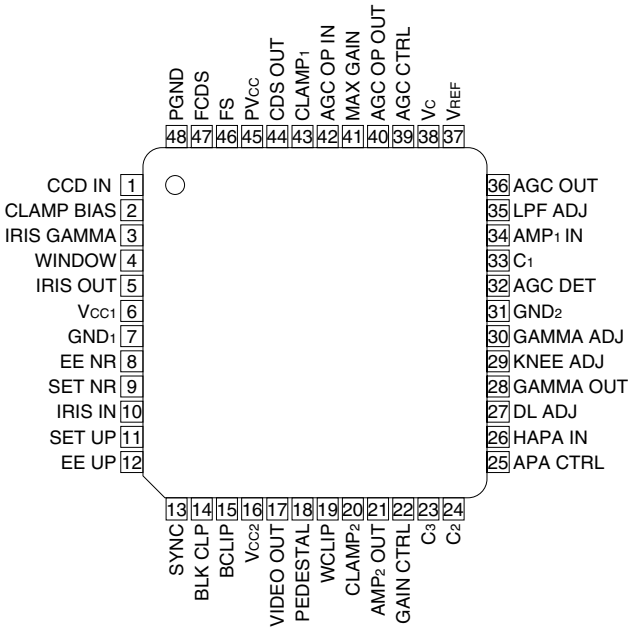
- Low power consumption : 265 mW (TYP.)
- Wide AGC range : –3 to +29 dB
- High speed sample-and-hold circuits : pulse width 15 ns (MIN.)
- Signal processing from CCD output to 75 Ω video output is possible
- Built-in low-pass filter
- Built-in comparator for electronic exposure control
- Built-in aperture circuit and delay line
- Single +5 V power supply
- Packages
  - IR3Y30M : 48-pin QFP (QFP048-P-1010)
  - IR3Y30M1 : 48-pin QFP (QFP048-P-0707) 0.5 mm pin-pitch

COMPARISON TABLE

	IR3Y30M	IR3Y30M1
Package	48-pin QFP (QFP048-P-1010)	48-pin QFP (QFP048-P-0707)
Power consumption	725 mW	560 mW
P_D derating ratio	5.8 mW/˚C	4.5 mW/˚C
Operating temperature	–30 to +75 ˚C	–30 to +70 ˚C

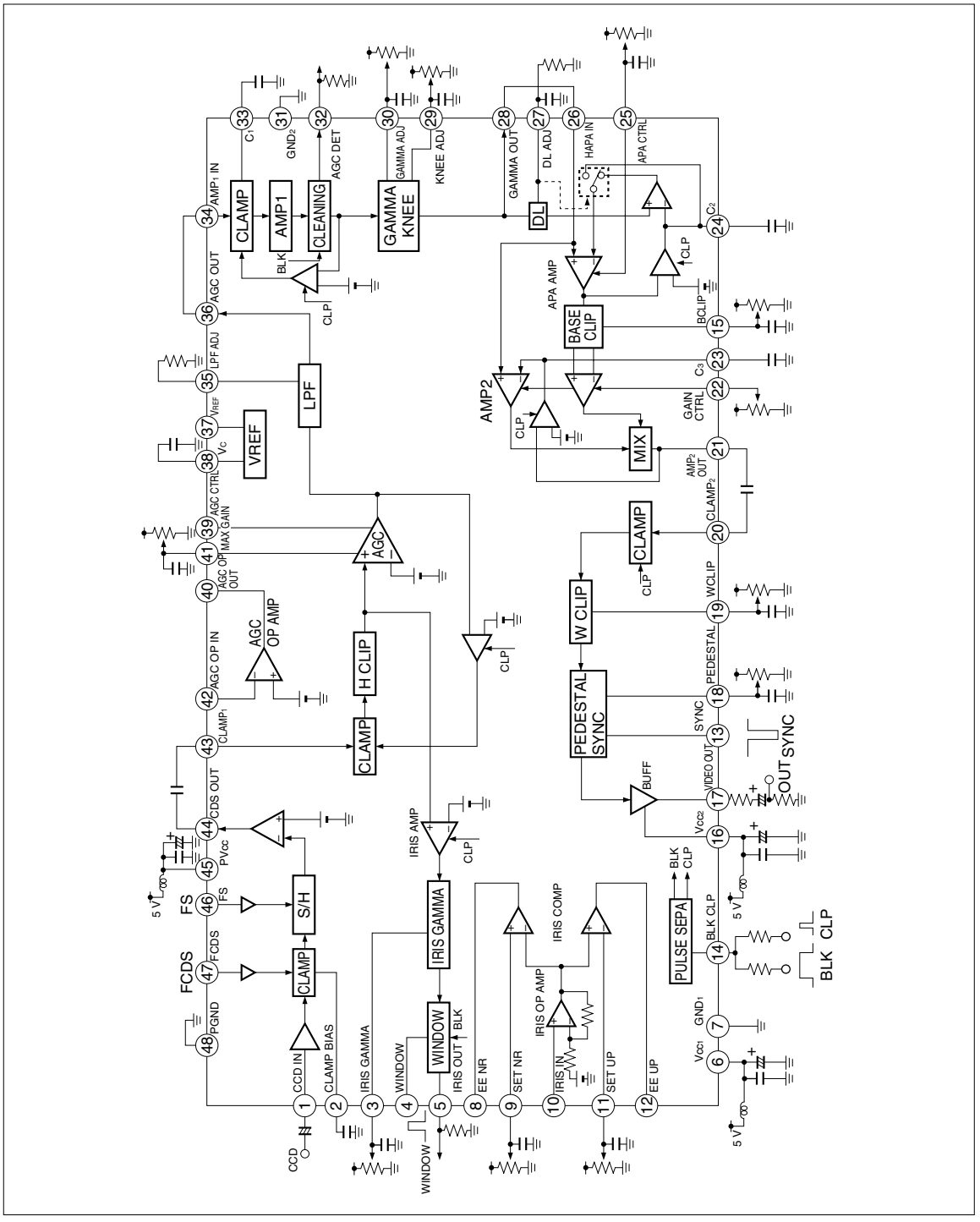
PIN CONNECTIONS

48-PIN QFP TOP VIEW

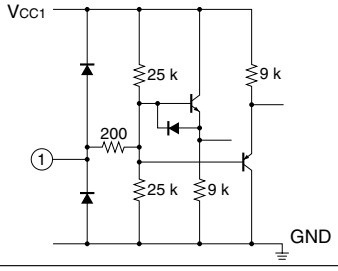
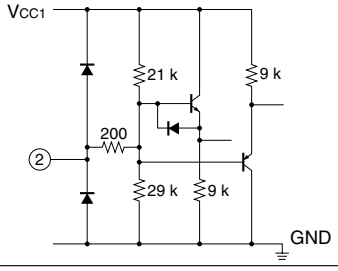
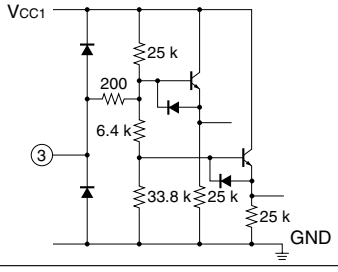
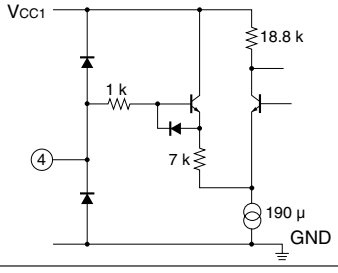
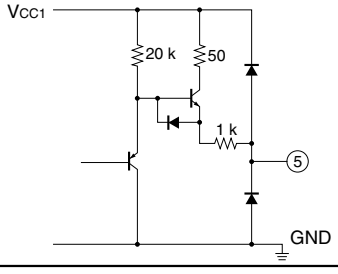


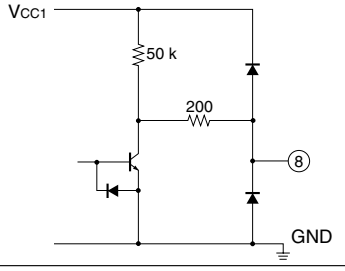
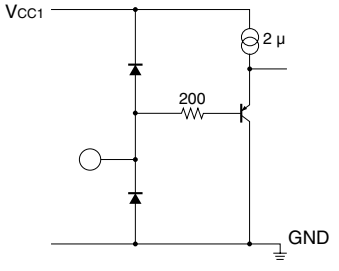
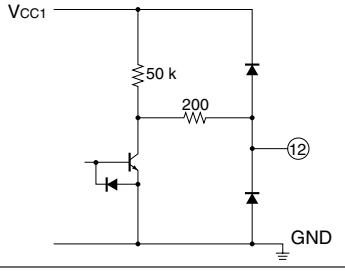
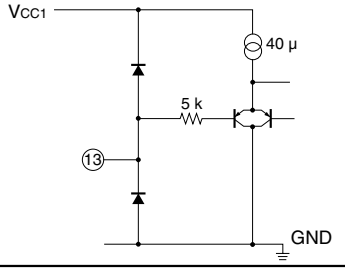
(QFP048-P-1010)
(QFP048-P-0707)

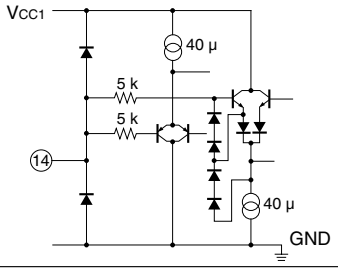
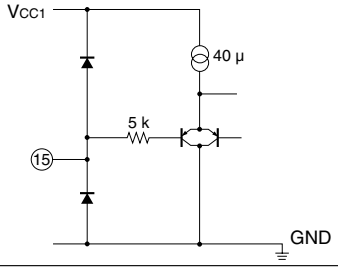
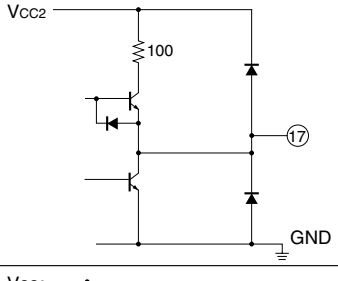
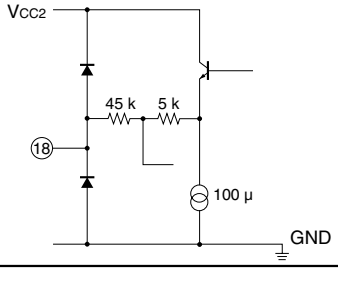
BLOCK DIAGRAM

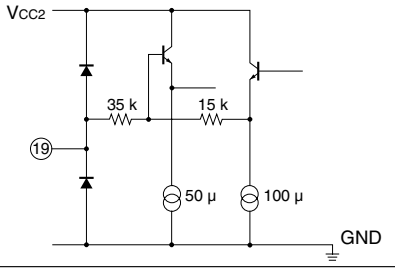
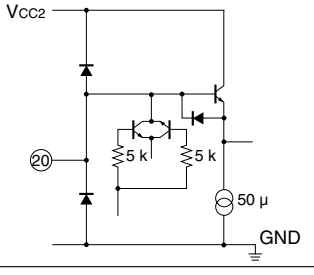
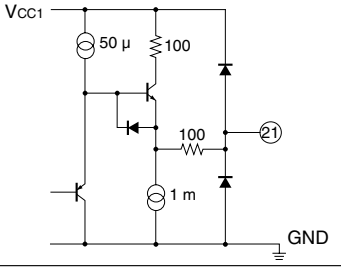
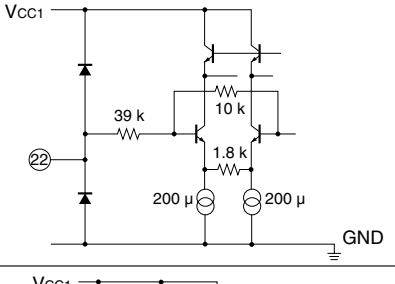
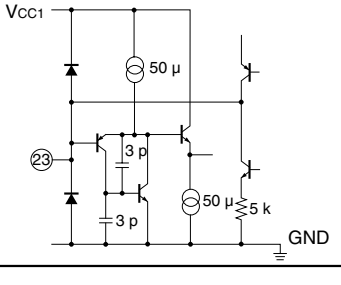


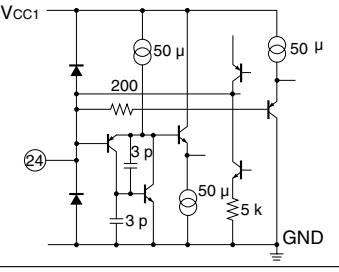
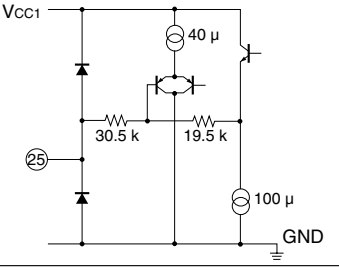
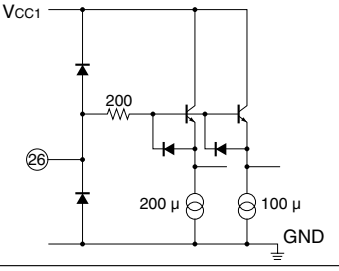
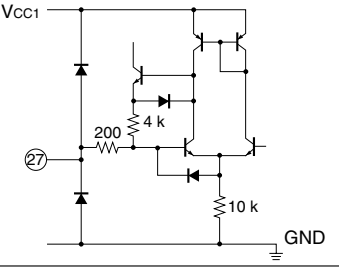
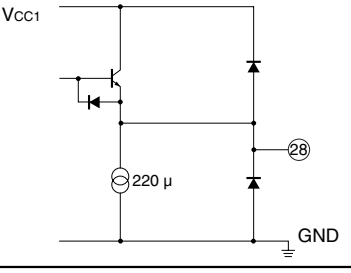
PIN DESCRIPTION

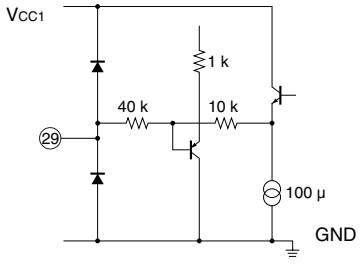
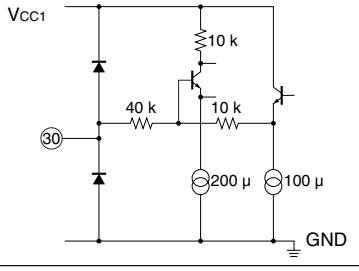
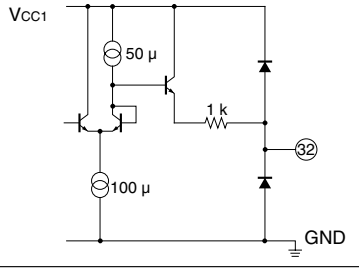
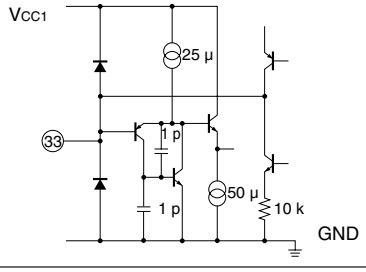
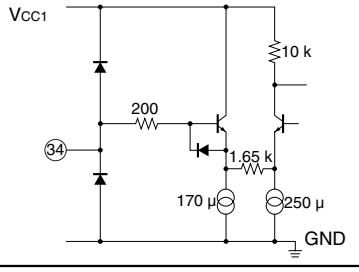
PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
1	CCDIN	2.5 V		Input for the signal from CCD area sensor. 2.5 V bias applied internally.
2	CLAMP BIAS	2.9 V		Feed through level of the input signal is clamped to this pin voltage. 2.9 V bias applied internally. Connect capacitor between this pin and GND.
3	IRIS GAMMA	3.1 V		Gamma adjustment of the exposure circuit. This pin is preset to 3.1 V, and gamma becomes 0.45 at open.
4	WINDOW			Window pulse input for the exposure circuit. Outputs the signal while "H".
5	IRIS OUT	2.3 V		Output for the exposure signal. Connect a resistor between this pin and GND.

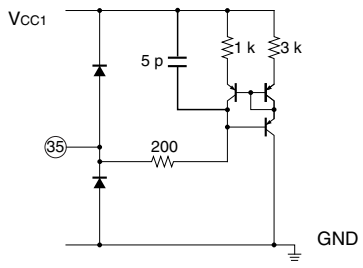
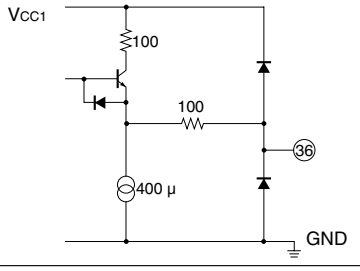
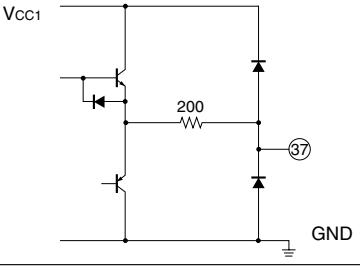
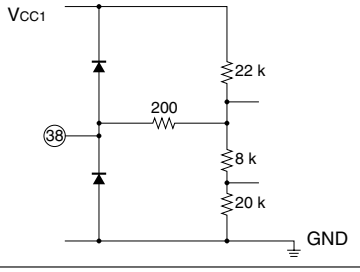
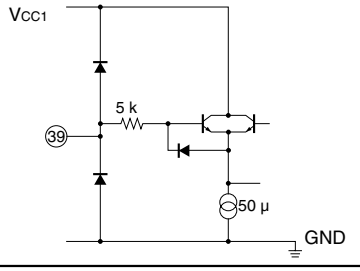
PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
6	V_{CC1}			Power supply for analog circuits.
7	GND_1			Ground for analog circuits.
8	EE NR			Comparator output for electronic exposure control.
9	SET NR			High reference voltage input of the comparator for electronic exposure control.
10	IRIS IN			Input of the amplifier for electronic exposure control. This amplifier has 5 times gain.
11	SET UP			Low reference voltage input of the comparator for electronic exposure control.
12	EE UP			Output of the comparator for electronic exposure control.
13	SYNC			Synchronous signal input.

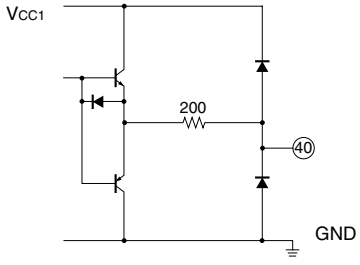
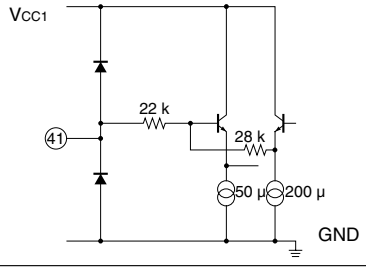
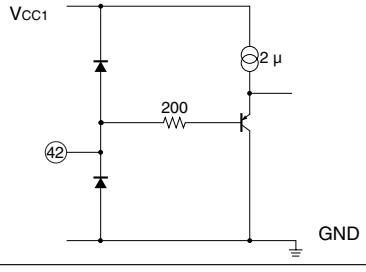
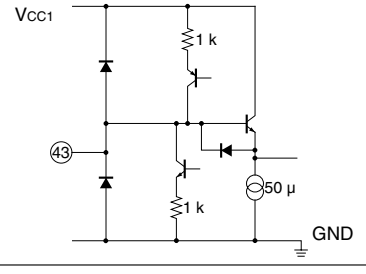
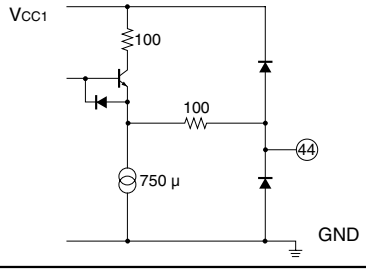
PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
14	BLK CLP			Composite pulse input. (pulse for optical black clamp and pulse for blanking)
15	BCLIP			Adjustment for the base clip level in the aperture circuit. Eliminates the low-level noise of aperture signal. When opened, base clip is canceled.
16	VCC2			Power supply for output amplifier circuits.
17	VIDEO OUT	1.5 V		Video signal output. At 75 Ω terminated : 1 Vp-p (Synchronous level 0.3 Vp-p)
18	PEDESTAL	2.5 V		Blanking level adjustment. 100 mV when opened.

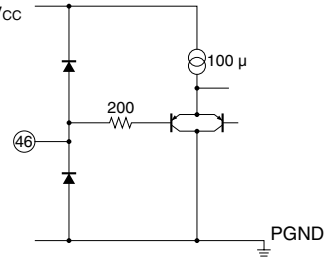
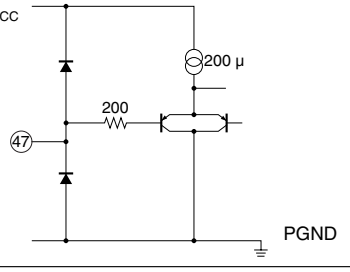
PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
19	WCLIP	3.3 V		White clip adjustment. 120% when opened.
20	CLAMP2	2.3 V		Input for encoder circuit. Black level of input signal is clamped to 2.3 V.
21	AMP2 OUT	1.0 V		Output for the gain control amplifier.
22	GAIN CTRL	2.5 V		Controls the output amplitude at pin No. 21. Gain is controlled in the range from 6 to 12 dB. It is approximately 10 dB when this pin is open.
23	C3	1.8 V		Feedback clamp detector. Connect capacitor between this pin and GND.

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
24	C_2	1.8 V		Feedback clamp detector. Connect capacitor between this pin and GND. When the external DL circuit is used, this will be input pin to make the aperture signal.
25	APA CTRL	1.8 V		Adjustment for the horizontal aperture amount. It is approximately 12 dB when this pin is open.
26	HAPA IN			Input for signal from pin 28. This signal is used as a main signal when aperture signals are mixed.
27	DL ADJ	1.2 V		Adjustment for built-in delay line. When 200 kΩ resistor is connected between this pin and GND, delay line can be turned off.
28	GAMMA OUT	2.3 V		Gamma and knee processed signal output.

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
29	KNEE ADJ	2.8 V		Knee adjustment. 120% when opened.
30	GAMMA ADJ	2.0 V		Gamma correction adjustment. 0.7 when opened.
31	GND_2			Ground for analog circuits.
32	AGC DET	2.0 V		Signal output for AGC control. Connect resistor between this pin and GND.
33	C_1	2.0 V		Feedback clamp detector. Connect capacitor between this pin and GND.
34	AMP_1 IN			Input for gamma and knee signal process.

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
35	LPF ADJ			Adjustment for built-in LPF characteristic. When connected resistor is 220 kΩ or more between this pin and GND, LPF can be turned off.
36	AGC OUT	2.3 V		AGC signal output.
37	VREF	2.0 V		Reference voltage.
38	VC	2.0 V		Bias for reference voltage. Connect capacitor between this pin and GND.
39	AGC CTRL			Gain control for AGC amplifier. Be sure to input the voltage within the range from 2 to 4 V.

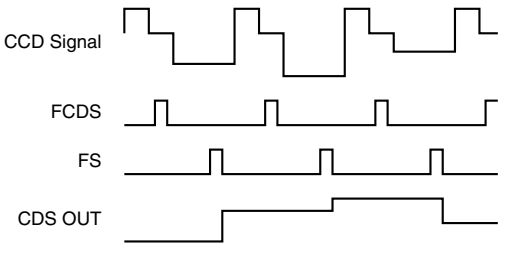
PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
40	AGC OP OUT			Output of the operation at amplifier for AGC control.
41	MAX GAIN	3.3 V		Adjustment for AGC amplifier maximum gain. Maximum gain is 18 dB when opened. When applied voltage is 0.62 V or less, AGC circuit turns off and the amplifier is fixed to 0 dB.
42	AGC OP IN			The operational amplifier for AGC control.
43	CLAMP1	2.0 V		Input of AGC amplifier. Black level is clamped at 2.0 V.
44	CDS OUT	2.4 V		CDS signal output.

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
45	PVCC			Power supply for pulse circuits.
46	FS			Pulse input for sample-hold.
47	FCDS			Pulse input for feed-through level clamp.
48	PGND			Ground for pulse circuits.

FUNCTIONAL OPERATION

CDS Circuit

The feed-through level of the input signal is clamped by the clamp circuit. Then the signal period is sampled and other periods are held by the sample and hold circuit, so that signals can be obtained.



Highlight Clip Circuit

Before the AGC circuit, excessive signals of more than approximately 0.5 Vp-p are clipped.

AGC Amplifier Circuit

The amplitude of output signals from the AGC amplifier is externally detected and the gain is controlled with control signals from the AGC operational amplifier. Decreasing voltage at pin 41 to 0.62 V or less causes the amplifier to be fixed to 0 dB.

LPF Circuit

The characteristics can be controlled with an external resistor at pin 35. Increasing the resistor to 220 kΩ or more allows signals passing over the LPF to be output.

Gamma and Knee Corrections Circuits

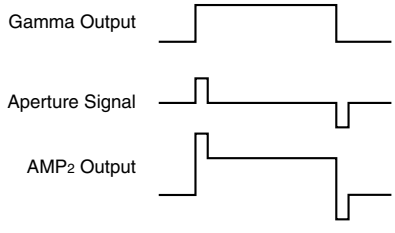
In order to comply with the characteristics of CRT, the high-bright part is suppressed. Pin 29 and 30 can be used to control this suppression. If voltage at pin 30 is increased to 4 V or more gamma will be 1.

Exposure Circuit

Signals which have not been processed by AGC are amplified, suppressed by gamma correction, and then output. Control signals can be generated by inputting the above signals to pin 10 after detecting them.

Aperture Circuit

The video articulation can be increased by enhancing the signal contour. If the built-in delay line is not used, it can be turned off by using an external resistor of minimum 200 kΩ at pin 27.
To control the aperture amount, use a base clip.



Output Circuit

A load of 75 Ω can be driven directly. In addition, the pedestal level can be controlled vertically.

CAUTIONS

- To control the aperture amount, apply base clip by controlling pin 15.
- Avoid connecting or disconnecting an external resistor at pin 27 to prevent the malfunction of the built-in delay line.
- Use the shortest possible distance to connect the bypass capacitors between the power supply and GND pins. The addition or removal of any external component should be determined by how the existing components are mounted.
- This device is electronically sensitive. Handle only at electrostatically safe work stations.

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, T_A = +25 ˚C)

PARAMETER	SYMBOL	CONDITIONS	RATING		UNIT
			IR3Y30M	IR3Y30M1	
Supply voltage	V_{CC1}, V_{CC2}		7		V
	PV_{CC}		7		V
Input voltage	V_{IA}	Except for pins 46 (FS) and 47 (FCDS)	V_{CC}		V
	V_{IP}	Pins 46 (FS) and 47 (FCDS)	−0.2 to PV_{CC} + 0.2		V
Comparator output voltage	V_{SD}		V_{CC}		V
Power consumption	P_D	$T_A \leq$ +25 ˚C	725	560	mW
P_D derating ratio		$T_A >$ +25 ˚C	5.8	4.5	mW/˚C
Operating temperature	T_{OPR}		−30 to +75	−30 to +70	˚C
Storage temperature	T_{STG}		−55 to +150		˚C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT
Supply voltage	V_{CC}	Pins 6 (V_{CC1}), 16 (V_{CC2}) and 45 (PV_{CC})	4.75 to 5.25	V
H-aperture signal	$V_{H\text{-}AP}$	Pin 26 (HAPA IN)	600 (MAX.)	mVp-p
Standard CCD input signal	V_{CCD}	Pin 1 (CCD IN)	200 (TYP.)	mVp-p
Clamp pulse width	t_{FS}	Pin 46 (FS)	15 (MIN.)	ns
Sample-hold pulse width	t_{FCDS}	Pin 47 (FCDS)	15 (MIN.)	ns

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, T_A = +25 ˚C, V_{CC} = 5.0 V, SW conditions→(a), V_{26} = 2.3 V, V_{34} = 2.0 V, V_{39} = 3 V, R27 = 30 kΩ, R35 = 22 kΩ)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Supply current	I_{CC1}	Measure pin 6 (V_{CC1}).			43.0	54.5	mA
	I_{CC2}	Measure pin 16 (V_{CC2}).			5.7	7.8	mA
	I_{CC3}	Measure pin 45 (PV_{CC}).			4.3	5.4	mA
CDS Circuit							
Low frequency attenuation	G_{LF}	With signal 1 applied to SG1, measure the signal attenuation on TP44. FS = 5 V, FCDS = Signal 2 (FCDS), V_A = TP44 amplitude (f = 100 kHz), V_B = TP44 amplitude (f = 10 MHz) G_{LF} = 20✻LOG (V_A/V_B)			–30	–25	dB
Gain	G_{CDS}	Signal 2 applied to SG1, FS and FCDS, measure the amplitude on TP44. SG1 = 200 mVp-p, f = 10 MHz		–2	0	2	dB
Clamp bias	$V_{CP/BIAS}$			2.7	2.9	3.1	V
AGC Operational Amplifier Circuit							
Low level	A_{OPL}	Measure the voltage on TP40B. SW40, SW42→(b)	V_{42} = 3 V, I_{40} = +200 µA		1.0	1.2	V
High level	A_{OPH}		V_{42} = 1 V, I_{40} = –200 µA	3.9	4.1		
Exposure Operational Amplifier & Comparator Circuits							
Operational amplifier gain	G_{OP}	With V_{10} = 2.3 V, measure the voltage of V_{9a} (TP8 : L→H) and V_{11a} (TP12 : H→L). With V_{10} = 2.4 V, measure the voltage of V_{9b} (TP8 : L→H) and V_{11b} (TP12 : H→L). G_{OP} = (V_{9b}-V_{9a}) or (V_{11b}-V_{11a}) SW9, SW10, SW11→(b)		0.40	0.46	0.51	V
Comparator low level	I_{OPL}	Change the voltage of V_9 and V_{11}, and measure the voltage on TP8 and TP12. V_{10} = 2.3 V SW9, SW10, SW11→(b)			0	0.2	V
High level	I_{OPH}			4.70	4.95		
AGC Circuit							
Highlight clip level	H_{CL}	Change the amplitude of signal 3 which is applied to SG43, and measure the amplitude on TP36 when TP36's output signal is clipped. SW43, SW41→(b), Pulse→CLP, V_{41} = 0 V, R35 = 220 kΩ		0.4	0.5	0.6	Vp-p

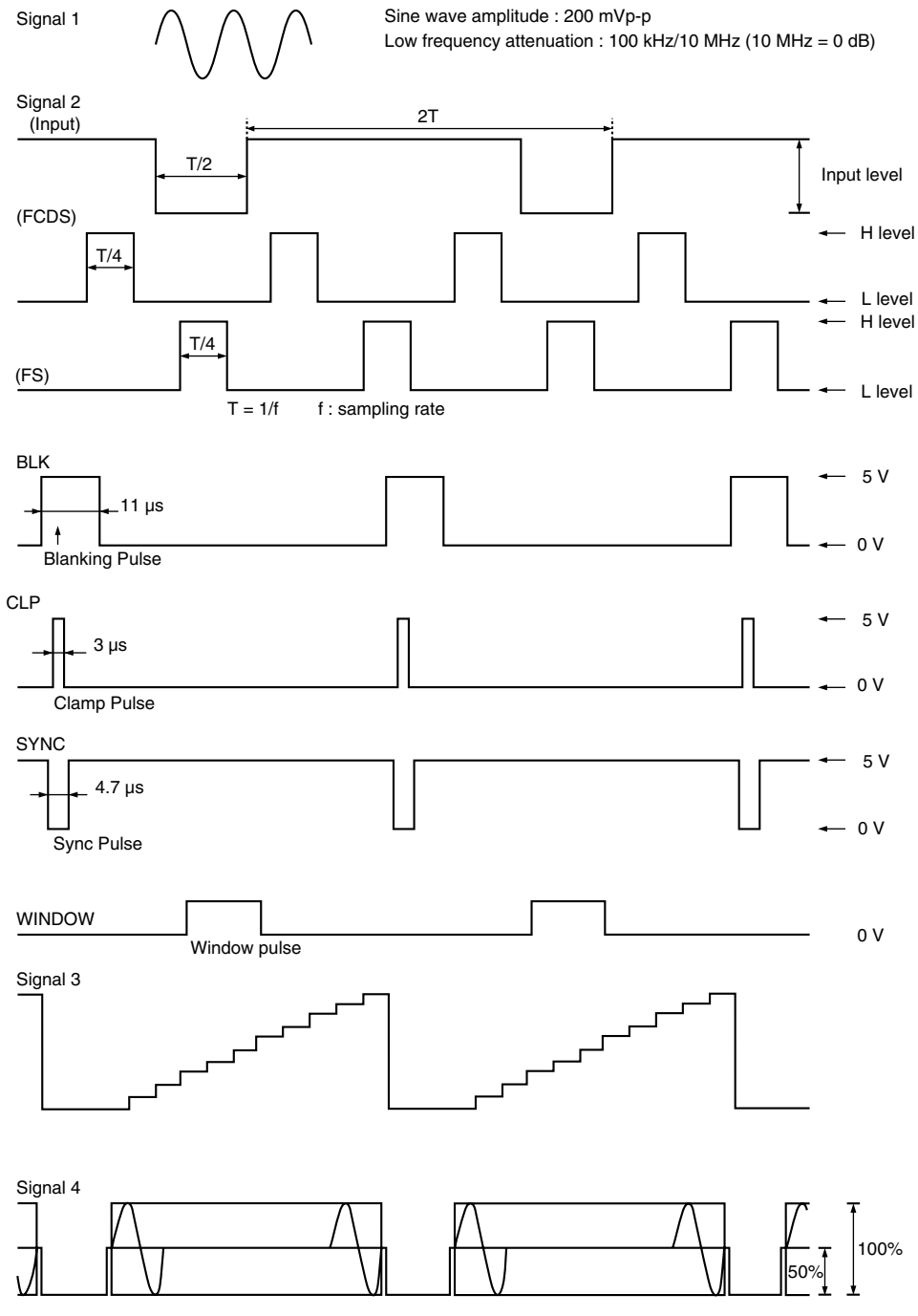
PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
AGC circuit (contd.)							
AGC maximum gain (1)	G_{AMAX1}	Apply signal 3 to SG43 and measure the amplitude on TP36. GA1 to GA4 = 20✻LOG (TP36 amplitude/SG43 amplitude) SW41, SW43→(b), Pulse→CLP, R35 = 220 kΩ	SG43 = 20 mVp-p V_{39} = 4 V, V_{41} = 5 V	27	29	31	dB
AGC maximum gain (2)	G_{AMAX2}		SG43 = 20 mVp-p V_{39} = 4 V, SW41→(a)	15.5	18.0	20.5	
AGC minimum gain	G_{AMIN}		SG43 = 400 mVp-p V_{39} = 2 V, V_{41} = 5 V	−6.5	−3.5	−0.5	
AGCOFF gain	G_{AOFF}		SG43 = 200 mVp-p V_{39} = 4 V, V_{41} = 0 V	−2	0	2	
Output dynamic range	D_A	Apply signal 3 to SG43 and measure the amplitude on TP36. SG43 = 50 mVp-p, SW41, SW43→(b), Pulse→CLP, V_{39} = 4 V, V_{41} = 5 V, R35 = 220 kΩ		0.55	0.75		Vp-p
Frequency characteristic (1)	f_{A1}	Apply signal 4 to SG43. Increase the frequency of signal 4 until the frequency components of the signal on TP36 are 3 dB lower than that at f = 100 kHz, and measure the frequency of signal 4. SW41→(b), Pulse→CLP, V_{41} = 5 V When measuring case (2), adjust the V_{39} such that the amplitude of the output on TP36 is 200 mVp-p.	SG43 = 10 mVp-p R35 = 22 kΩ V_{39} = 4 V	3.5	4.5		MHz
Frequency characteristic (2)	f_{A2}		SG43 = 200 mVp-p R35 = 220 kΩ	7.0	10.0		
Frequency characteristic (3)	f_{A3}		SG43 = 10 mVp-p R35 = 22 kΩ V_{39} = 4 V f = 9.5 MHz		−35	−25	dB
AGC ON/OFF switching voltage	V_{AGC}	Apply signal 3 to SG43, change V_{41}, and measure the voltage of V_{41} when the gain on TP36 changes from −3.5 to 0 dB. The gain on TP36 : 20✻LOG (TP36 amplitude/SG43 amplitude) SG43 = 400 mVp-p, SW43, SW41→(b), Pulse→CLP, V_{39} = 2 V, R35 = 220 kΩ		0.4	0.6	0.8	V
Reference voltage 1	V_{REF}	Measure the voltage on TP37A.		1.84	1.94	2.04	V
Reference voltage 2	ΔV_{REF2}	With I_{37} = +500 µA, measure the change in voltage on TP37B. SW37→(b)		0	0.15	0.30	V
Reference voltage 3	ΔV_{REF3}	With I_{37} = −500 µA, measure the change in voltage on TP37B. SW37→(b)		−0.30	−0.15	0	V

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Exposure Circuit							
Exposure AMP gain	G_I	Apply signal 3 to SG43 and measure the amplitude on TP5. SW3, SW4, SW43→(b), Pulse→CLP, BLK	SG43 = 200 mVp-p V_3 = 5 V, V_4 = 5 V	10.5	11.5	12.5	dB
Gamma output level	γ_{PRE}		SW3→(a)	0.25	0.32	0.40	Vp-p
Output dynamic range	D_I		SG43 = 800 mVp-p V_3 = 5 V, V_4 = 5 V	1.5	1.9		Vp-p
Black level	B_I	Measure the voltage on TP5. SW4→(b), Pulse→CLP, BLK, V_4 = 0 V		2.15	2.30	2.45	V
Black level offset 1	B_{IOFF1}	Measure the voltage on TP5. SW4→(b), Pulse→CLP, BLK	V_4 = 5 V	–50	0	50	mV
Black level offset 2	B_{IOFF2}		V_4 = 0 V	–50	0	50	
Frequency characteristic	f_I	Apply signal 4 to SG43. Increase the frequency of signal 4 until the frequency components of the signal on TP5 are 3 dB lower than that at f = 100 kHz, and measure the frequency of signal 4. SG43 = 200 mVp-p, V_4 = 5 V, SW4, SW43→(b), Pulse→CLP, BLK		0.7	1.1		MHz
Window OFF output level	O_{WOFF}	Apply signal 3 to SG43 and measure the amplitude on TP5. SG43 = 200 mVp-p, SW4, SW43→(b), Pulse→CLP, BLK, V_4 = 0 V			40	70	mVp-p
Window ON switching voltage	V_W	Same as in the window OFF output level measurement. Increase V_4, and measure V_4 when the amplitude of output signal on TP5 is not changed.		1.2	1.4	1.6	V
Window input current	I_W	With V_4 = 5 V, measure input current on pin 4. SW4→(b)		0.5	1.2	3.0	µA
AMP_1 Circuits							
AMP_1 gain	G_{AMP1}	Apply signal 3 to SG34 and measure the amplitude on TP32. SW34→(b), Pulse→CLP, BLK, SG34 = 100 mVp-p, Black level = 2 V		13	14	15	dB
Output dynamic range	D_{AMP1}	Same as in the AMP_1 gain measurement. Measure output dynamic range on TP32.		1.20	1.40		Vp-p
Black level	B_{AMP1}	Measure the voltage on TP32. Pulse→CLP, BLK		1.9	2.0	2.1	V
Gamma & Knee Circuits							
Gamma gain (1)	$G_{\gamma1}$	Apply signal 3 to SG34 and measure the amplitude on TP28. SW34→(b), Pulse→CLP, BLK, Input black level = 2 V	SG34 = 100 mVp-p	310	410	510	mVp-p
Gamma gain (2)	$G_{\gamma2}$		SG34 = 30 mVp-p		–6.4		dB
Gamma gain (3)	$G_{\gamma3}$		SG34 = 200 mVp-p		1.3		

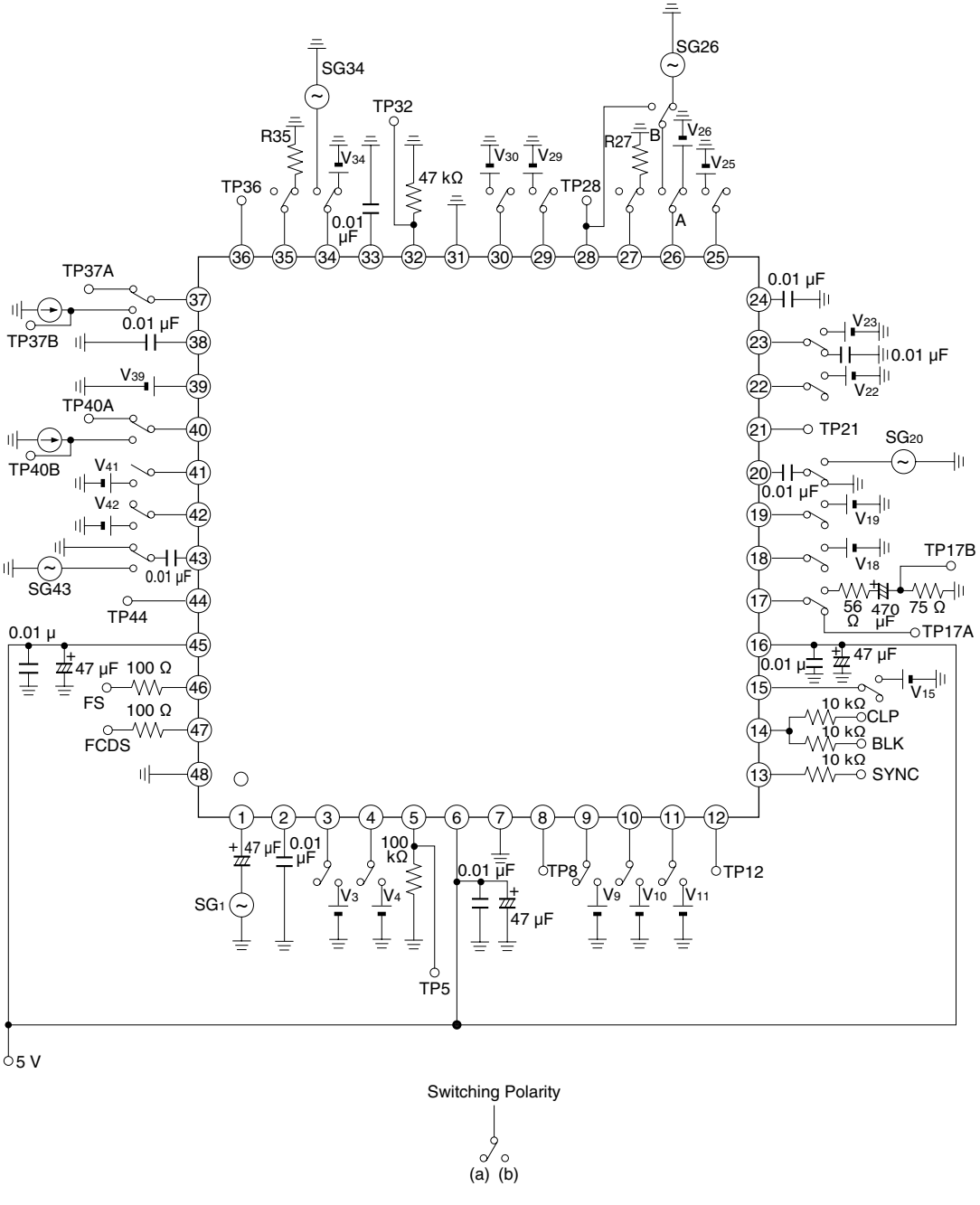
PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Gamma & Knee Circuits (contd.)							
Gamma OFF gain	$G_{\gamma OFF}$	Apply signal 3 to SG34 and measure the amplitude on TP28. SW29, SW30, SW34→(b), Pulse→CLP, BLK, SG34 = 100 mVp-p, Black level = 2 V, V_{29} = 5 V, V_{30} = 5 V		450	510	580	mVp-p
Cleaning offset	(1) C_{L1}	Measure the amplitude of TP28 between BLK level and black level. Pulse→CLP, BLK	SW30→(a)	−50	0	50	mV
	(2) C_{L2}		SW30→(b), V_{30} = 5 V	−50	0	50	
Frequency characteristic	f_γ	Apply signal 4 to SG34. Increase the frequency of signal 4 until the frequency components of the signal on TP28 are 3 dB lower than that at f = 100 kHz, and measure the frequency of signal 4. SW34→(b), Pulse→CLP, BLK, SG34 = 100 mVp-p, Black level = 2 V		6.0			MHz
Aperture & AMP2 Circuits							
Aperture maximum gain	G_{APMAX}	Apply signal 3 to SG26 and measure the amplitude on TP21. SW26A→(b), Pulse→CLP, BLK, SG26 = 100 mVp-p, Black level = 2.3 V	SW25→(b), V_{25} = 5 V	840	1 130		mVp-p
Aperture preset gain	G_{APPRE}			740	840	940	
Aperture minimum gain	G_{APMIN}		SW25→(b), V_{25} = 0 V	320	420	520	
Base clip output	B_{CL}		SW15→(b), V_{15} = 0 V SW25→(b), V_{25} = 5 V	250	350	450	
Delay line output	DL_{OUT}	Apply signal 3 to SG34 and measure the amplitude on TP21. SW15, SW23, SW25, SW29, SW30, SW34→(b), Pulse→CLP, BLK, SG34 = 50 mVp-p, Black level = 2 V, V_{15} = V_{25} = V_{29} = V_{30} = 5 V, V_{23} = 1.2 V, V_{26} = 2.3 V		1 100	1 700		mVp-p
AMP2 maximum gain	$G_{AMP2MAX}$	Apply signal 3 to SG26 and measure the amplitude on TP21. Pulse→CLP, BLK, SW15, SW22, SW25, SW26A→(b), Input black level = 2.3 V, V_{15} = V_{25} = 0 V	SG26 = 100 mVp-p, V_{22} = 5 V	370	440	510	mVp-p
AMP2 minimum gain	$G_{AMP2MIN}$		SG26 = 100 mVp-p, V_{22} = 0 V	180	230	280	
Output dynamic range	D_{AMP2}		SG26 = 800 mVp-p, V_{22} = 5 V	2 000	2 550		
Frequency characteristic	f_{AMP2}	Apply signal 4 to SG26. Increase the frequency of signal 4 until the frequency components of the signal on TP21 are 3 dB lower than that at f = 100 kHz, and measure the frequency of signal 4. SW15, SW25, SW26A→(b), V_{15} = 0 V, V_{25} = 0 V, Pulse→CLP, BLK, SG26 = 100 mVp-p, Black level = 2.3 V		8.0			MHz

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Encoder Circuit							
White clip (1)	W_{C1}	Apply signal 3 to SG20 and measure the amplitude on TP17A. SW20→(b), Pulse→CLP, BLK	SW19→(b), V_{19} = 5 V	1.9	2.0		V
White clip (2)	W_{C2}		SW19→(b), V_{19} = 0 V		0.85	0.95	
White clip preset	W_{CPRE}		SW19→(a)	1.75	1.85	1.95	
Setup (1)	S_{UP1}	Measure the amplitude of TP17A between BLK level and black level. Pulse→CLP, BLK	SW18→(b), V_{18} = 5 V	230	280		mV
Setup (2)	S_{UP2}		SW18→(b), V_{18} = 0 V		−310	−260	
Setup preset	S_{UPPRE}		SW18→(a)	−150	−100	−50	
SYNC level	V_{SYNC}	Measure the amplitude of TP17A between SYNC level and black level. Pulse→CLP, BLK, SYNC		530	580	630	mV
Gain	G_{OUT}	Apply signal 3 to SG20 and measure the amplitude on TP17A. SW20→(b), Pulse→CLP, BLK, SG20 = 1 Vp-p		−1	0	1	dB
Output dynamic range	D_{OUT}	Apply signal 3 to SG20 and measure the amplitude of TP17A between SYNC level and white level. SW19, SW20→(b), V_{19} = 5 V, Pulse→CLP, BLK, SYNC		2.2	2.5		Vp-p
Frequency characteristic	f_{OUT}	Apply signal 4 to SG20. Increase the frequency of signal 4 until the frequency components of the signal on TP17B are 3 dB lower than that at f = 100 kHz, and measure the frequency of signal 4. SG20 = 1 Vp-p, SW17, SW20→(b), Pulse→CLP, BLK, SYNC		10			MHz
Output voltage	V_{OUT}	Apply signal 3 to SG20 and measure the amplitude of TP17B between SYNC level and white level. SG20 = 1.3 Vp-p, SW17, SW20→(b), Pulse→CLP, BLK, SYNC		0.9	1.0		Vp-p
Pulse Circuit							
Clamp threshold voltage	V_{FCDS}	Apply voltages to FCDS, FS, SYNC, BLK and CLP and measure the threshold voltage of each circuit.			1.3		V
Sample-hold threshold voltage	V_{FS}				1.5		
Synchronous signal threshold voltage	V_{SYNC}				2.5		
Blanking threshold voltage	V_{BLK}				1.5		
Clamp threshold voltage	V_{CP}				3.5		

Measurement Waveforms



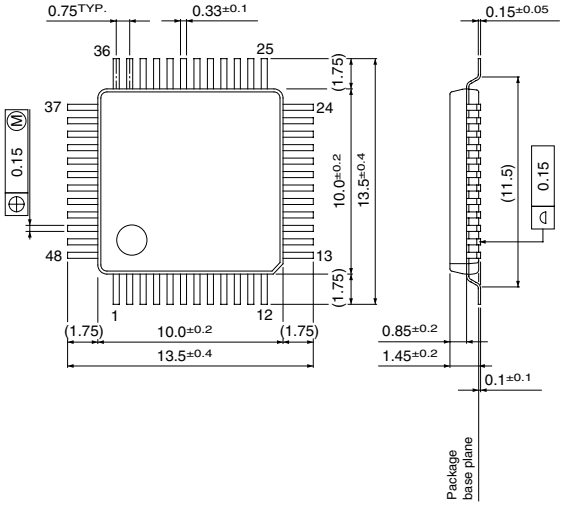
Test Circuit



PACKAGES

(Unit : mm)

48 QFP (QFP048-P-1010)



48 QFP (QFP048-P-0707)