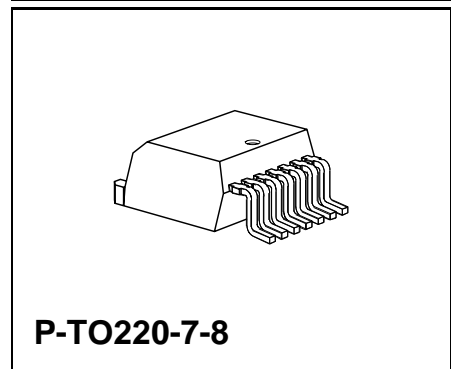
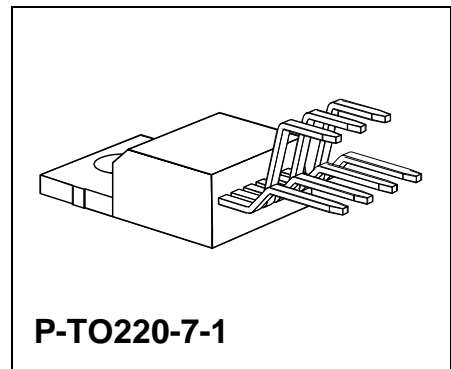


### Overview

SPT IC <sup>1)</sup>

### Features

- Output current  $\pm 3$  A
- I/O error diagnostics
- Short-circuit proof
- Four-quadrant operation
- Integrated free-wheeling diodes
- Wide temperature range
- Break low **and** break high, if open load detection is required, the device TLE 5203 will fit



Type	Ordering Code	Package
TLE 5204	Q67000-A9177	P-TO220-7-1
TLE 5204 G	Q67006-A9234	P-TO220-7-8

### Description

TLE 5204 is an integrated power bridge with DMOS output stages for driving DC motors. This motor bridge is optimized for driving DC motors in reversible operation. The internal protective circuitry in particular ensures that no crossover currents can occur.

Because the free-wheeling diodes are integrated, the external circuitry that is necessary is reduced to the capacitors on the supply voltage.

The control inputs have TTL/CMOS-compatible levels.

<sup>1)</sup> **SIEMENS Power Technology**

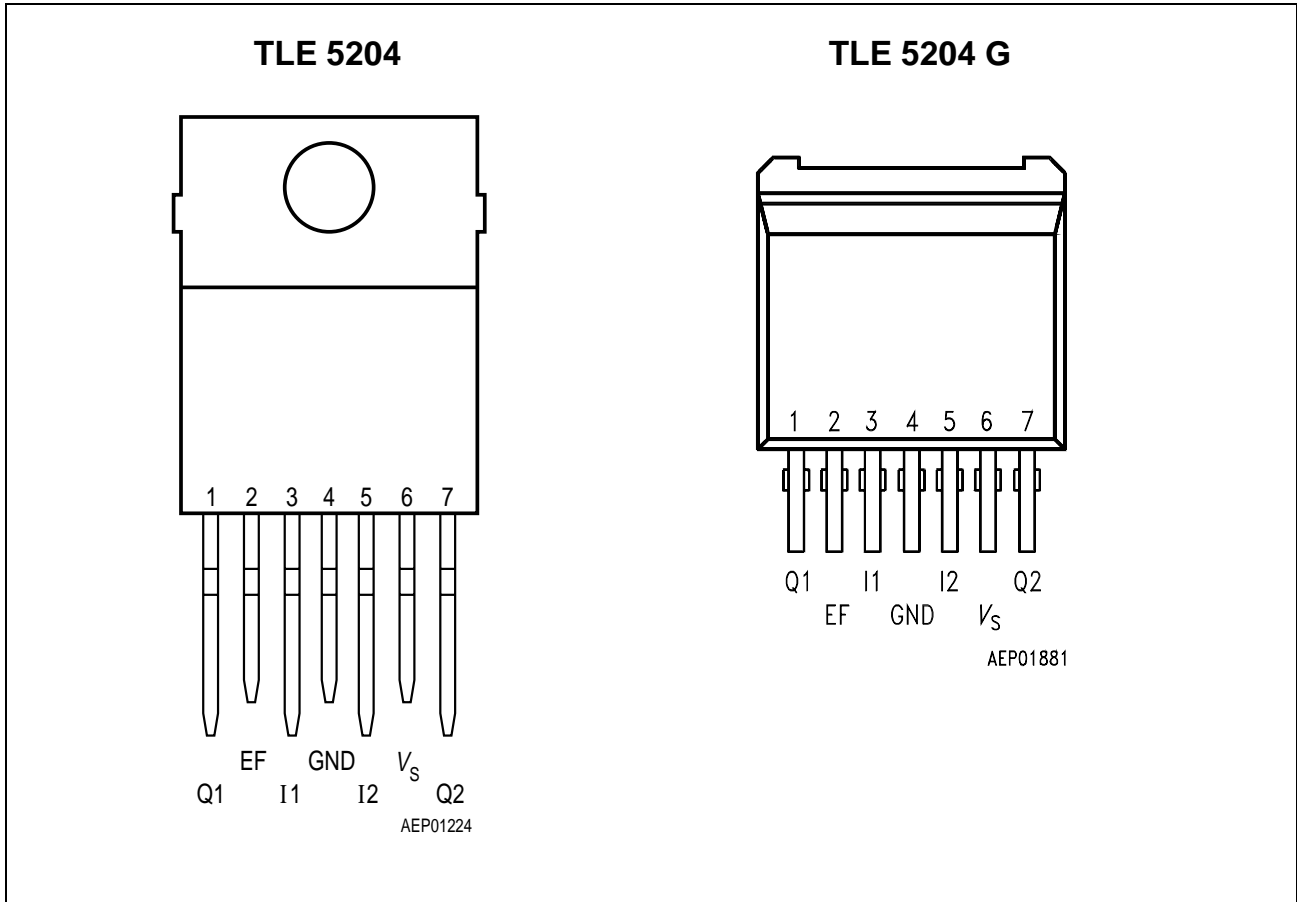


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	Q1	<b>Output of channel 1</b> ; Short-circuit proof, free-wheeling diodes integrated for inductive loads
2	EF	<b>Error flag</b> ; TTL/CMOS-compatible output for error detection (open drain)
3	I1	<b>Control input 1</b> ; TTL/CMOS-compatible
4	GND	<b>Ground</b> ; connected internally to cooling fin
5	I2	<b>Control input 2</b> ; TTL/CMOS-compatible
6	V <sub>s</sub>	<b>Supply voltage</b> ; wire with capacitor matching load
7	Q2	<b>Output of channel 2</b> ; Short-circuit proof, free-wheeling diodes integrated for inductive loads

## Circuit Description

### Input Circuit

The control inputs consist of TTL/CMOS-compatible Schmitt triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages.

### Output Stages

The output stages form a switched H-bridge. Protective circuits make the outputs short-circuit proof to ground and to the supply voltage throughout the operating range. Positive and negative voltage spikes, which occur when switching inductive loads, are clamped by integrated power diodes.

### Functional Truth Table

E1	E2	Q1	Q2	Comments
L	L	L	L	Motor brake; both low side transistors turned-ON
L	H	L	H	Motor turns clockwise
H	L	H	L	Motor turns counterclockwise
H	H	H	H	Motor brake; both high side transistors turned-ON

### Notes for Output Stage

Symbol	Value
L	Low side transistor is turned-ON High side transistor is turned-OFF
H	High side transistor is turned-ON Low side transistor is turned-OFF

**Monitoring Functions**

An internal circuit ensures that all output transistors are turned-OFF if the supply voltage is below the operating range.

A monitoring circuit for each output transistor detects whether the particular transistor is active and in this case prevents the corresponding source transistor (sink transistor) from conducting in sink operation (source operation). Therefore no crossover currents can occur. Pulse-width operation is possible up to a maximum switching frequency of 1 kHz for any load.

Depending on the load current higher frequencies are possible.

**Protective Function**

Various errors like short-circuit to +  $V_s$ , ground or across the load are detected. All faults result in turn-OFF of the output stages after a delay of 40  $\mu$ s and setting of the error flag EF to ground. Changing the inputs resets the error flag.

**Output Shorted to Ground Detection**

If a high side transistor is switched on and its output is shorted to ground, the output current is limited to typ 8 A. After a delay of 40  $\mu$ s all outputs will be switched off and the error flag EF is set to ground.

**Output Shorted to +  $V_s$  and Overload Detection**

An internal circuit detects if the current through the low side transistor is higher than 4 A typ. In this case all outputs are turned-OFF after 40  $\mu$ s and the error flag is set to ground.

At a junction temperature higher than 160 °C the thermal shutdown turns-OFF, all four output stages commonly and the error flag is set without a delay.

**Diagnosis**

Input		Output		Diagnosis			EF
E1	E2	Q1	Q2	Shorted to GND	Shorted to $V_s$	Overload	
L	L	L	L	–	Q1, Q2	–	L
L	H	L	H	Q2	Q1	X	L
H	L	H	L	Q1	Q2	X	L
H	H	H	H	Q1, Q2	–	–	L

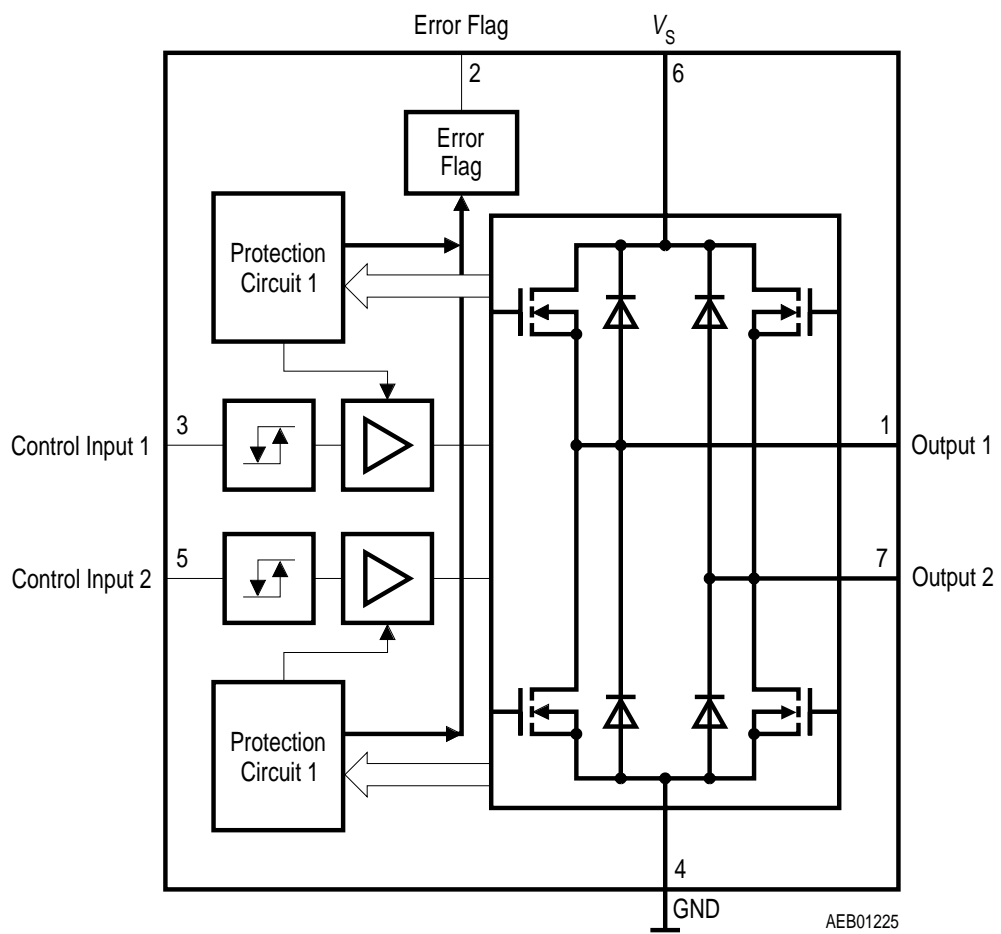


Figure 2 Block Diagram

## Absolute Maximum Ratings

$T_j = -40$  to  $150$  °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

### Voltage

Supply voltage	$V_S$	- 0.3	40	V	-
Supply voltage	$V_S$	- 1	-	V	$t < 500$ ms; $I_S < 5$ A
Logic input voltage	$V_{11,2}$	- 0.3	7	V	$V_S = 0 - 40$ V
Diagnostics output voltage	$V_{EF}$	- 0.3	7	V	-

### Current

Free-wheeling current	$I_F$	- 4	4	A	$T_j \leq 150$ °C
Output current <sup>1)</sup>	$I_Q$	- 4	4	A	-
Junction temperature	$T_j$	- 40	150	°C	-
Storage temperature	$T_{stg}$	- 50	150	°C	-

### Thermal Resistance

Junction-case	$R_{thjC}$	-	4	K/W	-
Junction-ambient	$R_{thjA}$	-	65	K/W	-

### Operating Range

Supply voltage	$V_S$	6	24	V	-
Logic input voltage	$V_{11,2}$	- 0.3	7	V	-
Switching frequency <sup>2)</sup>	$f$	-	1	kHz	-
Junction temperature	$T_j$	- 40	150	°C	-

- <sup>1)</sup> During overload condition currents higher than 4 A can dynamically occur, before the device shuts off, without any damaging the device.
- <sup>2)</sup> Depending on load higher frequencies are possible.

**Electrical Characteristics** $V_S = 6$  to  $18$  V;  $T_j = -40$  to  $150$  °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
<b>General</b>						
Quiescent current	$I_q$	–	–	10	mA	$I_L = 0$ A
Turn-ON delay	$t_{d1}$	–	10	20	µs	Input to output
Turn-OFF delay	$t_{d2}$	–	–	10	µs	Input to output
Turn-ON time	$t_r$	–	10	20	µs	$I_Q = 2.5$ A; cf diagram
Turn-OFF time	$t_f$	–	–	10	µs	$I_Q = 2.5$ A; cf diagram
Undervoltage	$V_S$	–	5.5	5.9	V	$I_{C ON}$
Undervoltage	$V_S$	–	4.5	5.2	V	$I_{C OFF}$

**Logic**

Control inputs						
H-input voltage	$V_{IH}$	2.8	–	–	V	–
L-input voltage	$V_{IL}$	–	–	1.2	V	–
Hysteresis of input voltage	$\Delta V_I$	0.4	0.8	1.2	V	–
H-input current	$I_I$	– 2	–	2	µA	$V_I = V_{IH}$
L-input current	$I_I$	– 10	– 4	0	µA	$V_I = V_{IL}$
Diagnosis output						
Delay time	$t_d$	20	40	60	µs	–
L-output voltage	$V_{EF}$	–	–	0.4	V	$I = 3$ mA
Leakage current	$I_{RD}$	–	–	10	µA	–
Error detection						
Switching threshold U	$V_{EH}$	2	2.7	3.5	V	Error low
Switching threshold L	$V_{EL}$	2	2.7	3.5	V	Error high
Overcurrent 1	$I_{F1}$	3	4	5	A	Error low

## Electrical Characteristics (cont'd)

$V_S = 6 \text{ to } 18 \text{ V}; T_j = -40 \text{ to } 150 \text{ }^\circ\text{C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Outputs

RDSONU	—	—	—	0.4	$\Omega$	$V_S > 6 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ <sup>1)</sup>
RDSONU	—	—	—	0.65	$\Omega$	$V_S > 6 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$ <sup>1)</sup>
RDSONL	—	—	—	0.4	$\Omega$	$V_S > 6 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ <sup>1)</sup>
RDSONL	—	—	—	0.65	$\Omega$	$V_S > 6 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$ <sup>1)</sup>
Diode forward voltage	$V_{FU}$	—	—	1.5	V	$I_F = 3 \text{ A}$
Diode forward voltage	$V_{FL}$	—	—	1.5	V	$I_F = 3 \text{ A}$

<sup>1)</sup> Values for RDSON are for  $t > 100 \mu\text{s}$  after applying +  $V_S$ .



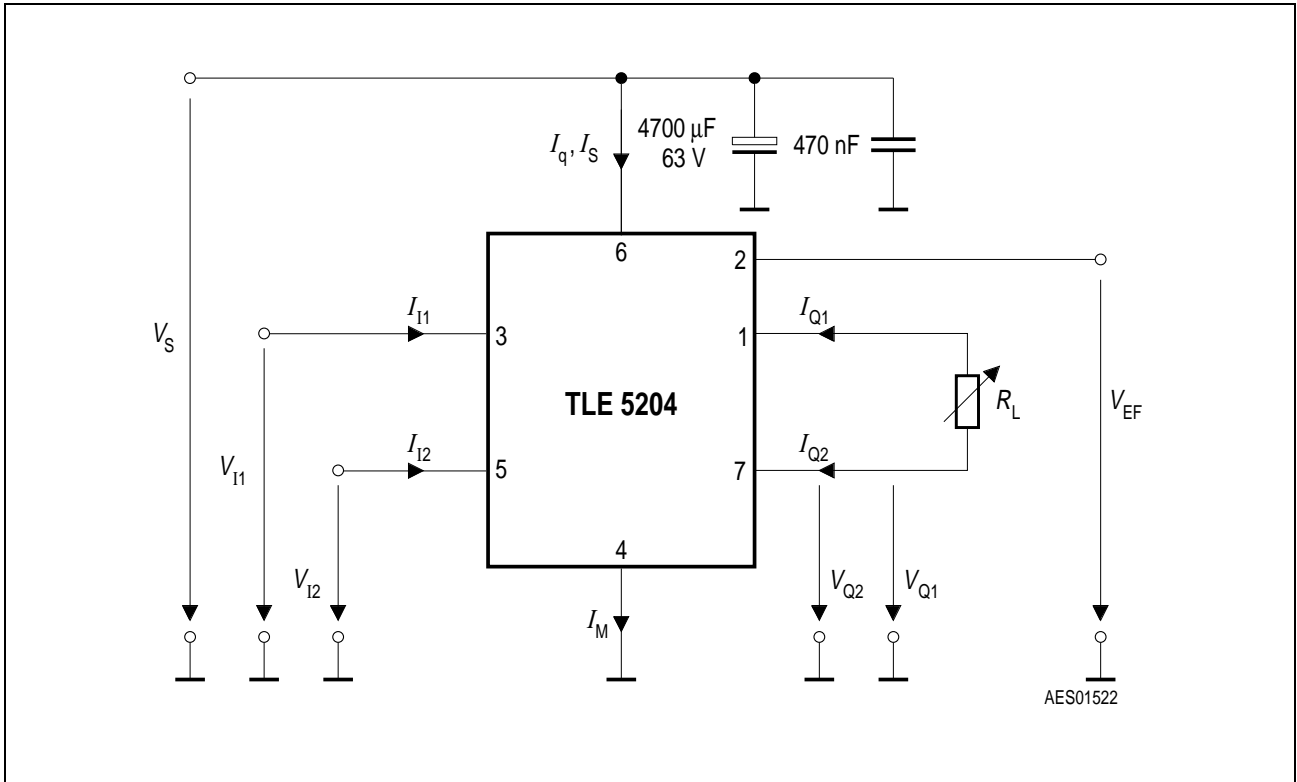


Figure 3 Test Circuit

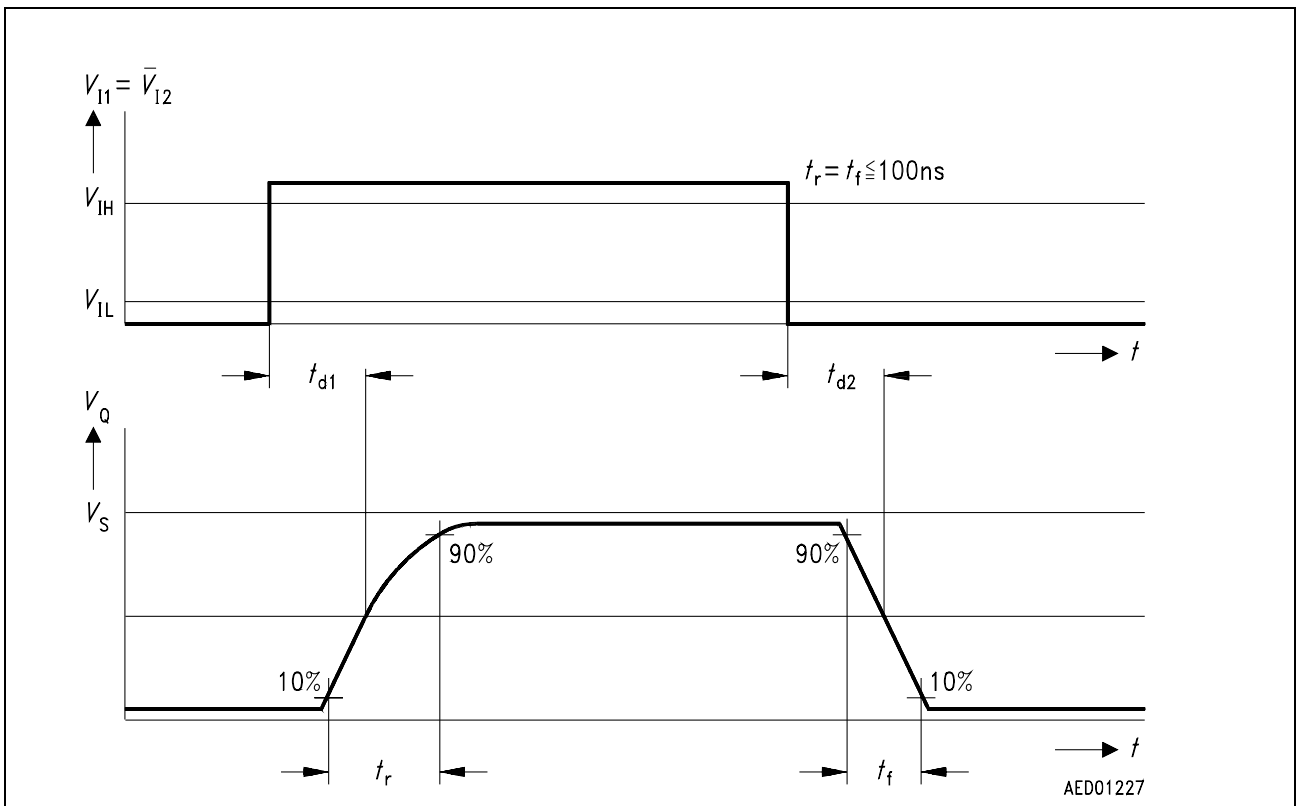


Figure 4 Timing Diagram

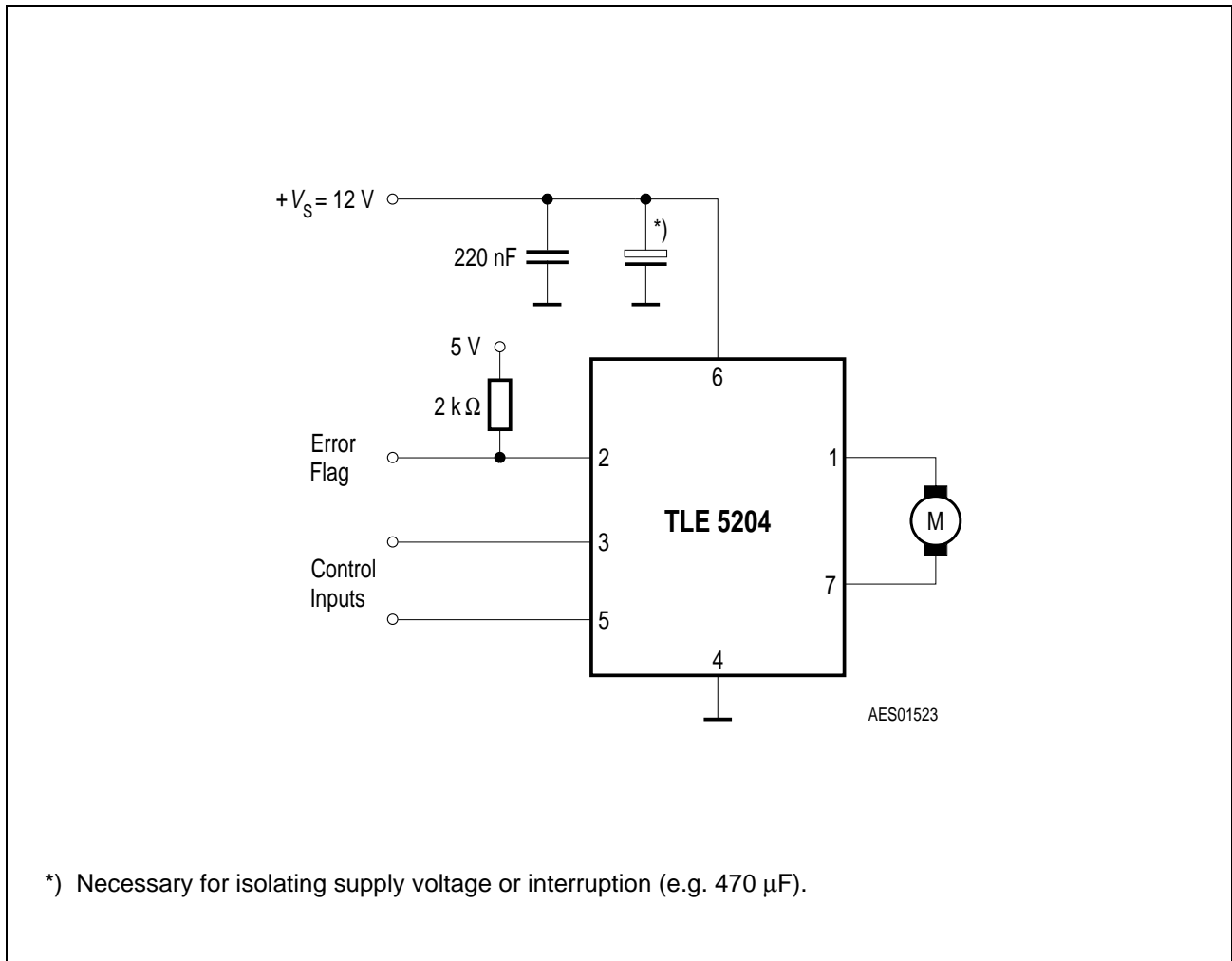
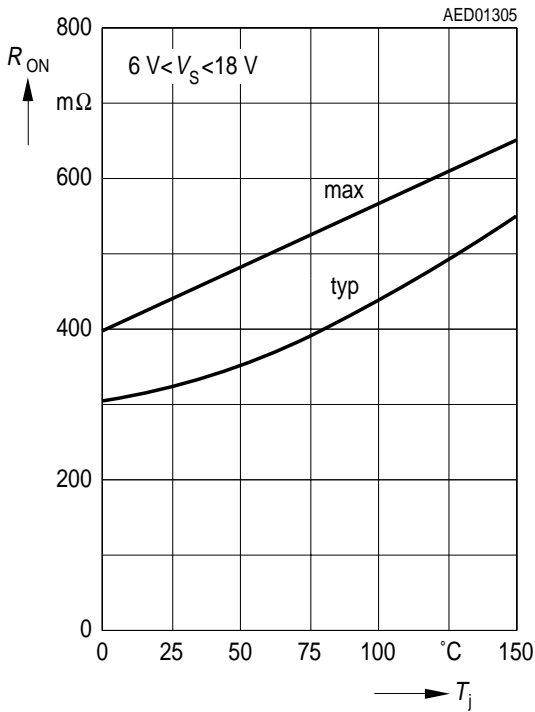


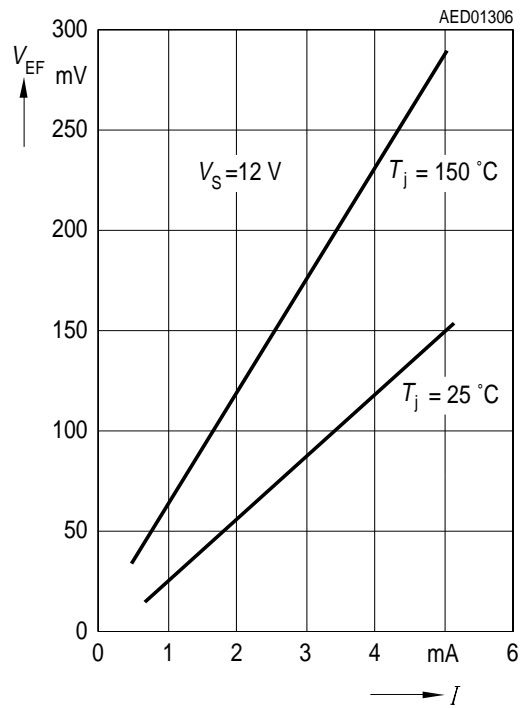
Figure 5 Application Circuit

## Diagrams

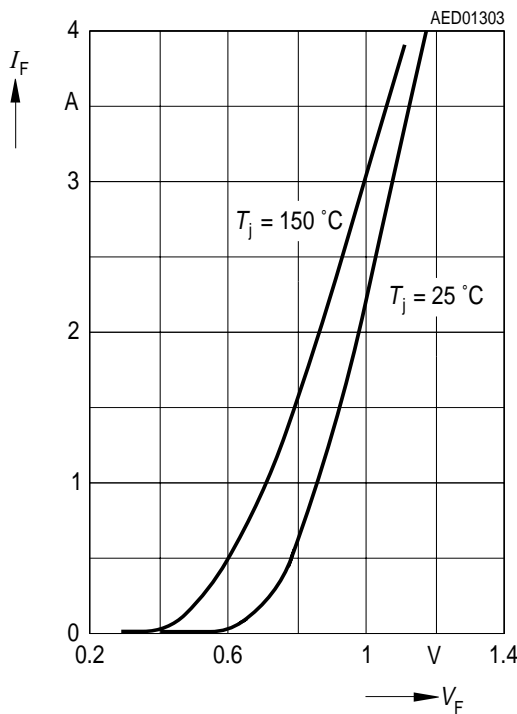
**$R_{ON}$  Resistance of Output Stage over Temperature**



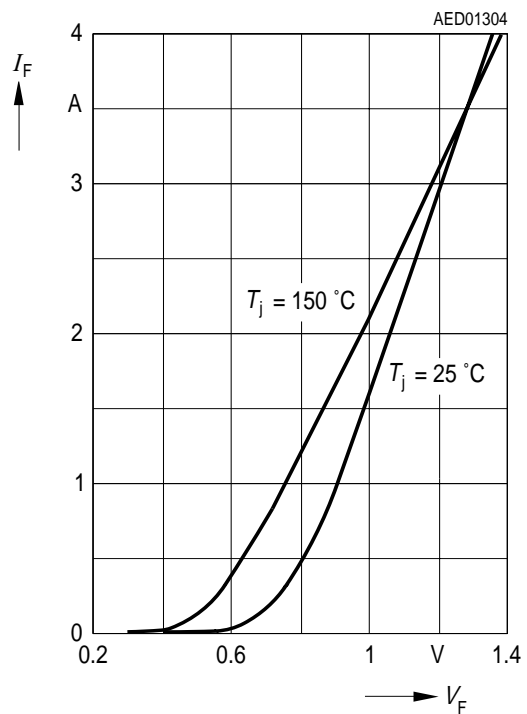
**Output Voltage on Diagnostics Output versus Current**



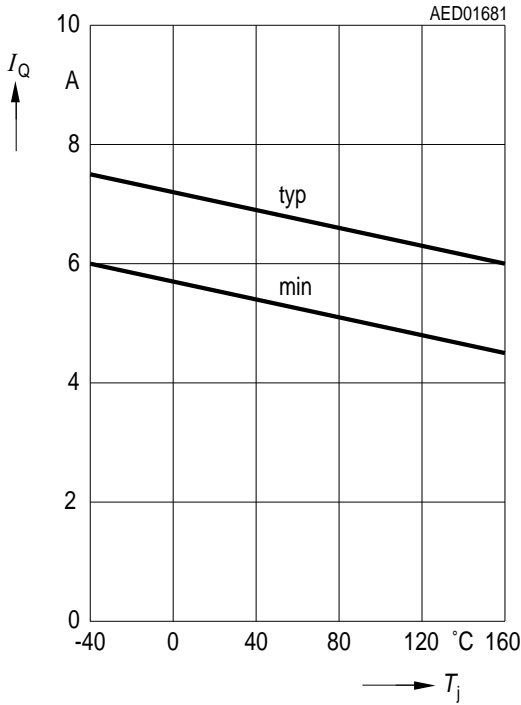
**Forward Current of Upper Free-Wheeling Diode versus Voltage**



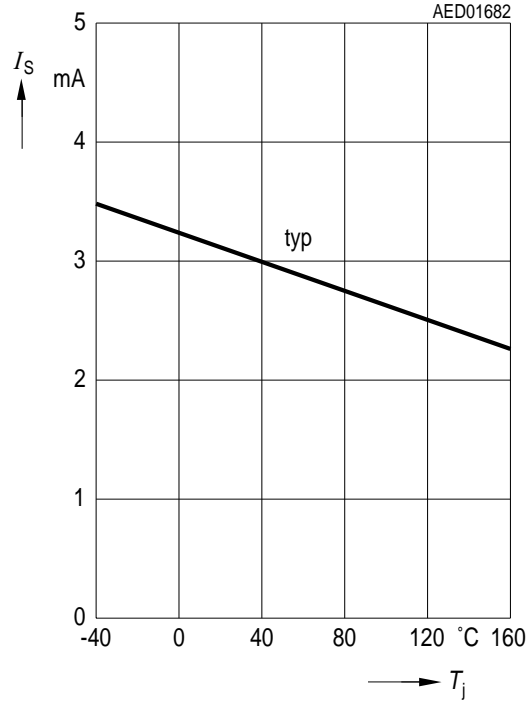
**Forward Current of Lower Free-Wheeling Diode versus Voltage**



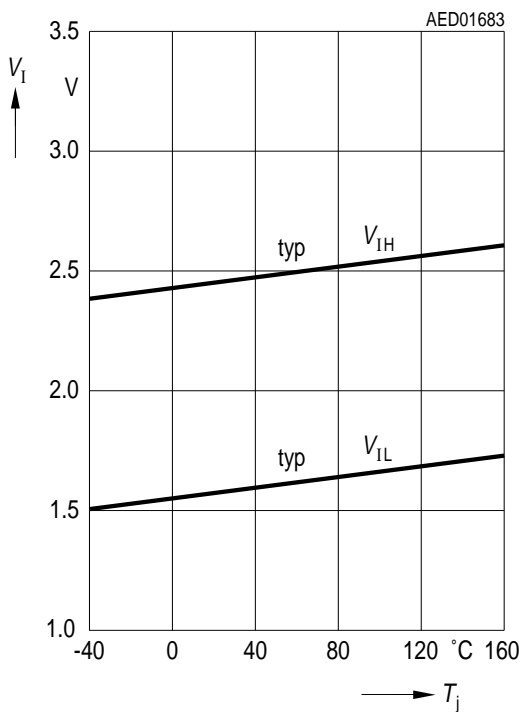
**Overcurrent Threshold versus Temperature**



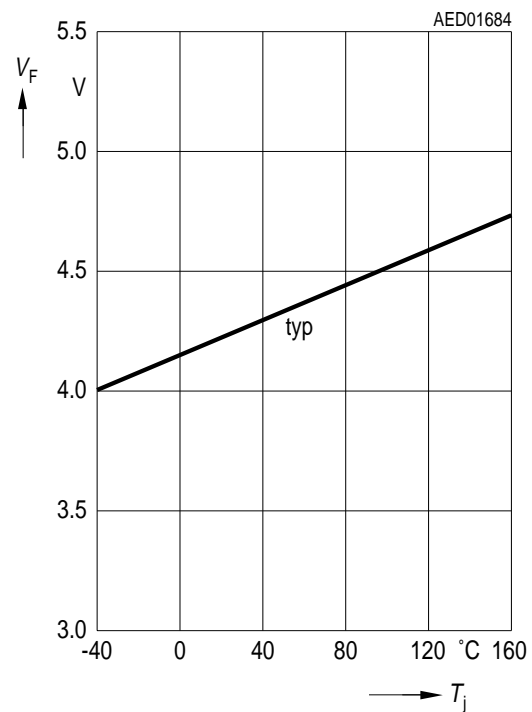
**Quiescent Current versus Temperature**



**Input Threshold versus Temperature**



**Switching Threshold  $V_{EL, EH}$  versus Temperature**



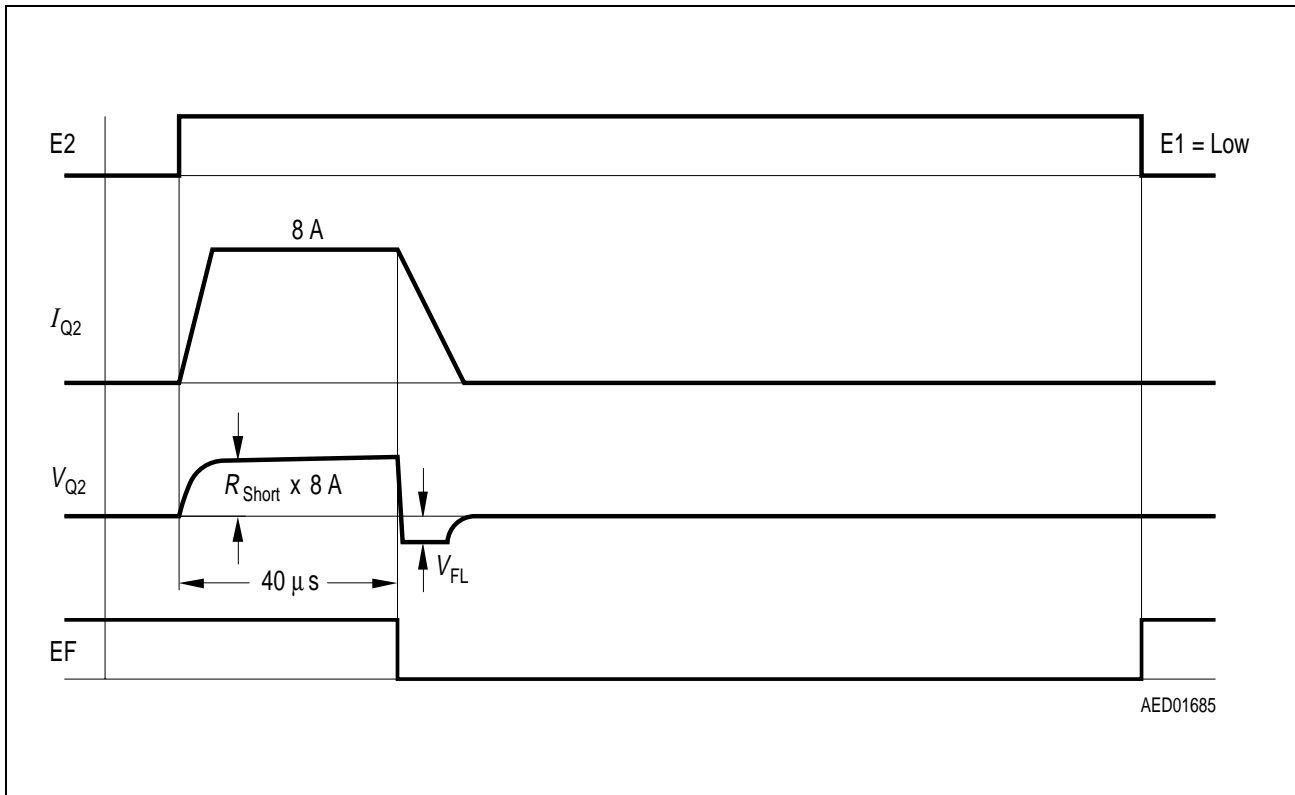


Figure 6 Timing Diagram for Output Shorted to Ground

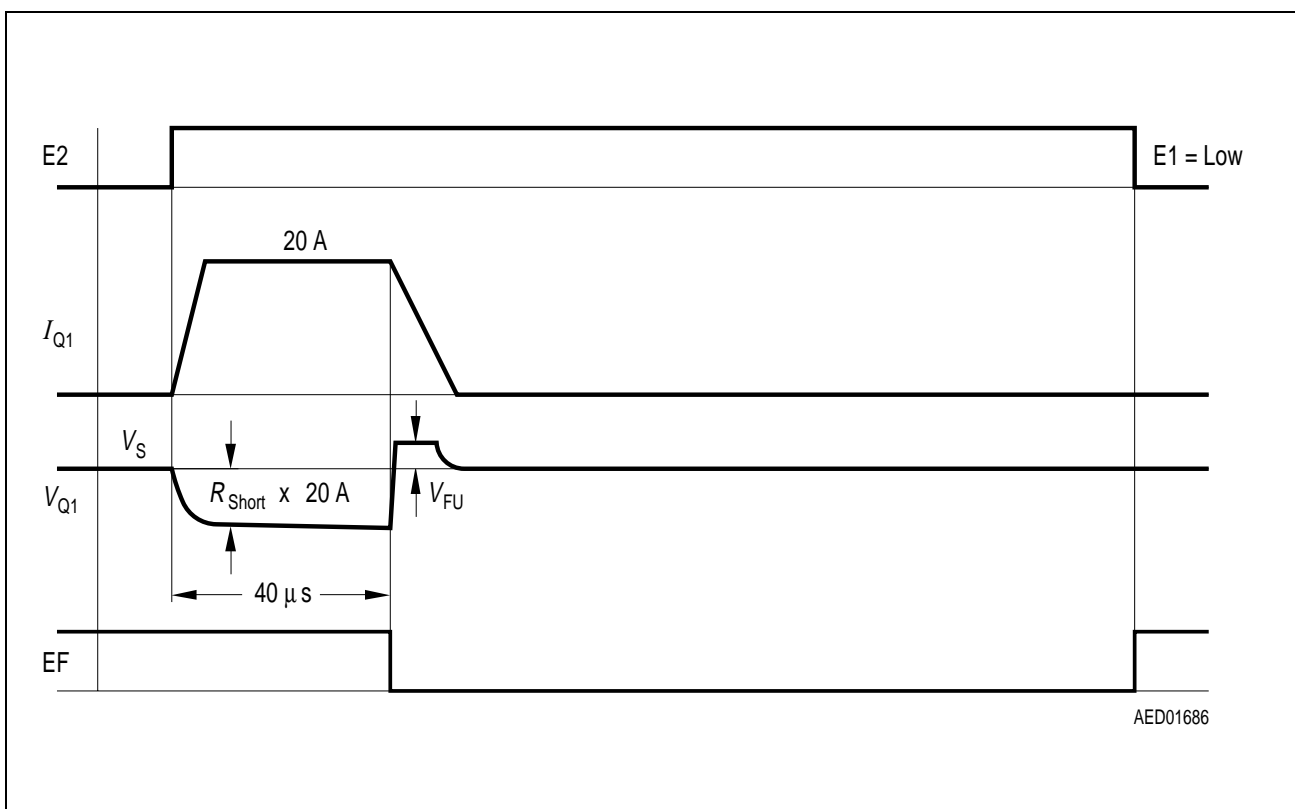
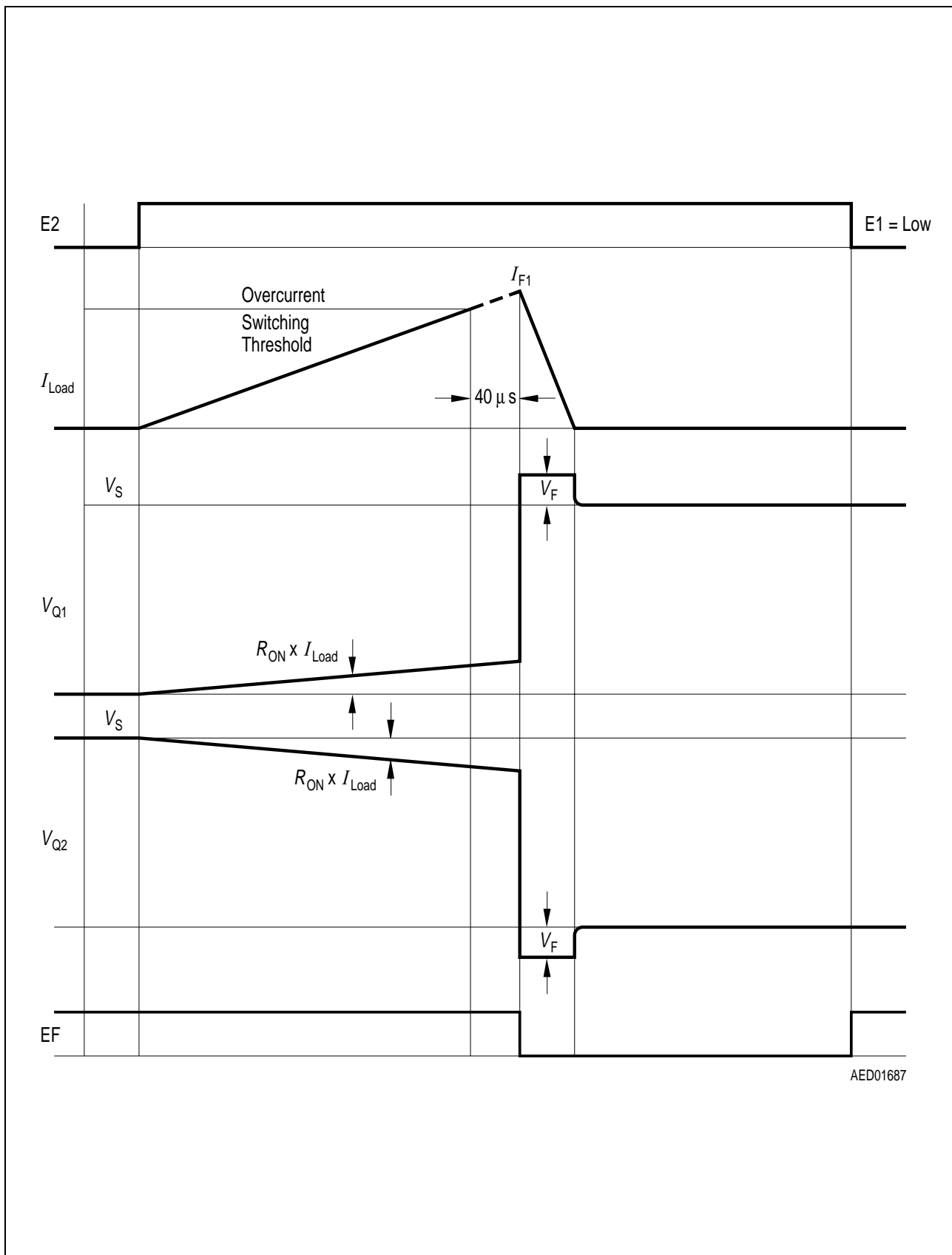


Figure 7 Timing Diagram for Output Shorted to V<sub>s</sub>

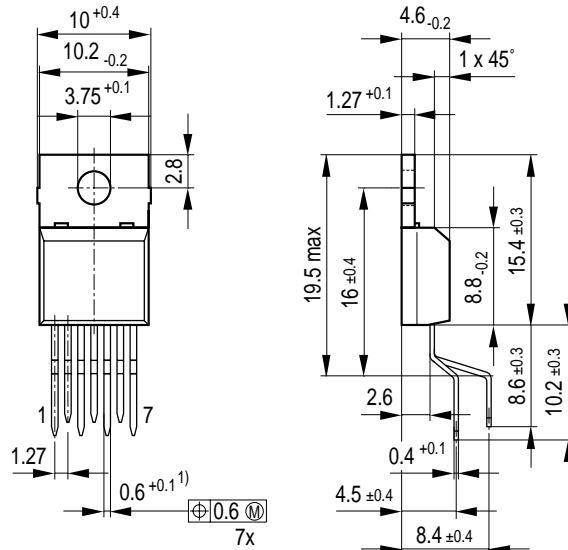


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Figure 8 Timing Diagram for Overcurrent

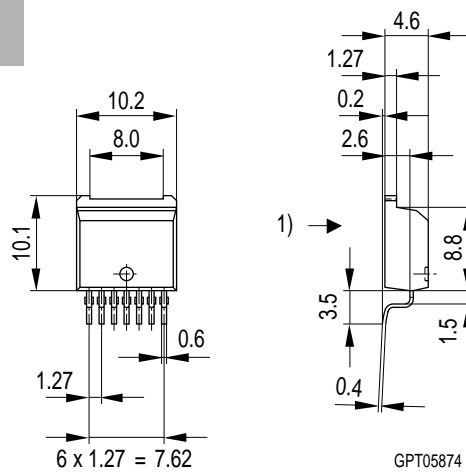
Package Outlines

**P-TO220-7-1**  
(Plastic Transistor Single Outline)



- 1) 0.75<sup>-0.15</sup> at dam bar (max 1.8 from body)
  - 1) 0.75<sup>-0.15</sup> im Dichtstegbereich (max 1.8 vom Körper)
- GPT05108

**P-TO220-7-8 (SMD)**  
(Plastic Transistor Single Outline)



- 1) shear and punch direction burr free surface

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm