Ordering number: EN 2019A

SANYO

No.2019A

2SB1124/2SD1624

PNP/NPN Epitaxial Planar Silicon Transistors

High-Current Switching Applications

Applications

. Voltage regulators, relay drivers, lamp drivers, electrical equipment.

Features

. Adoption of FBIT, MBIT processes.
. Low collector-to-emitter saturation voltage.
. Fast switching speed.
. Large current capacity and wide ASO

( ): 2SB1124

Absolute Maximum Ratings at Ta=25°C

			unit
Collector to Base Voltage	V_{CBO}	(-)60	V
Collector to Emitter Voltage	V_{CEO}	(-)50	V
Emitter to Base Voltage	V_{EBO}	(-)6	V
Collector Current	I_C	(-)3	A
Collector Current(Pulse)	I_{CP}	(-)6	A
Collector Dissipation	P_C	500	mW
	Mounted on ceramic board (250mm^2 x 0.8mm)	1.5	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55 to +150	°C

Electrical Characteristics at Ta=25°C

			min	typ	max	unit
Collector Cutoff Current	I_{CBO}	V_{CB}=(-)40V, I_E=0			(-)1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=(-)4V, I_C=0			(-)1	μA
DC Current Gain	$h_{FE}(1)$	V_{CE}=(-)2V, I_C=(-)100mA	100*		560*	
	$h_{FE}(2)$	V_{CE}=(-)2V, I_C=(-)3A	35			
Gain-Bandwidth Product	f_T	V_{CE}=(-)10V, I_C=(-)50mA		150		MHz
Output Capacitance	c_{ob}	V_{CB}=(-)10V, f=1MHz		(39)		pF
				25		pF

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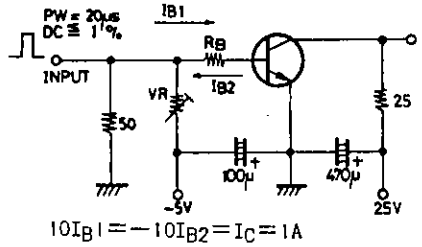
*: The 2SB1124/2SD1624 are classified by 100mA h_{FE} as follows:

100 R 200	140 S 280	200 T 400	280 U 560

Marking 2SB1124: BG
2SD1624: DG

h_{FE} rank : R, S, T, U

Switching Time Test Circuit



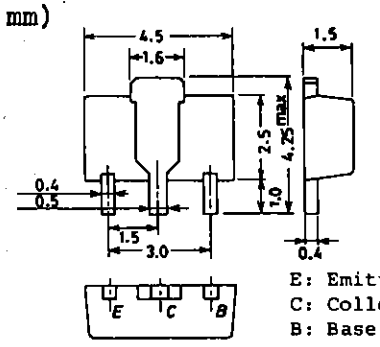
$10I_{B1} = -10I_{B2} = I_C = 1A$

(For PNP, the polarity is reversed.)

Unit (Resistance : Ω, Capacitance : F)

Package Dimensions 2038

(unit: mm)



E: Emitter
C: Collector
B: Base

SANYO: PCP

(Bottom View)

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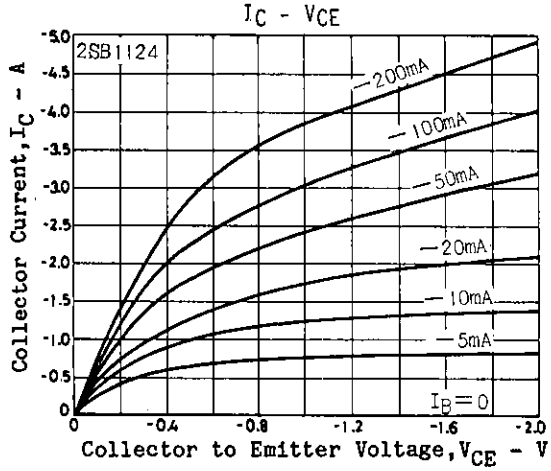
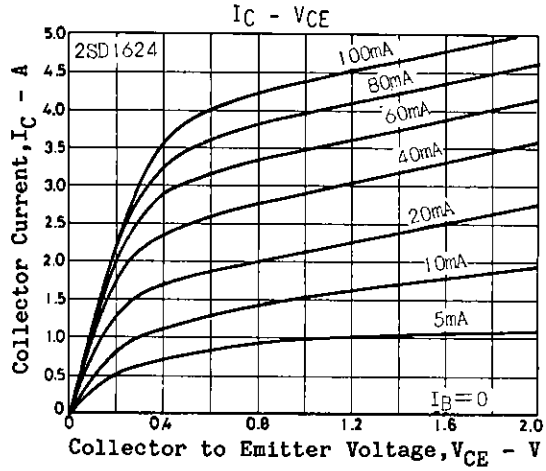
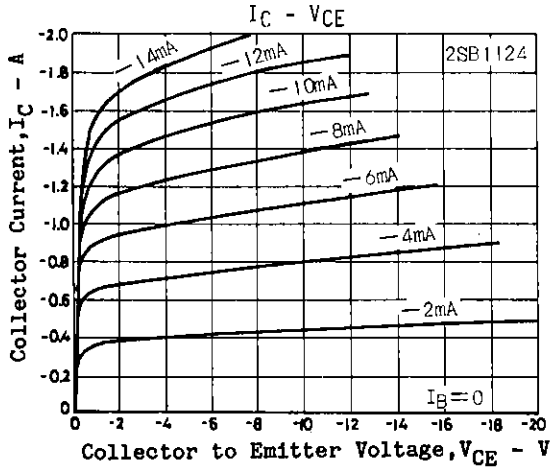
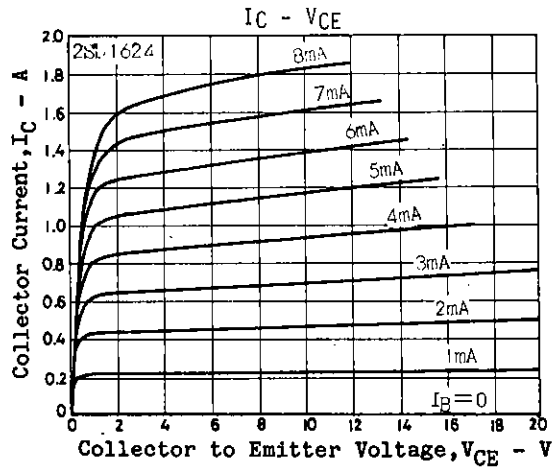
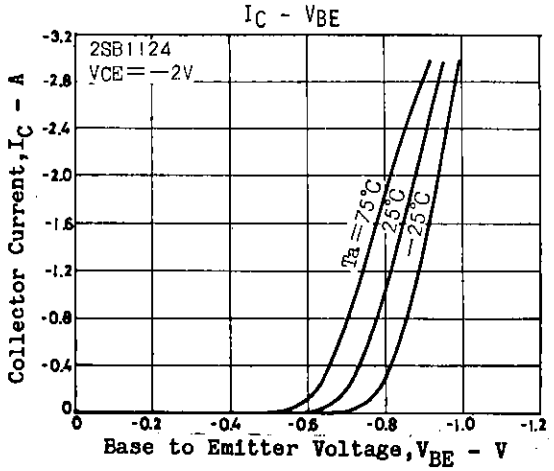
			min	typ	max	unit
C-E Saturation Voltage	$V_{CE(sat)}$	I_C=(-)2A, I_B=(-)100mA		(-0.35)	(-0.7)	V
				0.19	0.5	V
B-E Saturation Voltage	$V_{BE(sat)}$	I_C=(-)2A, I_B=(-)100mA		(-0.94)	(-)1.2	V
C-B Breakdown Voltage	$V_{(BR)CBO}$	I_C=(-)10μA, I_E=0	(-)60			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	I_C=(-)1mA, R_{BE}=∞	(-)50			V
E-B Breakdown Voltage	$V_{(BR)EBO}$	I_E=(-)10μA, I_C=0	(-)6			V
Turn-on Time	t_{on}	See specified Test Circuit.		(70)		ns
		"		70		ns
Storage Time	t_{stg}	"		(450)		ns
		"		650		ns
Fall Time	t_f	"		(35)		ns
		"		35		ns

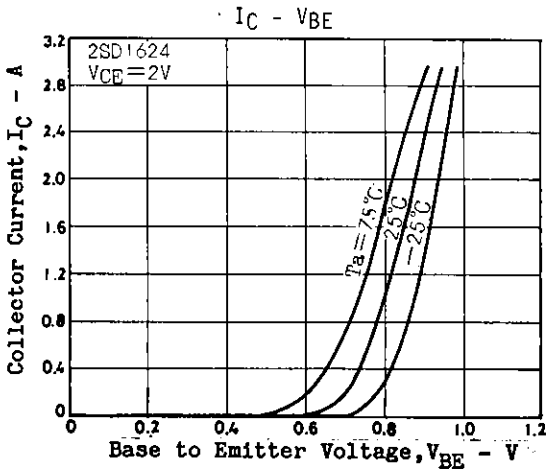




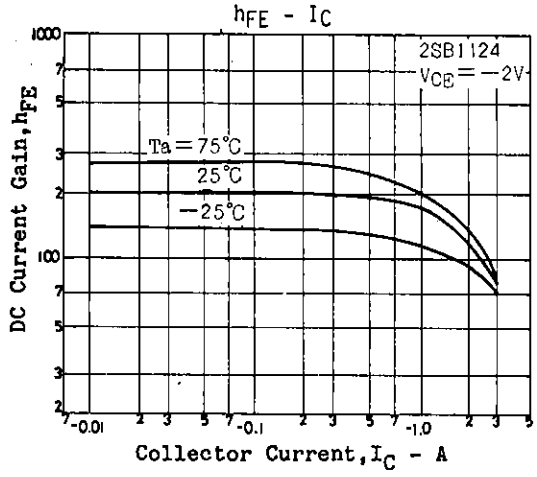




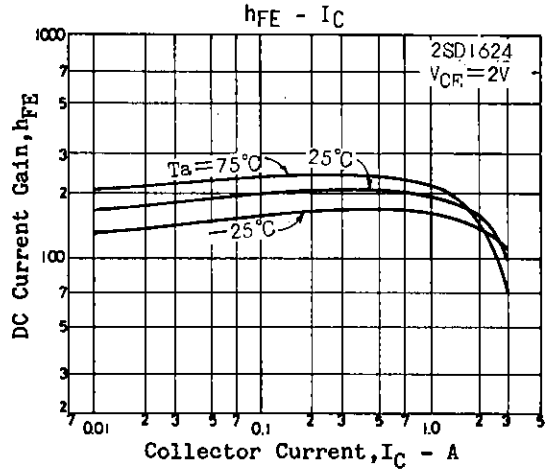




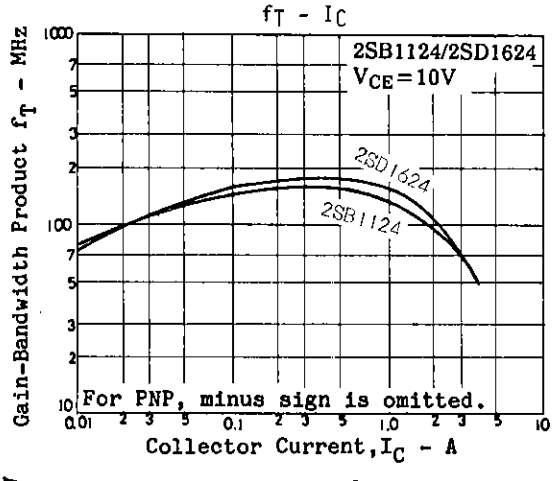
h_{FE} - I_C



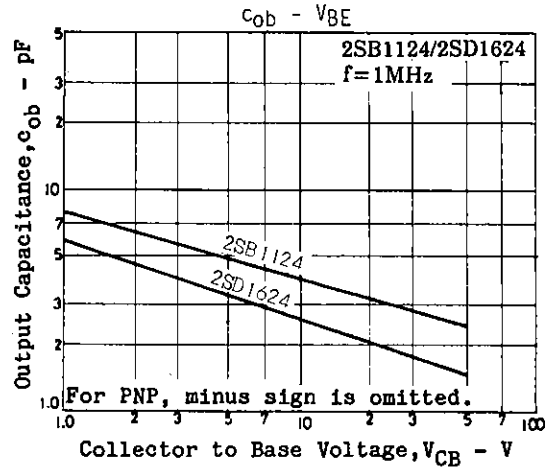
h_{FE} - I_C



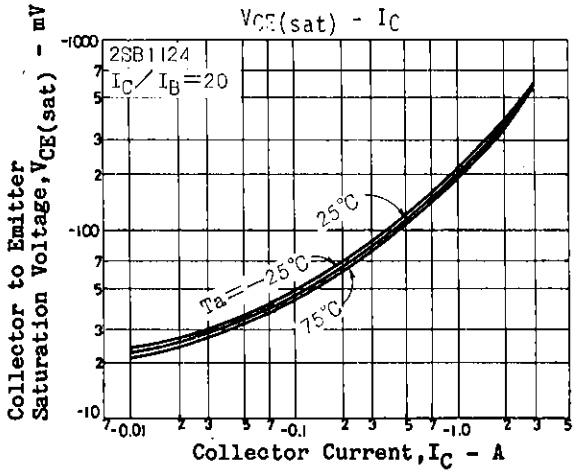
f_T - I_C



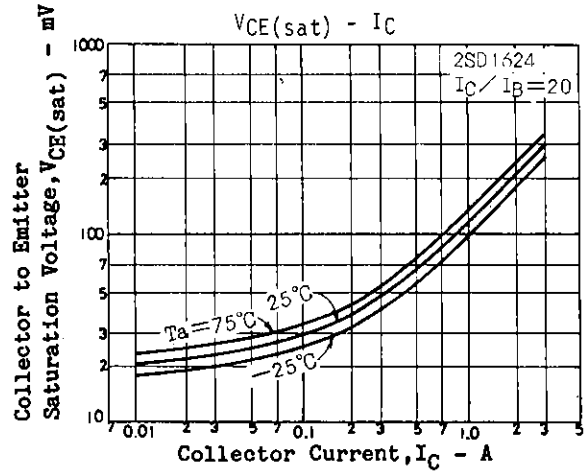
C_{ob} - V_{BE}



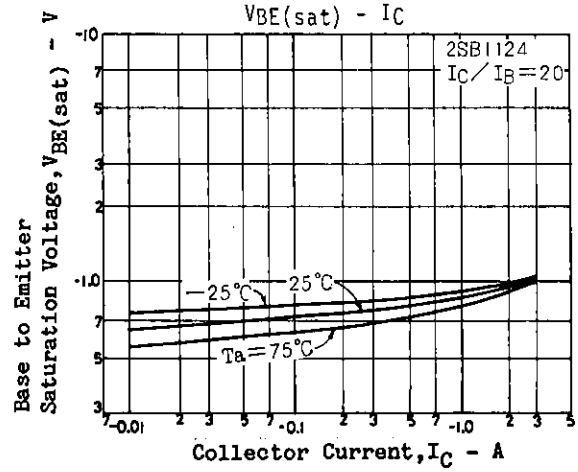
$V_{CE(sat)}$ - I_C



$V_{CE(sat)}$ - I_C



$V_{BE(sat)}$ - I_C



$V_{BE(sat)}$ - I_C